

**Color Killer Circuit for Generating Color Killer Signal
and Color Television Receiver having the Color Killer Circuit**

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to a color killer circuit to be assembled in a color television receiver for disabling output operation of a color signal when field strength of a television signal is lowered.

Description of the Prior Art

In general, a color television receiver is provided with a color killer circuit for generating a color killer signal to disable output operation of a color signal from a color reproducing circuit. The color killer circuit compares the amplitude of a burst signal included in the television wave with a reference level. When the television wave is transmitted in monochrome broadcasting or the level of color signal components included in the television wave is extremely small, the burst signal is lower than the reference level. In such a state, the color killer circuit generates the color killer signal, which disables output operation of a color signal from the color reproducing circuit. Thus, color noise on the receiving screen is removed and a monochrome image appears on the receiving screen.

In recent years there is a requirement for reduction of

the reference level (killer level) in the color killer circuit. Namely, activation of the color processing circuit is required even if field strength of the television wave is extremely low, so far as synchronization between the scannings of the receiving screen and the television wave is maintained. Thus, there is proposed technique of providing a synchronous wave detection circuit in an automatic color saturation control circuit (ACC circuit) for lowering the killer level.

However, when the killer level is lowered the color killer circuit sometimes causes a malfunction even when the color killer signal should be generated. When, for example, field strength of a television wave received by an antenna is gradually lowered, a color killer signal is activated in a region where the field strength is lower than a certain field strength value as expected. If the field strength is further lowered to realize no television wave state, the color killer circuit malfunctions through noise, whereby the color killer signal temporarily enters an inactive state. As the result, color noise appears on the receiving screen.

In order to prevent such a malfunction, the killer level of a conventional color killer circuit is set at a level higher by two dB or three dB than a desired level. The function of the color killer circuit is not sufficiently effectuated in such conventional technique although the color killer circuit is capable to correctly operate so far as the burst signal has a

finite amplitude.

SUMMARY OF THE INVENTION

The present invention is directed to a colour killer circuit which is assembled in a colour television receiver to generate a colour killer signal for disabling output operation of a colour signal from a colour processing circuit provided in the colour television receiver when strength of a television signal is lowered.

The colour killer circuit comprises burst lowering detecting means for comparing an amplitude of a burst signal included in the television signal with a prescribed reference level to generate a burst lowering detecting signal which is a DC signal and is activated when the amplitude is lower than the reference level; synchronisation detecting means for detecting synchronisation between a synchronous signal obtained from the television signal and a periodic pulse signal for indicating timing of actual image scanning in the colour television receiver to generate a synchronisation detecting signal which is a DC signal and is activated when the synchronisation is established; and gate means for passing the burst lowering detecting signal when the synchronisation detecting signal is at an active level while continuously outputting an active level when the synchronisation detecting signal is at an inactive level thereby to generate a colour killer signal.

According to an embodiment of the present invention, a colour television receiver receiving a television signal for reproducing a colour television image comprises burst lowering detecting means for comparing an amplitude of a burst signal included in the television signal with a prescribed reference level to generate a burst lowering detecting signal which is a DC signal and is activated when the amplitude is lower than the reference level; synchronisation detecting means for detecting synchronisation between a synchronous signal obtained from the television signal and a periodic pulse signal indicating timing of actual image scanning on a display provided in the colour television receiver to generate a synchronisation detecting signal which is a DC signal and is activated when the synchronisation is established; gate means for passing the burst lowering detecting signal only when the synchronisation detecting signal is at an active level while continuously outputting an active level when the synchronisation detecting signal is at an ~~active~~^{inactive} level thereby to generate a colour killer signal; and colour

killer signal transfer means for transferring the colour killer signal to a circuit for generating a colour signal in the colour television receiver thereby to disable output operation of the colour signal when the colour killer signal is at an active level.

Accordingly, an object of the present invention is to provide a colour killer circuit which causes no malfunction even if a killer level is set at a low value.

Another object of the present invention is to provide a

color television receiver in which no color noise appears on the screen even if a killer level is set at a low value.

These and other objects, features, aspects and advantages of the present invention will become more apparent from the following detailed description of the present invention when taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is an overall block diagram showing a color television receiver having a color killer circuit according to an embodiment of the present invention;

Fig. 2 is a block diagram showing process for generating flyback pulse;

Figs. 3 and 4 are block diagrams showing examples of internal structure of a horizontal synchronization detector;

Figs. 5A to 5C are waveform diagrams showing operation of the synchronization detector as shown in Fig. 4.

Fig. 6 is a block diagram showing exemplary internal structure of a color burst lowering detector;

Figs. 7A to 7D are waveform diagrams showing operation of the embodiment of the present invention; and

Fig. 8 is an explanatory diagram showing a modification of the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENT

Fig. 1 is a block diagram showing a color television receiver which is provided with a color killer circuit according

to an embodiment of the present invention. A television wave W is received by an antenna ANT of a color television receiver 1, to provide a television signal S including a video signal and a sound signal. A video signal receiving circuit 2 receives the television signal S , to generate a color television signal S_1 , a luminance signal Y and an intermediate frequency signal S_m . A sound receiving circuit 3 generates a sound signal S_0 on the basis of the intermediate frequency signal S_m , to supply the same to a speaker SP. The luminance signal Y is outputted to a color signal reproducing circuit 4.

The color television signal S_1 is supplied to a synchronous deflection circuit 6, which in turn generates a horizontal sawtooth current I_H and a vertical sawtooth current I_V on the basis of a horizontal synchronous signal and a vertical synchronous signal included in the color television signal S_1 . The sawtooth currents I_H and I_V are supplied to a deflection coil of a CRT 5 provided in the television receiver 1 as a display, thereby to perform horizontal scanning and vertical scanning on a screen of the CRT 5. The horizontal sawtooth current I_H is further supplied to a high-voltage rectifying circuit 7. The high-voltage rectifying circuit 7 rectifies the horizontal sawtooth current I_H , thereby to generate DC high voltage V_0 to be supplied to an anode of the CRT 5.

The color television signal S_1 is further outputted to a

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color signal processing circuit 10. In the color signal processing circuit 10, the color television signal S_1 is amplified by first bandpass amplifier 11 to provide first chrominance carrier signal S_2 , which is further amplified by second bandpass amplifier 12 to be amplified to give second chrominance signal S_3 . A signal including the first chrominance carrier signal S_2 and a color burst signal S_B obtained by the first bandpass amplifier 11 is supplied to a color synchronizing circuit 14. The color synchronizing circuit 14 extracts the color burst signal S_B from the inputted signal, to output the same to an ACC circuit 15. The ACC circuit 15 generates a gain control signal S_G on the basis of the color burst signal S_B , to output the same to the first bandpass amplifier 11. This gain control signal S_G is utilized for gain control in the first bandpass amplifier 11.

The color synchronizing circuit 14 generates a reference subcarrier signal S_4 , to supply the same to a color demodulating circuit 13. The color demodulating circuit 13 generates a color signal S_C on the basis of the carrier chrominance signal S_3 and the reference subcarrier signal S_4 , to output the same to the color signal reproducing circuit 4. The color signal reproducing circuit 4 generates primary color signals R, G and B on the basis of the luminance signal Y and the color signal S_C , to output the same to the CRT 5. Electron beams generated in the CRT 5 are controlled by the primary color signals R, G and B.

to collide with fluorescent materials on the screen while oscillating by a horizontal scanning and a vertical scanning, thereby a color image is displayed on the screen of the CRT 5.

The color television receiver 1 is provided with a color killer circuit 20. The color killer circuit 20 includes a synchronization detector 30, a color burst lowering detector 40 and an AND circuit 50. The synchronization detector 30 receives a horizontal synchronous signal S_H supplied from the synchronizing deflection circuit 6 and flyback pulse FB supplied from the high-voltage rectifying circuit 7. The horizontal synchronous signal S_H is obtained from the horizontal synchronizing component included in the television signal S. The flyback pulse FB is obtained from a flyback transformer FBT provided in the high-voltage rectifying circuit 7.

Fig. 2 is a block diagram showing a circuit for obtaining the flyback pulse FB. With respect to internal circuits of the synchronous deflection circuit 6, only those required for illustration are shown in Fig. 2. An AFC circuit 61 receives the horizontal synchronous signal S_H generated in the synchronous deflection circuit 6 on the basis of the horizontal synchronizing component of the television signal S. The AFC circuit 61 further receives a horizontal pulse S_7 supplied from the flyback transformer FBT. The horizontal pulse S_7 and the horizontal synchronous signal S_H are compared with each other with respect to their phases so that an AFC signal S_5

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is generated. On the basis of the AFC signal S_5 , an oscillation circuit 62 generates a horizontal drive pulse S_6 for driving a horizontal drive transistor 64 included in a horizontal drive and horizontal output circuit 63. The horizontal drive pulse S_6 and other pulses generated therefrom are locked in frequency and phase with the horizontal synchronous signal S_H when the strength of the television signal S is not extremely low. The horizontal drive and horizontal output circuit 63 generates a horizontal output pulse S_p at a horizontal output transistor 65 on the basis of output of the horizontal drive transistor 64. The horizontal output pulse S_p is used to supply the horizontal sawtooth current I_H to the horizontal deflection coil 66 and the flyback transformer FBT. The flyback pulse FB is obtained as pulse generated in the flyback transformer FBT in a flyback time of the horizontal sawtooth current I_H . The horizontal pulse S_7 is generated at the flyback transformer FBT in the same manner.

The horizontal sawtooth current I_H determines timing of actual horizontal image scanning on the screen of the CRT 5. Thus, the horizontal drive pulse S_6 , the flyback pulse FB, and the horizontal pulse S_7 are periodic pulses for indicating the timing of the actual horizontal image scanning. These pulses are in synchronism with the horizontal output pulse S_p .

Fig. 3 shows an example of internal structure of the synchronization detector 30 of Fig. 1. The horizontal synchronous signal S_H and the flyback pulse FB are inputted in

an AND circuit 31. Output of the AND circuit 31 is supplied to a comparator 33 through a low-pass filter circuit 32. Therefore, when the horizontal synchronous signal S_H and the flyback pulse FB are in phase with each other, the AND circuit 31 outputs high level periodically and DC component thereof is transmitted to the comparator 33 through the filter circuit 32. Therefore, in this case, a substantially constant positive voltage level V_1 is supplied to the comparator 33. The comparator 33 is also supplied with reference voltage V_2 ($0 < V_2 < V_1$). Therefore, a synchronization detecting signal S_{sync} is at a high level.

When the horizontal synchronous signal S_H and the flyback pulse FB are not in synchronization with each other, the output of the AND circuit 31 is at a zero level. As the result, the synchronization detecting signal S_{sync} goes low.

Fig. 4 shows another example of the synchronization detector 30, which is implemented in the form of an analog circuit. First, consider such case where synchronization is established between the horizontal synchronous signal S_H and the flyback pulse FB as shown in Fig. 5A. Symbols I_1 and I_2 in Fig. 5A indicate collector currents of transistors Q_1 and Q_2 in Fig. 4, respectively. When the synchronization is established, transistors Q_4 and Q_5 included in a differential amplifier 34 are strongly turned on, because the horizontal synchronous signal S_H and the flyback pulse FB are supplied to bases of the

transistor Q_4 and Q_5 , respectively. First output S_8 of the differential amplifier 34 pulsingly goes low while second output S_9 thereof pulsingly goes high level corresponding to a power source level V_{cc} . As the result, the transistor Q_1 pulsingly enters an on state and the transistor Q_2 pulsingly enters an off state. A signal S_{10} supplied from a collector of the transistor Q_1 is changed to a pulsating high level signal through the filter function of a filter circuit 32. Thus, a synchronization detecting signal S_{sync} obtained from a comparator 33 goes high.

When the horizontal synchronous signal S_H and the flyback pulse FB are in lack of synchronization as shown in Fig. 5B, only the transistor Q_4 and another transistor Q_3 simultaneously enter on states. The first output S_8 remains at a high level and the transistor Q_1 is in an off state. The transistor Q_2 enters an on state when the horizontal synchronous signal S_H is at a high level. As the result, the charge of a capacitor C in the filter 32 is discharged and the level of the signal S_{10} becomes low so that the synchronization detecting signal S_{sync} goes low. When the horizontal synchronous signal S_H is completely lacking, the waveforms as shown in Fig. 5C are obtained and the synchronization detecting signal S_{sync} goes low.

On the other hand, the color burst lowering detector 40 of Fig. 1 can be formed through a comparator 41 shown in Fig. 6. The comparator 41 is supplied in its first input with the color

burst signal S_B and with a reference level V_3 in its second input. The reference level V_3 is in a relatively low positive value. Therefore, a burst lowering detecting signal S_{BL} is changed into an active low level only when the burst signal S_B is at a sufficiently low level which is lower than the reference level V_3 . The burst lowering detecting circuit 40 shown in Fig. 6 corresponds to a color killer detector employed in a conventional color television circuit.

As shown in Fig. 1, the horizontal synchronous signal S_H and the burst lowering detecting signal S_{BL} are supplied to an AND circuit 50. The AND circuit 50 in turn generates a color killer signal S_K having a level responsive to the logical sum of the horizontal synchronous signal S_H and the burst lowering detecting signal S_{BL} . The color killer signal S_K is transferred to the second bandpass amplifier 12 through a transfer line L. When the color killer signal S_K is at an active low level, the second bandpass amplifier 12 is disabled so that output operation of the color signal S_C is prevented.

Figs. 7A to 7D are waveform diagrams showing operation of the color killer circuit 20. When synchronization is established between horizontal image scanning in the CRT 5 and the horizontal synchronous signal S_H as shown in Fig. 7A, the synchronization detecting signal S_{sync} maintains an active high level. Under such condition that field strength of the television wave W is sufficiently high, the burst lowering

detecting signal S_{BL} is at a high level since the amplitude of the burst signal S_B (not shown in Fig. 7A) has a sufficiently high level. Therefore, the color killer signal S_K outputted from the AND circuit 50 is at an inactive high level, so that the color signal S_C is generated. As the result, a color image is obtained on the screen of the CRT 5.

When field strength of the television wave W is lowered, the horizontal synchronous signal S_H is separated into fine pulses as shown in Fig. 7B. Further, noise N appears in the horizontal synchronous signal S_H . However, the synchronization detecting signal S_{sync} maintains a high level if the field strength is not extremely lowered. Reduction in amplitude of the burst signal S_B is also relatively small, and hence the burst lowering detecting signal S_{BL} is at an inactive high level. As the result, the color killer signal S_K is at an inactive high level.

As shown in Fig. 7C, the synchronization detecting signal S_{sync} maintains the active high level even if the field strength of the television wave W is further lowered. This is because detecting ability of the synchronization detector 30 is considerably high. In such a state, however, the burst signal S_B is lower than the reference level V_3 . In response to this, the burst lowering detecting signal S_{BL} is changed into an active low level. Thus, the color killer signal S_K is changed into an active low level, whereby output operation of the color

signal S_C is disabled.

It is understood from Figs. 7A to 7C that the burst lowering detecting signal S_{BL} passes through the AND circuit 50 when the synchronization detecting signal S_{sync} is at an active high level, whereby the color killer signal S_K is generated. The AND circuit 50 performs operation as a gate circuit whose gate signal is the synchronization detecting signal S_{sync} .

Then, consider such case where field intensity of the television wave W is substantially zero as shown in Fig. 7D. In such a state, the horizontal synchronous signal S_H substantially includes only the noise N . This also applies to the case where a null channel is selected. Since the horizontal synchronous signal S_H includes no effective synchronizing pulse, synchronization between the horizontal synchronous signal S_H and the flyback pulse signal F_B is lost and the synchronization detecting signal S_{sync} is changed into an inactive low level. This is because a state substantially equivalent to that of Fig. 5C appears in Fig. 7D.

In such a state, the burst signal S_B is lower than the reference level V_3 , whereby the burst lowering detecting signal S_{BL} is changed into an active low level. However, when noise is superposed on the burst signal S_B , the burst lowering detecting signal S_{BL} is temporarily changed into an inactive high level in a period F of Fig. 7D, for example. If the burst lowering detecting signal S_{BL} is directly employed as the color killer

signal S_K as the conventional color killer detector, color noise will appear on the screen of the CRT 5. However, the color killer signal S_K is provided by the logical sum of the synchronization detecting signal S_{sync} and the burst lowering detecting signal S_{BL} in this embodiment. Thus, the color killer signal S_K maintains the active low level as shown in Fig. 7D, and no color noise will appear on the screen of the CRT 5.

Since the synchronization detector 30 has sufficiently high detection sensitivity in general, the color killer signal S_K is changed into an active low level only when strength of the television signal S is sufficiently low, regardless of the level of the burst lowering detecting signal S_{BL} . Therefore, the requirement for reduction of the killer level of the color killer circuit 20 is sufficiently satisfied. According to an experiment made by the inventor, it is possible to lower the killer level over 3 dB as compared with the conventional case.

According to the present invention, the horizontal drive pulse S_6 can also be employed as periodic pulse for indicating actual image scanning on the screen of the CRT 5 in place of the flyback pulse FB. Other periodic pulse synchronous with the horizontal output pulse S_p can also be employed. The synchronization detector 30 may be provided not only for the control of the color killer circuit 20, but also for automatic station discrimination or mute signal generation. Further, the AND circuit 50 may be replaced by a gate circuit 90 shown in

Fig. 8, which comprises a selector 91 adapted to select its A input when the synchronization detecting signal S_{sync} is at an active high level, while selecting its B input in other case.

Synchronization between a vertical synchronous signal and actual vertical scanning on the screen of the CRT 5 may be detected to generate the synchronization detecting signal. However, detection of horizontal synchronization is more preferable since detection sensitivity for horizontal synchronization is higher than that for vertical synchronization.



CLAIMS:

1. A colour killer circuit to be assembled in a colour television receiver for generating a colour killer signal for disabling the output of a colour signal from a colour processing circuit in said colour television receiver when the strength of a television signal is lowered, said colour killer circuit comprising:

burst lowering detecting means for comparing an amplitude of a burst signal included in said television signal with a prescribed reference level to generate a burst lowering detecting signal which is a DC signal and is activated when said amplitude is lower than said reference level;

synchronisation detecting means for detecting synchronisation between a synchronous signal obtained from said television signal and a periodic pulse signal for indicating the timing of image scanning on a display provided in said colour television receiver to generate a synchronisation detecting signal which is a DC signal and is activated when said synchronisation is established; and

gate means for passing said burst lowering detecting signal when said synchronisation detecting signal is at an active level while continuously outputting an active level when said synchronisation detecting signal is at an inactive level, thereby to generate said colour killer signal.



2. A color killer circuit in accordance with claim 1, wherein

said synchronous signal is a horizontal synchronous signal.

3. A color killer circuit in accordance with claim 2, wherein

said periodic pulse signal is a signal synchronous with horizontal output pulse generated in said color television receiver, and

said synchronization detecting means is a synchronization detector for detecting synchronization between said periodic pulse signal and said horizontal synchronous signal.

4. A color killer circuit in accordance with claim 3 wherein

said periodic pulse signal is flyback pulse.

5. A color killer circuit in accordance with claim 1, wherein

an activated state of said synchronization detecting signal is expressed by a high level.

respective active states of said burst lowering



detecting signal and said colour killer signal are expressed by low levels, and

said gate means is an AND circuit for receiving said burst lowering detecting signal and said synchronisation detecting signal to obtain the logical product of said burst lowering detecting signal and said synchronisation detecting signal.

6. A television receiver for receiving a television signal for reproducing a colour television image, said colour television receiver comprising:

burst lowering detecting means for comparing an amplitude of a burst signal included in said television signal with a prescribed reference level to generate a burst lowering detecting signal which is a DC signal and is activated when said amplitude is lower than said reference level;

synchronisation detecting means for detecting synchronisation between a synchronous signal obtained from said television signal and a periodic pulse signal for indicating timing of actual image scanning on a display provided in said colour television receiver to generate a synchronisation detecting signal which is a DC signal and is activated when said synchronisation is established;

gate means for passing said burst lowering detecting signal only when said synchronisation detecting signal is at an



active level while continuously outputting an active level when said synchronization detecting signal is at an inactive level, thereby to generate said color killer signal; and

color killer signal transfer means for transferring said color killer signal to a circuit for generating a color signal in said color television receiver thereby to disable output operation of said color signal when said color killer signal is at an active level.

7. A color television receiver in accordance with claim 6, wherein

said synchronous signal is a horizontal synchronous signal.

8. A color television receiver in accordance with claim 7, wherein

said periodic pulse signal is a signal synchronous with horizontal output pulse generated in said color television receiver, and

said synchronization detecting means is a synchronization detector for detecting synchronization between said periodic pulse signal and said horizontal synchronizing signal.

9. A color television receiver in accordance with claim



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8, wherein

said periodic pulse signal is flyback pulse.

10. A colour television receiver in accordance with claim 6, wherein

an activated state of said synchronisation detecting signal is expressed by a high level,

respective active states of said burst lowering detecting signal and said colour killer signal are expressed by low levels, and

said gate means is an AND circuit for receiving said burst lowering detecting signal and said synchronisation detecting signal to obtain the logical product of said burst lowering detecting signal and said synchronisation detecting signal.
