METHODS OF FORMING ISOLATED ACTIVE AREAS, TRENCHES, AND CONDUCTIVE LINES IN SEMICONDUCTOR STRUCTURES AND SEMICONDUCTOR STRUCTURES INCLUDING THE SAME

TECHNICAL FIELD

Embodiments of the invention relate to integrated circuit fabrication and, more specifically, to methods of forming asymmetric features on semiconductor structures and semiconductor structures including the asymmetric features.

BACKGROUND

As a consequence of many factors, including demand for increased portability, computing power, memory capacity and energy efficiency in modern electronics, integrated circuits are continuously being reduced in size. To facilitate this size reduction, the sizes of the constituent features, such as electrical devices and interconnect line widths that form the integrated circuits, are also constantly being decreased.

The continual reduction in feature size places ever greater demands on techniques used to form the features. For example, photolithography is a conventional method of patterning features, such as conductive lines, on a substrate. The concept of pitch may be used to describe the size of these features. Pitch is defined as the distance between identical points in two neighboring features. These features are conventionally defined by spacings between adjacent features, which may be filled by a material, such as an insulator. As a result, pitch may be viewed as the sum of the width of a feature and of the width of the space separating that feature from a neighboring feature, or the distance between one edge of a feature and the corresponding same edge of the next adjacent feature. However, due to factors such as optics and light or radiation wavelength, photolithography techniques have a minimum pitch below which the particular photolithographic technique cannot reliably form features. Thus, the minimum pitch of a photolithographic technique may limit feature size reduction.

Pitch doubling, or pitch multiplication, techniques have been proposed for extending the capabilities of photolithographic techniques. One example of a method of pitch multiplication is illustrated in FIGS. 1A-1F herein and described in U.S. Pat. No. 5,328,810, issued to Lowrey et al., the entire disclosure of which is incorporated herein by reference. With reference to FIG. 1A, photolithography may first be used to form a pattern of lines 10 in a photoresist material overlying a layer 20 of an expendable material and a substrate 30. As shown in FIG. 1B, the pattern may then be transferred by an etch step (preferably anisotropic)

to the layer 20, forming placeholders, or mandrels 40. The photoresist lines 10 may be stripped and the mandrels 40 may be isotropically etched to increase the distance between neighboring mandrels 40, as shown in FIG. 1C. A layer 50 of material may be subsequently deposited over the mandrels 40, as shown in FIG. 1D. Spacers 60, *i.e.*, material extending or originally formed extending from sidewalls of another material, may then be formed on sidewalls of the mandrels 40 by preferentially etching the spacer material from the horizontal surfaces 70 and 80 in a directional spacer etch, as shown in FIG. 1E. The remaining mandrels 40 may then be removed, leaving behind the freestanding spacers 60, as shown in FIG. 1F. The spacers 60 act as an etch mask for patterning underlying layers, as shown in FIG. 1F. Thus, where a given pitch formerly included a pattern defining one feature and one space, the same width now includes two features and two spaces. As a result, the smallest feature size possible with a photolithographic technique is effectively decreased.

However, conventional pitch doubling processes are limited in that they cannot be reliably used to pitch double asymmetric features, for example, in a DRAM array where symmetry is broken by the removal of the passing wordline over the field region. Problems arise at an array gate patterning level since three features need to be defined on a pitch: two wordlines and a grounded gate over field. The grounded gate over field balances the pattern density as well as ensures that a linear self-aligned contact etch may be performed to form cavities for conducting plugs to the storage and bit contact active regions. Conventional pitch doubling is not effective in this instance because the pitch-doubled feature on every other patterned form does not define the correct gap for the wordline versus wordline and grounded gate. Accordingly, there exists a continuing need in the art for methods of pitch doubling asymmetric features and semiconductor structures including such sub-lithographic features.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWINGS

FIGs. 1A-1F are schematic, cross-sectional views of mask lines formed in accordance with conventional pitch doubling methods;

FIG. 2 is a simplified plan view of a circuit layout for one configuration of a $6F^2$ memory array;

FIG. 3 is a cross-sectional view of an embodiment of a work piece at a preliminary stage in processing;

FIG. 4 is a plan view of an embodiment of a work piece at a stage in processing step subsequent to that illustrated in FIG. 3;

FIG. 5A is a top view of an embodiment of a semiconductor structure and FIG. 5B is a cross-sectional view of an intermediate semiconductor device;

FIG. 5C is a cross-sectional view of an embodiment of a semiconductor structure at a stage in processing subsequent to that illustrated in FIG. 5B;

FIG. 6A is a top view of an embodiment of a semiconductor structure and FIG. 6B is a cross-sectional view of the semiconductor structure of FIG. 6A taken along the dashed line labeled A;

FIG. 6C is a cross-sectional view of an embodiment of a semiconductor structure at a stage in processing step subsequent to that illustrated in FIG. 6B;

FIG. 7A is a top view of an embodiment of a semiconductor structure and FIG. 7B is a cross-sectional view of the semiconductor structure of FIG. 7A taken along the dashed line labeled A;

FIG. 8 is a cross-sectional view of an embodiment of a semiconductor structure at a stage in processing step subsequent to that illustrated in FIG. 7B;

FIG. 9 is a top view of an embodiment of a semiconductor structure at a stage in processing subsequent to that illustrated in FIG. 8;

FIG. 10A is a top view of an embodiment of a semiconductor structure and FIG. 10B is a cross-sectional view of the semiconductor structure of FIG. 10A taken along the dashed line labeled A;

FIG. 11A is a top view of an embodiment of a semiconductor structure and FIG. 11B is a cross-sectional view of the semiconductor structure of FIG. 11A taken along the dashed line labeled A;

FIG. 12A is a top view of an embodiment of a semiconductor structure at a stage in processing subsequent to that illustrated in FIG. 11B and FIG. 12B is a cross-sectional view of the semiconductor structure of FIG. 12A taken along the dashed line labeled A;

FIG. 13 is a top view of an embodiment of a semiconductor structure at a stage in processing subsequent to that illustrated in FIG. 12B;

FIG. 14A is a top view of an embodiment of a semiconductor structure and FIG. 14B is a cross-sectional view of the semiconductor structure of FIG. 14A taken along the dashed line labeled A;

FIG. 15 is a cross-sectional view of an embodiment of a semiconductor structure at a stage in processing subsequent to that illustrated in FIG. 14B;

FIG. 16 is a top view of an embodiment of a semiconductor structure at a stage in processing subsequent to that illustrated in FIG. 15;

FIGs. 17 and 18A are top views of embodiments of semiconductor structures during various stages of fabrication;

FIG. 18B is a cross-sectional view of the semiconductor structure of FIG. 18A taken along the dashed line labeled A; and

FIGs. 19 and 20 are top views of embodiments of semiconductor structures during various stages of fabrication.

DETAILED DESCRIPTION

The following description provides illustrative examples of embodiments of devices and methods of the invention with reference to the drawings. Such description is for illustrative purposes only and is nonlimiting to the scope of the invention. The drawings presented herein are not necessarily drawn to scale and are not actual views of a particular semiconductor structure or fabrication process thereof, but are merely idealized representations that are employed to describe the embodiments of the invention. As understood by a person of ordinary skill in the art, other embodiments of devices and methods may be implemented in accordance with the invention.

Semiconductor structures including at least one asymmetric, sub-lithographic feature are disclosed, as are methods of forming such semiconductor structures. Pitch doubling processes may be used to form isolated active areas on a substrate. The asymmetrical features may disrupt the symmetry between lines and spaces on the substrate. As described in detail herein and as illustrated in FIGs. 3-10B, masking materials may be formed over the substrate and patterned in a first direction on the substrate to form an active area pattern. An active area mask may be formed and patterned in a substantially perpendicular direction on the substrate and removed after formation of spacers adjacent thereto. The spacers may function as a mask during subsequent etching so that first trenches are formed between the spacers to isolate active areas on the substrate.

Subsequently, recessed access device (RAD) trenches, may be formed on the substrate. As described in detail herein and as illustrated in FIGs. 11A-15, multiple mask materials may be formed on the isolated active areas and patterned. Spacers may be formed adjacent to the mask materials and, after removal of the spacers, the mask materials may function as masks during subsequent etching to form the sub-lithographic trenches. By way of non-limiting example, the trenches may be RAD trenches, FIN trenches, double FIN trenches, or wordlines of a memory array.

Conductive lines and grounded gates of a memory array may then be formed on the substrate. As described in detail herein and as illustrated in FIGs. 16A-20, alternating mask materials and spacers may be formed above the trenches and patterned. The mask materials may be removed and the spacers may function as masks during subsequent etching to form connections to the trenches.

The following description provides specific details, such as material types, etch chemistries, and processing conditions, in order to provide a thorough description of embodiments of the invention. However, a person of ordinary skill in the art will understand

and appreciate that these and other embodiments of the invention may be practiced without employing these specific details. Indeed, embodiments of the invention may be practiced in conjunction with conventional fabrication techniques and etching techniques employed in the industry, which, therefore, are not described in detail herein. In addition, the description provided below does not form a complete process flow for manufacturing a semiconductor device. The semiconductor structures described herein do not form a complete semiconductor device. Only those process acts and semiconductor structure structures necessary to understand embodiments of the present invention are described in detail below. Additional acts to form the complete semiconductor device from the semiconductor structures may be performed by conventional fabrication techniques, which are, therefore, not described herein.

The methods described herein may be used to form semiconductor structures of memory devices, such as dynamic random access memory (DRAM), including RAD features, FinFETs, saddle FETs, nanowires, three-dimensional transistors, as well as other three-dimensional semiconductor device features. The memory device or other semiconductor device incorporating such structures may be used in wireless devices, personal computers, or other electronic devices, without limitation. By way of nonlimiting example, the methods herein describe fabricating semiconductor structures of memory devices, such as a DRAM memory device or a RAD memory device. While the methods herein describe fabricating semiconductor structures of memory devices, the methods may also be used in other situations where pitch doubling of asymmetric features is desired. In addition, while the methods described herein are illustrated in reference to a $6F^2$ DRAM device configuration or layout, the methods may be used to form DRAM devices or other semiconductor devices having other layouts, such as for example, $4F^2$ or $8F^2$ layouts, as long as the isolation regions are substantially parallel to locations where transistor gates will ultimately be formed.

Embodiments of the invention may include pitch-doubling features to form an active area, trenches in gates and/or connections to gates of a $6F^2$ memory array. FIG. 2 shows a simplified view of a portion of a circuit layout for a $6F^2$ memory array, which is referred to herein as memory array 100 including a substrate 110. A plurality of continuous active areas 112 may be formed relative to substrate 110. For purposes of clarity, each illustrated continuous active area 112 has been shown to extend outside the boundary of substrate 110. Continuous active areas 112 are conventionally non-linear, following a serpentine path across the memory array 100 in a substantially horizontal direction. A plurality of buried bit lines 118 are shown as hatched areas extending generally horizontally across memory array 100.

Each bitline 118 also follows a serpentine path across memory array 100, with the serpentine weave of the bitlines 118 being in the opposite direction relative to the weave of the continuous active areas 112.

A plurality of conductive lines 120, 134 may be formed over substrate 110 relative to the active areas 112. In FIG. 2, six of the conductive lines are designated 120 while two are designated 134. A pair of conductive lines 120 may be formed on either side of conductive line 134. Conductive lines 120, 134 run substantially orthogonally relative to the active areas 112.

Individual areas which are consumed by single memory cells in accordance with the depicted memory array are illustrated by a dashed outline designated numeral 125. Such area can be considered or described as relative to a dimension "F," which is a minimum feature size. In the illustrated example, F equals one-half of the "minimum pitch" of the memory array. The term "pitch" as used herein is intended to be used in its conventional usage, and (as previously noted) may be defined as the distance between one edge of a device or feature and the corresponding same edge of the next adjacent device or feature. Accordingly, with respect to the memory cell 125, the term "minimum pitch" is about equal to the smallest distance of a line width (such as conductive lines 120, 134) plus the width of a space immediately adjacent the conductive line 120 on one side of the conductive line 120 between the conductive line 120 and the next adjacent conductive line 120 in a repeated pattern within the memory cell 125. As shown, a single memory cell 125 is about 3F wide by about 2F deep, thus providing a consumed area for a single memory cell 125 of about $6F^2$.

In examples of implementations of the memory array 100, such as that depicted in FIG. 2, selected individual conductive lines may provide electrical isolation relative to adjacent memory cells 125. For instance, as depicted, conductive lines 120 serve as wordlines relative to individual memory cells 125. Electrical isolation between adjacent pairs of memory cells 125 is provided by intervening conductive line 134, which, in operation, may be connected with ground or a suitable negative voltage. Alternatively, field oxide isolation techniques may be utilized.

The memory array 100 depicted in FIG. 2 may additionally include capacitor containers 136 and bitline contacts 138. Capacitors may conventionally be formed within capacitor containers 136 and may be coupled to active areas via storage node contacts 140. In particular aspects, the storage node contacts 140 may include a conductive material which extends to a node portion of an active area.

It is noted with reference to FIG. 2 that the capacitor containers 136 depicted have a pitch substantially equivalent to the pitch of the memory cell 125. In other words, the width of each capacitor container 136 (in a vertical direction on the page) plus the width of the space between immediately adjacent capacitor containers (in a vertical direction on the page) is substantially equivalent to the pattern pitch "P," where P is the sum of the line width "W" plus the width of the space "S" immediately adjacent the line, as depicted in FIG. 2.

To form the memory array 100 depicted in FIG. 2, masking materials are used in combination with a substantially vertical etch of materials overlying the substrate 110 to form self-aligned features in or on the substrate 110. As used herein "self-aligned" means and includes using a single photomask to form an initial pattern upon which other features are based. As such, features formed on the substrate 110 are aligned without utilizing additional masking and photolithography acts. The substrate may be a conventional silicon substrate or other bulk substrate comprising a layer of semiconductive material. As used herein, the term "bulk substrate" means and includes not only silicon wafers, but also silicon-on-insulator ("SOI") substrates, such as silicon-on-sapphire ("SOS") substrates and silicon-on-glass ("SOG") substrates, epitaxial layers of silicon on a base semiconductor foundation, and other semiconductor or optoelectronic materials, such as silicon-germanium, germanium, gallium arsenide, gallium nitride, and indium phosphide.

FIGs. 3-10B depict an embodiment of a semiconductor structure 200 at various stages of fabrication using pitch doubling to form an isolated active area on the substrate 110. FIG. 3 depicts the semiconductor structure 200 with various materials which may include insulative material 250, an optional etch-stop material 260, first expendable material 212 and selectively definable material 210 on the substrate 110. Collectively, insulative material 250, the optional etch-stop material 260, expendable material 212 and selectively definable material 210 may be referred to as "masking materials." While the materials are illustrated on the substrate 110 in the form of layers, the materials may also be formed in other configurations. The masking materials described herein may be formed by any suitable deposition technique including, but not limited to, spin coating, blanket coating, chemical vapor deposition ("CVD"), atomic layer deposition ("ALD"), plasma-enhanced ALD, or physical vapor deposition ("PVD"). Depending on the specific material to be used, the technique for forming the masking materials may be selected by a person of ordinary skill in the art.

By way of nonlimiting example, the substrate 110 is formed from silicon, such as a silicon semiconductor substrate. Insulative material 250 may be deposited on the substrate 110. The insulative material 250 may be a silicon oxide, such as tetraethylorthosilicate ("TEOS"), silicon dioxide ("SiO_2"), or a high density plasma ("HDP") oxide. The insulative

material 250 may be thermally grown on the substrate 110. By way of non-limiting example, the insulative material 250 may have a thickness within a range of from approximately 25 Å to approximately 75 Å. In one embodiment, the insulative material 250 is SiO_2 and is thermally grown on the substrate 110.

The etch-stop material 260, if present, may be deposited on the insulative material 250. The etch-stop material 260 may function as an effective etch stop during chemical mechanical planarization ("CMP") of overlying materials. The etch-stop material 260 may be a nitride material. In one embodiment, the etch-stop material 260 is a nitride including, but not limited to, silicon nitride ("Si_3N_4").

The expendable material 212 may be formed from a patternable material that is selectively etchable relative to the substrate 110 and to other exposed underlying materials of the semiconductor structure 200. The material of the expendable material 212 may be a carbon-containing material, a dielectric antireflective coating ("DARC"), or a bottom antireflective coating ("BARC") material. By way of non-limiting example, the expendable material 212 may be amorphous carbon, transparent carbon, tetraethylorthosilicate ("TEOS"), silicon nitride ("Si_3N_4"), silicon carbide ("SiC"), silicon or a dielectric antireflective coating (DARC), such as a silicon-rich oxynitride ("SiO_3N_4"), silicon oxide (SiO_2), or combinations thereof. By way of non-limiting example, the expendable material 212 may be deposited at a thickness within a range of from approximately 800 Å to approximately 2500 Å, such as at approximately 2000 Å. The materials overlying the substrate 110 may be selected based upon consideration of the chemistry and process conditions for the various pattern forming and pattern transferring steps discussed herein. Because the materials between the expendable material 212 and the substrate 110 function to transfer a pattern derived from the expendable material 212 to the substrate 110, these materials are selected so that they may be selectively etched relative to other exposed materials. As used herein, a material is "selectively etchable" when the material exhibits an etch rate of at least approximately two times greater than that of the other material exposed to the same etch chemistry. Ideally, such a material has an etch rate of at least approximately ten times greater than that of another material exposed to the same etch chemistry. As such, it will be understood that the expendable material 212, insulative material 250 and etch-stop material 260 may be any combination of materials that enable selective removal as described herein.

The selectively definable material 210 may be definable by a lithographic process, e.g., formed of a photoresist material, including any photoresist material known in the art. Since photoresist materials and photolithographic techniques are well known in the art, selecting,

depositing, patterning, and developing the photoresist material to produce a desired pattern are not discussed in detail herein.

FIG. 4 shows an embodiment of the semiconductor structure 200 having a patterned, selectively definable material 210 thereon. The pattern in the selectively definable material 210 may include spaces and lines having substantially equal widths. The spaces may correspond to removed portions of the selectively definable material 210 while the lines correspond to remaining portions of the selectively definable material 210. The width of the lines may be a minimum feature size ("F") printable by the photolithography technique used to form the pattern. Alternatively, the spaces and lines may be printed at a feature size greater than F. By way of non-limiting example, F may range from approximately 40 nm to approximately 70 nm, such as approximately 44 nm. While FIG. 4 illustrates a 1F weave pattern, it will be appreciated that other layouts may be used.

The pitch between adjacent lines in FIG. 4 is equal to the sum of the width of the line of selectively definable material 210 and the width of the neighboring space. To minimize the critical dimensions of features formed using this pattern of lines and spaces, the pitch may be at or near the limits of the photolithographic technique used to pattern the selectively definable material 210. For example, the pitch of the lines may be between about 80 nm and about 140 nm. Thus, the pitch may be at the minimum pitch of the photolithographic technique and the spacer pattern discussed below may advantageously have a pitch below the minimum pitch of the photolithographic technique. Alternatively, because the margin of error for position and feature size typically increases as the limits of a photolithographic technique are approached, the lines may be formed having larger feature sizes to minimize errors in the positions and sizes of the lines and may be subsequently trimmed to a smaller size.

Referring to FIG. 5A, the pattern in the selectively definable material 210 may be transferred into the expendable material 212 forming an expendable structure 264 over etch-stop material 260, if present. After transferring the pattern to the expendable material 212, the selectively definable material 210 may be removed by conventional techniques. In one embodiment, the expendable structure 264 may be an expendable line. The pattern formed in the selectively definable material 210 may be etched into the expendable material 212 using a conventional etch process, such as a conventional dry etch process, a conventional wet etch process, or combinations thereof. By way of non-limiting example, a dry etch chemistry may be used to etch the expendable material 212, producing the expendable structure 264 having substantially vertical sidewalls 265. As used herein, the term "substantially vertical sidewalls" means and includes sidewalls having a slope angle of less than approximately 5° to the vertical. In one embodiment, the width of the expendable structures 264 may be F.

After removing the selectively definable material 210, the expendable structure 264 may be trimmed. In an embodiment of the invention, the expendable structure 264 may be trimmed from F to ½F. As shown in FIGs. 5B and 5C, the spaces 266 between each expendable structure 264 may be widened by etching the expendable structures 264, to form modified spaces 266a and modified structures 264a (FIG. 5C). The expendable structure 264 may be etched using an isotropic etch to "shrink" those features. Suitable etches include etches using an oxygen-containing plasma, e.g., a $SO_2/O_2/N_2/Ar$, $Cl_2/O_2/He$ or $HBr/O_2/N_2$ plasma. The extent of the etch may be selected so that the widths of the modified structures 264a are substantially equal to the desired spacing between later-formed, spacers 268, as will be appreciated from the discussion herein. For example, the width of the expendable structure 264 may be reduced from about 70 nm to about 35 nm. Advantageously, the width-reducing etch enables the modified structures 264a to be narrower than would otherwise be possible using the photolithographic technique used to pattern the selectively definable material 210. In addition, the etch may smooth the edges of the modified structures 264a, thus improving the uniformity of those lines.

Spacer material 214 may be formed over the exposed surfaces of the semiconductor structure 200, as shown in FIGs. 6A and 6B. The spacer material 214 may be conformally deposited over modified structure 264a by conventional techniques, such as by ALD. By conformally depositing the spacer material 214, the thickness of the spacer material 214 may remain substantially uniform regardless of the geometry or topography of underlying features, such as the modified structures 264a. The modified structures 264a may be selectively etchable relative to the spacer material 214. As an example only, spacer material 214 may be formed from polysilicon, silicon nitride Si_3N_4 or silicon oxide ("SiO_x").

Referring to FIG. 6C, the spacer material 214 may be anisotropically etched, removing the spacer material 214 from substantially horizontal surfaces while leaving the spacer material 214 on substantially vertical surfaces. As such, the substantially horizontal surfaces of the modified structure 264a and the substantially horizontal surfaces of the underlying portions of the semiconductor structure 200 may be exposed. If the spacer material 214 is formed from SiO_x, the anisotropic etch may be a plasma etch, such as a CF_4-containing plasma, a C_2F_6-containing plasma, a C_4F_8-containing plasma, a CHF_3-containing plasma, a CH_2F_2-containing plasma, or mixtures thereof. If the spacer material 214 is formed from silicon nitride, the anisotropic etch may be a $CHF_3/O_2/He$ plasma or a $C_4F_8/CO/Ar$ plasma. The spacers 268 produced by the etch may be present on substantially vertical sidewalls of the etched portions of the modified structures 264a. The

width of the spacers 268 may correspond to the desired width of features, such as trenches, ultimately to be formed on the semiconductor structure 200. In one embodiment, the width of the spacers 268 may be ½F. As discussed in further detail herein, first trenches 222 (shown in FIGs. 10A and 10B) having a sub-lithographic width may be formed in the substrate 110 between the area defined by spacers 286. As used herein "sub-lithographic" means less than about 70 nm, such as about 44 nm. In one embodiment, the first trenches 222 (shown in FIGs. 10A and 10B) have a width of approximately ½F.

The modified structure 264a may then be removed by conventional methods, leaving behind the spacers 268, as shown in FIGs. 7A and 7B. For instance, if an amorphous carbon is used as the expendable material 212 from which the modified structure 264a is formed, the amorphous carbon may be removed using an oxygen-based plasma, such as an O_2/Cl_2 plasma, an O_2/HBr plasma, or an $O_2/SO_2/N_2$ plasma.

Next, a dry etch chemistry may be used to transfer the pattern of the spacers 268 into the materials underlying the modified structure 264a. Alternatively, multiple dry etch chemistries may be used to separately etch each of the materials underlying the modified structures 264a. For example, a first etch may transfer the pattern of the spacers 268 into the underlying etch-stop material 260, if present, and a second etch may transfer the pattern of the spacers 268 into the substrate 110, as shown in FIG. 8, forming trenches therein. Etch chemistries suitable for etching these materials are known in the art and, therefore, are not described in detail herein.

As shown in FIG. 9, active areas 230 of the semiconductor structure 200 may be patterned with an active area mask that includes openings 221 to isolate active areas 230 with a relaxed pitch and feature size. The active area 230 is illustrated as extending in a substantially horizontal direction across the substrate 110 while the openings 221 of the active area mask 220 are illustrated as extending substantially perpendicular to the active area 230. The active area mask including the openings 221 may be thought to extend in a substantially vertical direction across the substrate 110. The active area mask 220 may be formed from carbon, such as amorphous carbon or transparent carbon. To reduce the dimensions of the openings 221 in the active area mask, sacrificial spacer material (not shown) may, optionally, be deposited on sidewalls of the openings 221 and trimmed to expose the active area mask 220 such that the active area mask 220 openings 221 are flanked by spacers. The pattern of openings 221 may be transferred to the substrate 110 to isolate the active areas 230. The pattern of openings 221 in the active area mask 220 may be transferred by conventional etching methods or by methods described herein. In an embodiment of the invention, a 70 nm pitch active area 230 may be formed on the semiconductor structure 200.

As shown in FIGs. 10A and 10B, the active area mask 220 may be removed and the substrate 110 may be etched in the location previously masked by the active area mask 220. If the active area mask 220 is flanked by spacers, the active area mask 220 may be removed and the remaining spacers may be used as a mask to etch the substrate 110. The substrate 110 may be etched by ion milling, reactive ion etching, or chemical etching. For instance, if the substrate 110 is formed from silicon, the substrate 110 may be anisotropically etched using HBr/Cl_2 or a fluorocarbon plasma etch. To etch a desired depth into the substrate 110 formed from silicon, the etch time may be controlled. For instance, the silicon may be exposed to the appropriate etch chemistry for an amount of time sufficient to achieve the desired depth in the silicon.

After etching, the spacers may be removed by conventional methods, such as wet or dry etching. By way of non-limiting example, if the spacers are formed from polysilicon, the spacers may be etched using a solution of tetramethylammonium hydroxide (TMAH). Alternatively, if the spacers are formed from a nitride, the spacers may be removed using a dry etch chemistry.

Referring to FIG. 10A, first trenches 222 are formed between active areas 230 which may be, for example, active silicon. As shown in FIG. 10B, a first fill material 226 may be blanket deposited over the semiconductor structure 200 and densified, as known in the art. The first fill material 226 may be a silicon dioxide-based material, such as a spin-on-dielectric ("SOD"), silicon dioxide, TEOS, or a high density plasma ("HDP") oxide. The first fill material 226 may be planarized, such as by chemical mechanical polishing ("CMP"), to remove portions of the first fill material 226 extending above silicon pillars 232 of the substrate 110.

The silicon pillars 232 in the active area 230 and first trenches 222 shown in FIGs. 10A and 10B have been pitch doubled in two directions. It will be appreciated that while the pitch is actually halved in the example above, this reduction in pitch is conventionally referred to as pitch "doubling." It will be further understood that embodiments of the invention include pitch doubling in only one direction, for example, either the width of the silicon pillar 232 or the width of the first trenches 222. In an embodiment of the invention, the width of the silicon pillar 232 and/or the width of the first trenches 222 may be sub-lithographic.

The semiconductor structure 200' of FIGs. 10A and 10B may be subjected to further processing. By way of non-limiting example, the semiconductor structure 200' may be subjected to an additional pitch doubling process to form trenches in gates of a memory array, as shown in FIGs. 11A-15. With reference to FIG. 11A, second expendable material 312 may be deposited over the active area 230 and patterned as described herein. The second expendable

material 312 may be patterned in a substantially parallel orientation relative to the first trenches 222. The second expendable material 312 may be deposited at F and trimmed to ½F. In an embodiment, the second expendable material 312 may be amorphous carbon and may be patterned using an anisotropic etch, such as an etch using a fluorocarbon plasma, although a wet (isotropic) etch may also be suitable if the second expendable material 312 is thin. Plasma etch chemistries may include, without limitation, CF_4, CFH_3, CF_2H_2, CF_3H.

A spacer material 314 may be deposited over the patterned second expendable material 312 and trimmed by conventional methods. The spacer material 314 may be deposited at ½F such that the second expendable material 312 and the spacer material 314 have a combined width of F. The spacer material 314 may be deposited by chemical vapor deposition or atomic layer deposition. The spacer material 314 may be any material capable of being selectively removed relative to the second expendable material 312 and later-formed sacrificial material 313. By way of non-limiting example, the spacer material 314 may include silicon nitrides and silicon oxides. In one embodiment, the spacer material 314 and the second expendable material 312 may be the same material. The spacer material 314 may be anisotropically etched to remove the spacer material 314 from horizontal surfaces of the second expendable material 312 and underlying substrate 110, as shown in FIG. 11B. Such an etch, also known as a spacer etch, may be performed using a fluorocarbon plasma.

Next, sacrificial material 313 may be deposited over the second expendable material 312 and spacer material 314. The sacrificial material 313 may be planarized to expose the second expendable material 312 and spacer material 314, as shown in FIGs. 12A, 12B. The sacrificial material 313 may include the same material as the second expendable material 312, or may be any material that is selectively etched compared to the spacer material 314.

As shown in FIG. 13, the spacer material 314 may be selectively etched relative to the second expendable material 312 and the sacrificial material 313 to create a gap 334. The remaining expendable material 312 and sacrificial material 313 may function as a mask during etching of the underlying substrate 110 to form the second trenches 322 in the location of gap 334, as shown in FIG. 14A. The second trenches 322 may have a width of 1/2F. Due to the spacing of the second expendable material 312 and sacrificial material 313, the second trenches 322 may be positioned asymmetrically on the substrate 110. The substrate 110 may be etched by ion milling, reactive ion etching, or chemical etching. For instance, if the substrate is formed from silicon, the substrate may be anisotropically etched using HBr/Cl_2 or a fluorocarbon plasma etch. To etch a desired depth into the substrate formed from silicon, the

etch time may be controlled. For instance, the silicon may be exposed to the appropriate etch chemistry for an amount of time sufficient to achieve the desired depth in the silicon.

In embodiments of the invention, the second trenches 322 may be recessed access device or "RAD" trenches. As used herein, "RAD trenches" means and includes an opening in a substrate in which a RAD transistor is ultimately formed. One example of a RAD transistor includes a transistor gate (wordline) which is partially formed within a trench in a semiconductor substrate.

After etching, the second expendable material 312 and the sacrificial material 313 may be removed by conventional methods. The pattern remaining after the second expendable material 312 and the sacrificial material 313 are removed may include silicon pillars 332 (also referred to as "pedestals" or "fins") of the active area 230 and the second trenches 322 (gate trenches) with array active area patterns, as shown in FIG. 14B. Thus, pitch doubling has occurred for the second trenches 322 in the gates. In an embodiment of the present invention, the second trenches 322 have a sub-lithographic width.

It will be understood that the second expendable material 312, spacer material 314 and sacrificial material 313, may be selected such that the spacer material 314 may be selectively removable relative to the second expendable material 312 and sacrificial material 313. Thus, in an embodiment, the second expendable material 312 and sacrificial material 313 may be the same material. Each of the second expendable material 312, sacrificial material 313 and spacer material 314 may be selected from amorphous or transparent carbon, polysilicon, silicon dioxide and silicon nitride such that the spacer material 314 may be selectively removable relative to the second expendable material 312 and sacrificial material 313. The material for the second expendable material 312 and sacrificial material 313 may be selected to withstand the subsequent trench etch chemistry.

Referring to FIG. 15, after forming the second trenches 322, a gate oxide material 370 may be grown by conventional methods. Next, various blanket transistor gate materials may be formed by conventional methods to form the semiconductor structure 200" of FIG. 15. The blanket transistor gate materials may be formed from materials of suitable work functions, such as doped polysilicon 372 or a metal, i.e., TiN, a conductor 374, for example tungsten, and a nitride capping material 376. The semiconductor structure 200" may be subjected to further conventional processing to produce transistors in the second trenches 322.

The semiconductor structure 200" of FIG. 15 may be subjected to further processing, as shown in FIG. 16. By way of non-limiting example, the semiconductor structure 200" may be subject to pitch doubling to form connections to the transistor gates via wordlines (i.e., conductive lines). A first expendable material 412 may be deposited over the semiconductor

structure 200". The first expendable material 412 may be patterned by conventional methods or methods described herein to expose the underlying second trenches 322.

Referring to FIG. 17, a first spacer material 414 may be deposited over the semiconductor structure 200". The first spacer material 414 may be planarized and trimmed by conventional methods. The thickness of the first spacer material 414 may define the critical dimension of the transistor gate. Referring to FIG. 18, a second expendable material 402 may be deposited over the semiconductor structure 200" and planarized to expose the first spacer material 414 and first expendable material 412. The second expendable material 402 may be trimmed to a desired width selected to leave an opening in similar width to the first spacer material 414. Next, a second spacer material 404 may be deposited over the semiconductor structure 200" and planarized to expose the first spacer material 414, first expendable material 412 and second expendable material 402, as shown in FIG. 18. The thickness of the second spacer material 404 may define the critical dimensions of the grounded gate. The first spacer material 414 and the second spacer material 404 may have a sub-lithographic width.

As shown in FIG. 19, the first expendable material 412 and second expendable material 402 may be selectively removed by conventional techniques. In an embodiment of the invention, the first expendable material 412 and second expendable material 402 are amorphous carbon and are removed by conventional methods, e.g., by using a SO_2-containing plasma. Then, the first spacer material 414 and second spacer material 404 may function as masks during a conventional etch to form conductive lines 425, as shown in FIG. 20. The conductive lines 425 may function as wordlines 425' and grounded gate 425". The gap between neighboring wordlines 425' is asymmetrical as compared to the gap between the underlying active areas. In an embodiment of the present invention, the conductive lines 425 have a sub-lithographic width.

Numerous advantages are achieved by utilizing the methods of embodiments of the invention to form the semiconductor structures 200', 200", 200"'. The methods described herein accommodate pitch doubling of $6F^2$ architecture at array gate patterning. The methods described herein accommodate the $6F^2$ architecture to be scaled significantly without scaling the lithography required. As such, sub-lithographic features may be formed independent of photolithography and etch trim capabilities. Further, the methods of embodiments of the invention provide for pitch doubling of asymmetric features on non-equal line space. It will be understood that the methods described herein may also be used during other fabrication processes, for example, to define the linear self-aligned contact features, such as capacitors, digit lines or other sub-lithographic features. The semiconductor structures 200', 200", 200"' may be subjected to conventional processing acts to produce the memory array 100 shown in

FIG. 2. Since the additional processing acts to form the memory array 100 are conventional, these acts are not described in detail herein.

The invention is susceptible to various modifications and alternative forms in addition to specific embodiments shown by way of example in the drawings and described in detail herein. Thus, the invention is not limited to the particular forms disclosed. Rather, the scope of the invention encompasses all modifications and alternatives falling within the following appended claims and their legal equivalents.

CLAIMS:

1. A semiconductor structure comprising:
a plurality of silicon pillars in a substrate; and
a plurality of trenches isolating each silicon pillar of the plurality of silicon pillars, wherein at least one of the plurality of trenches or the plurality of silicon pillars has a width of less than 44 nm.

2. The semiconductor structure of claim 1, wherein the width of the each pillar of the plurality of silicon pillars and the width of each trench of the plurality of trenches is less than 44 nm.

3. A semiconductor structure comprising a plurality of active areas separated by isolation regions, the plurality of active areas including recessed access device trenches therein respectively having a width of less than a minimum feature size.

4. The semiconductor structure of claim 3, wherein the width of the isolation regions is less than the minimum feature size.

5. The semiconductor structure of claim 3, wherein the width of the plurality of active areas is less than the minimum feature size.

6. The semiconductor structure of claim 3, further comprising conductive gate material within the recessed access device trenches and a plurality of conductive lines elevationally outward of the plurality of active areas and recessed access device trenches, some of the conductive lines connecting with the conductive gate material within the recessed access device trenches.

7. The semiconductor structure of claim 1, wherein the trenches comprise insulative material therein.

8. The semiconductor structure of claim 7, wherein the insulative material fills the trenches.

9. The semiconductor structure of claim 2, wherein the width of the each pillar of the plurality of silicon pillars and the width of each trench of the plurality of trenches are equal.

10. The semiconductor structure of claim 6, wherein the conductive lines have widths of less than the minimum feature size.

11. The semiconductor structure of claim 6, wherein the conductive lines run parallel the recessed access device trenches.

12. The semiconductor structure of claim 6, wherein another some of the conductive lines do not connect with the conductive gate material within the recessed access device trenches.

13. The semiconductor structure of claim 12, wherein the another some of the conductive lines have widths of less than the minimum feature size.

14. The semiconductor structure of claim 12, wherein the another some of the conductive lines comprise grounded gate lines.

15. The semiconductor structure of claim 14, wherein the grounded gate lines have widths of less than the minimum feature size.

16. The semiconductor structure of claim 6, wherein the some gate lines comprise word lines, and further comprising another some of the conductive lines which comprise grounded gate lines, two of the word lines being received between two immediately adjacent of the grounded gate lines.

17. The semiconductor structure of claim 16, wherein the grounded gate lines have widths of less than the minimum feature size.

18. The semiconductor structure of claim 16, wherein the word lines have widths of less than the minimum feature size.

19. The semiconductor structure of claim 16, wherein the word lines have widths of less than the minimum feature size and the grounded gate lines have widths of less than the minimum feature size.