REMOVAL OF SUBSTRATE PERIMETER MATERIAL

Background of the Invention

Field of the Invention

The present invention relates to a technique for removing material from the perimeter of a substrate.

Description of the Prior Art

In the production of semiconductor devices, it is frequently desirable to grow an epitaxial layer of material on a single-crystal semiconductor substrate. For example, silicon, germanium, or III-V semiconductor materials are epitaxially grown on silicon wafers. It is known to form a "cap" of material on the back-side of a wafer prior to the epitaxial growth on the front side of the wafer, in order to prevent autodoping. That is, the cap, typically of silicon dioxide, silicon nitride, or both, prevents dopants in the wafer from out-diffusing from the back side of the wafer and inadvertently doping the epitaxial material on the front side. One method of forming a silicon dioxide/silicon nitride cap on a wafer is disclosed in U. S. patent 4,687,682 coassigned with the present invention, with other techniques also known in the art. To a large extent, the cap also prevents the silicon (or other epitaxially deposited semiconductor material) from forming on the back side of the wafer.

However, pinholes in the cap material have been found to allow small nodules of silicon to deposit on the back side of the wafer. These nodules remain as irregularities on the surface of the wafer even after the cap material is removed. The pinholes tend to form inherently in many types of dielectric deposition or growth processes. In addition, they are often formed more frequently near the edge of a wafer due to contact by handling apparatus (e.g., tweezers, vacuum pick-up mechanisms, etc.) Furthermore, the pinholes may form more frequently near the edge of a wafer due to a higher concentration of silicon in the epitaxial growth atmosphere, which tends to deplete near the center of the wafer as it sits on the susceptor of the epitaxial deposition chamber. The nodules are especially troublesome around the perimeter of the back side of the wafer, where they can distort the planarity of the wafer when it is clamped in a subsequent process step. For example, lithography operations can be impaired due to lack of planarity caused by the nodules formed around the perimeter of the back side of a wafer.

To prevent the formation of nodules around the perimeter of a wafer, it is known in the art to remove a strip of the cap material around the perimeter of wafer. This allows the subsequent epitaxial deposition process to occur on this strip on the back side (as well as on the front side) of the wafer. Since the epitaxially-

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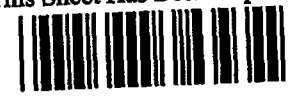
deposited material forms a relatively smooth, uniform surface, the wafer can be clamped around its periphery in subsequent lithographic operations without distorting its planarity. However, the prior art techniques for removing the perimeter strip of cap material have not been as rapid or uniform as could be desired. For example, a mask may be applied to the back side that covers the central portion of the wafer, while leaving a perimeter strip exposed. An etching operation can then remove the desired strip of cap material. However, this is a relatively slow process, requiring both a masking and etching operation for each wafer. Another possibility is to insert the wafer edge-wise into a liquid bath of hydrofluoric acid (HF), and roll the wafer until all of the perimeter cap material is etched off by the acid. However, this may not yield as smooth a strip of removed material as is desired, and also may require significant time and operator attention per wafer. Therefore, it is desirable to remove a strip of material from the perimeter of a wafer in a more uniform and/or more cost-effective manner.

Furthermore, a recent trend in the semiconductor art has been to polish the contoured edges of a semiconductor wafer to obtain a rounded and smooth edge. This is desirable to prevent the wafer from abrading the cassettes in which it is stored, or the processing equipment. Such abrasion can produce undesirable microscopic particles that impair the yield of integrated circuits formed on the wafers, especially those formed with sub-micron processing techniques. Prior-art techniques for smoothing the edge of a wafer include polishing with a wheel and polishing slurry, accomplished one wafer at a time. This yields a very smooth edge, but is very time consuming. Alternatively, it is known to roll a batch (e.g., 25) of wafers in liquid polishing acids to smooth the edge, followed by a clean and rinse operation.

Summary of the Invention

We have invented a method of removing material from the perimeter of a substrate. A surface of a first substrate is placed in contact with a surface of a second substrate having comparable size, and exposed to a gaseous etching atmosphere. The exposure continues for a duration sufficient to remove a strip of the material from at least the first substrate. In a typical embodiment, a plurality of semiconductor wafers are stacked, and exposed to a plasma etching atmosphere, in order to remove a perimeter strip of a dielectric cap prior to performing an epitaxial deposition operation.

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Brief Description of the Drawings

Fig. 1 illustrates a side view of a plurality of wafers stacked in an exemplary fixture.

Fig. 2 illustrates a top view of the cover plate of the exemplary fixture.

Fig. 3 illustrates a typical wafer boat loaded with wafers stacked back-to-back during the formation of a cap on the back side of the wafers.

Fig. 4 illustrates a typical wafer having a perimeter strip removed.

Fig. 5 illustrates a rough edge of a wafer formed by prior art techniques.

Fig. 6 illustrates a relatively smoother edge of a wafer formed by the present technique.

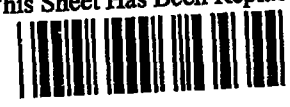
Detailed Description

The present detailed description relates to a method of removing material from the perimeter of a substrate, for use in a variety of applications. An exemplary case of removing a perimeter strip of a dielectric cap from a semiconductor wafer is shown. This operation also serves to smooth the edge contour of the wafer. However, the smoothing operation may be practiced independently of any cap removal, if desired, as further discussed below.

In an exemplary embodiment shown in Fig. 1, a stack of silicon wafers comprises a top wafer 10, a bottom wafer 12, and an intermediate wafer 11. The stack is placed in a holding device comprising a bottom platform 14 that is tilted at an angle θ, which is illustratively about 15 degrees. The tilt allows the wafers to slide into contact with retaining pins 15 and 16 (as shown in Fig. 2). The bottom plate and retaining pins are typically quartz, with other materials being possible. A top plate 13, typically quartz, is placed over the stack to provide sufficient weight to flatten out the warpage in the wafers. A top view of the stack is shown in Fig. 2, as viewed perpendicularly to the top plate 13. If desired, the flats 21 that are typically formed in silicon wafers may also be formed in the top plate. The stack is placed in a suitable etching apparatus, typically a barrel reactor, to remove a perimeter strip of dielectric cap material, as discussed further below.

The dielectric cap material typically comprises silicon dioxide and silicon nitride, as noted above. This dielectric cap material is usually formed on only one side of a wafer, as may be accomplished by loading wafers back-to-back on a furnace boat 30, as shown in Fig. 3. This prior-art technique allows for the growth and/or deposition of cap material on the exterior surfaces (33, 34) of a given pair of wafers (31, 32), while preventing cap material from forming on the contacting inner surfaces of the pair. In practicing the present invention, it is convenient to stack an entire furnace boat load of wafers, typically about 50 wafers, in the configuration shown in Fig. 1. Furthermore, it is convenient, although not necessary, to maintain

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the same back-to-back orientation of the wafers in each pair. Therefore, upon being stacked, the outer (capped) surface 34 of wafer 32 will contact the outer (capped) surface 37 of wafer 35, whereas the inner (uncapped) surfaces of wafer pairs 31-31 and 35-36 will remain in contact as shown. However, if desired, the wafers may be oriented in the stack of Fig. 1 so that the capped side of each wafer contacts the uncapped side of the adjacent wafer.

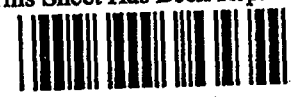
After the etching operation, the back side of a wafer (40) appears as shown in Fig. 4. The dielectric cap (41) remains on the central portion of the back side wafer surface, while the perimeter strip (42) is clear of the cap. In present-day commercial practice with silicon wafers, the width of the removed perimeter strip is at least 1 millimeter, but typically less than 10 millimeters. However, a wider range is possible. A comparable strip of silicon is also typically removed from the front side of the wafer (not shown) in most etching operations. However, the bare silicon front side surface is typically polished in a subsequent operation, according to principles known in the art. That polishing operation typically smooths out the front side to negate any artifacts of the perimeter strip that was removed from the front side. For example, one technique for polishing a wafer to obtain a smooth, flat surface is disclosed in U. S. patent 4,874,463, coassigned with the present invention. If that process is used, the perimeter strip may be removed according to the present invention after the isotropic etching operation disclosed in that patent.

The above principles will be more fully illustrated by means of the following Example.

EXAMPLE

The test wafers used in this Example were silicon wafers 150 millimeters (6 inches) in diameter. They each had a back side cap of SiO_2 25 nanometers (250 angstroms) thick that was covered by a layer of SiN that was 50 nanometers (500 angstroms) thick. A stack of 40 test wafers was placed in the apparatus shown in Fig. 1. A cover plate, consisting of 10 blank wafers, was placed on top of the stack, to provide a weight of about 0.5 kilograms. The stack was loaded into a barrel etcher (Branson model PM 11020 with a 3000C controller), and the etching chamber was evacuated to a pressure of 50 mtorr. The pressure was then increased to 1 torr while introducing CF_4 gas at a flow rate of 620 cubic centimeters per minute. The plasma was produced in this gas at a power level of 700 watts. An etching time of 10 minutes was sufficient to remove a perimeter strip of the oxide/nitride cap about 3 millimeters wide, after which the etching operation was terminated.

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The removed perimeter strip was quite uniform, having a more even shape than those typically resulting from prior-art removal processes. Furthermore, the perimeter strip is very concentric with the center of the wafer. It appears that these beneficial effects are due to the surprisingly uniform diffusion of the etchant gas between the contacting wafer surfaces. Such diffusion increases with time, so that a strip of greater width may be obtained from longer diffusion times. A large number of wafers may conveniently be treated at one time in a batch operation, for increased economies as compared to techniques that treat individual wafers, especially those that require masking steps for each wafer. However, the present invention may be practiced on only one wafer at a time, if desired. For example, a wafer having a cap layer may be placed in contact with a blank, such as a quartz disk having a diameter equal to, or greater than, that of the capped wafer. A force sufficient to ensure good contact between the wafer and the blank, and reduce warpage effects of the wafer, should desirably be applied. For semiconductor wafers having a diameter in the range of from 150 to 200 millimeters (6 to 8 inches), we recommend a force of at least 1 Newton (0.2 pounds) applied uniformly over the surface of the wafer. This force may conveniently be obtained by the weight of the blank disc as noted above, or by other means. The etching operation will then proceed as before to remove the perimeter strip of the cap on the wafer.

Subsequent to the removal of the perimeter strip of the dielectric cap, an epitaxial deposition process may be accomplished according to methods known in the semiconductor art. The epitaxial deposition on the bare (uncapped) front side of the wafer will typically also produce a smooth epitaxial deposit on the perimeter strip on the back side of the wafer. Therefore, subsequent lithographic operations that require clamping the wafer in a lithographic apparatus (e.g., optical or x-ray stepper, or electron beam device) may proceed without distortion of the planarity of the wafer, as could result from the uncontrolled presence of silicon nodules on the periphery of the wafer.

In addition to removing the perimeter strip of dielectric cap material, the exposure to the etching atmospheres also smooths out the contour of the edge of the wafer. For example, referring to Fig. 5, an edge 51 of a wafer 50 produced by prior-art edge grinding techniques has numerous sharp angles. (The scale of this rough edge surface is greatly enlarged for clarity.) This rough edge tends to abrade handling and storage equipment, as well as production equipment, in which the wafer is placed, creating problems as noted above. In contrast, the present invention produces a much smoother edge, as shown in Fig. 6, wherein the noted abrasion problems are reduced. In most cases, this edge smoothing is a consequential result

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of the perimeter strip removal, and requires no extra operations. However, the present invention may be practiced on wafers for the purpose of edge smoothing only, even where no cap material is to be removed. All such applications are considered to be removal of perimeter material, as used herein.

While the exemplary embodiment has been given in terms of silicon wafers used in the production of semiconductor devices (e.g., integrated circuits), still other applications of the present invention are possible. For example, removal of dielectric, conductive, magnetic, optical, adhesive, or other material may be accomplished by the inventive technique from optical, magnetic, or other types of substrates. While the substrates are often disc-shape, other shapes are possible, including rectangular, for example. Furthermore, while the etching atmosphere is typically a plasma, the use of a non-plasma (e.g., HF gas) is possible, depending upon the nature of the material to be removed.

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Claims:

1. A method of removing a layer of material from the perimeter (42) of a first substrate having a broad surface of a given size,

Characterized in that said removing is accomplished by steps comprising:

placing said broad surface of said first substrate (31) in contact with the broad surface of a second substrate (32) of said given size, and exposing the first and second substrates to a gaseous etching atmosphere until the desired layer of material is removed from said perimeter (42).

2. The method of claim 1 wherein said first substrate is a semiconductor wafer.

3. The method of claim 2 wherein said layer of material that is removed is a strip of dielectric material formed on said broad surface of said semiconductor wafer.

4. The method of claim 2 wherein said layer of material that is removed is semiconductor material from the edge of said semiconductor wafer, whereby the edge is smoothed.

5. A method of making a semiconductor wafer by steps comprising:

forming a cap layer of dielectric material (41) on the back side of a first semiconductor wafer,

removing a perimeter strip (42) of said dielectric material from said back side of said first wafer,

and thereafter epitaxially forming a semiconductor layer on the front side, and on the perimeter strip on said back side, of said first wafer,

Characterized in that said removing is accomplished by steps comprising:

placing said back side of said first wafer (31) in contact with a given side of a second wafer, (32) and

exposing said first and second wafers to an etching atmosphere until the desired layer of material is removed from said perimeter strip.

6. The method of claim 5 wherein a cap layer of dielectric material is also formed on the back side of said second wafer prior to said removing, and

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wherein a perimeter strip of said dielectric material is also removed from said back side of said second wafer, and wherein a semiconductor layer is also epitaxially formed on the front side, and on the perimeter strip on said back side, of said second wafer.

7. The method of claim 5 further comprising the step of clamping said wafer in a lithographic apparatus and performing a lithographic operation on said wafer to define features of an integrated circuit.

8. A method of making an integrated circuit by steps comprising clamping a first semiconductor wafer in a lithographic device and performing a lithographic operation to define features on a front side of the wafer having an epitaxial layer formed thereon; and with said first wafer having a dielectric cap layer (41) formed on the back side, from which a perimeter strip (42) has been removed,

CHARACTERIZED IN THAT the removing of said perimeter strip is accomplished by steps comprising:

placing said back side of said first wafer (31) in contact with a given side of a second wafer (32), and

exposing said first and second wafers to an etching atmosphere until the desired layer of material is removed from said perimeter strip.

9. The method of claim 5,6, or 8, wherein said second wafer has an epitaxial layer formed on the front side, and a cap layer of dielectric material formed on the back side.

10. The method of claim 5,6,8 or 9, wherein said back side of said second wafer is the given side that is placed in contact with said first wafer, and/or the front side of said second wafer is the given side that is placed in contact with said first wafer.

11. The method of claim 5 or 9, wherein said semiconductor wafer is a silicon wafer, and/or said semiconductor layer that is epitaxially formed is a silicon layer.

12. The method of claim 6 or 11, wherein said cap layer of dielectric material comprises at least one dielectric selected from silicon dioxide and silicon nitride, and/or said perimeter strip has a width in the range of from 1 to 10 millimeters.