9904983-5

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INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 6 : G06F 9/00 — A2

(11) International Publication Number: WO 98/48346

(43) International Publication Date: 29 October 1998 (29.10.98)

(21) International Application Number: PCT/US98/07708

(22) International Filing Date: 16 April 1998 (16.04.98)

(30) Priority Data:
08/843,996 18 April 1997 (18.04.97) US

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(81) Designated States: AL, AM, AT, AT (Utility model), AU (Petty patent), AZ, BA, BB, BG, BR, BY, CA, CH, CN, CU, CZ, CZ (Utility model), DE, DE (Utility model), DK, DK (Utility model), EE, EE (Utility model), ES, FI, FI (Utility model), GB, GE, GH, GM, GW, HU, ID, IL, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SK (Utility model), SL, TJ, TM, TR, TT, UA, UG, UZ, VN, YU, ZW, ARIPO patent (GH, GM, KE, LS, MW, SD, SZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, ML, MR, NE, SN, TD, TG).

Published
Without international search report and to be republished upon receipt of that report.

1 appl'n.
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(54) Title: EMULATION OF INTERRUPT CONTROL MECHANISM IN A MULTIPROCESSOR SYSTEM

(57) Abstract

A multiprocessor computer system that includes an emulation feature for lowest priority processor software compatibility while providing fault tolerance includes first and second processors coupled to a system bus that handles transmission of interruption messages within the system. An instruction resulting in an interruption which specifies an interrupt feature causes microcode to generate a trap. A trap handling routine reads ID information from a register of the first processor, and places it in a target processor ID field of an interruption message which gets broadcast on the system bus. The first processor eventually accepts the interruption message and is designated as the processor in the system which handles the interruption.

