CLAIMS

WHAT IS CLAIMED:

1. A method of forming a semiconductor device structure, comprising:

providing a first PMOS active region and a second PMOS active region in a semiconductor substrate;

forming a first masking pattern over said first PMOS active region;

forming a silicon germanium layer over said second PMOS active region in accordance with said first masking pattern;

removing said first masking pattern; and

forming gate electrode structures over said first and second PMOS active regions.

2. The method of claim 1, further comprising performing one or more implantation processes for implanting dopants into said first PMOS active region, wherein said dopants implanted into said first PMOS active region only consist of group 3 elements.

3. The method of claim 2, wherein boron is the only dopant implanted into said first PMOS active region.

4. The method of claim 1, further comprising performing one or more implantation processes for implanting dopants into said first PMOS active region, wherein said dopants are implanted along a direction substantially normal to an exposed surface of said first PMOS active region.

5. The method of claim 1, further comprising:

forming a second masking pattern over said first PMOS active region subsequently to said formation of gate electrode structures;

performing a first implantation process with a first halo implant dose for forming halo regions in said second PMOS active region; and

removing said second masking pattern.

6. The method of claim 5, further comprising:

forming a third masking pattern over said second PMOS active region; and

performing a second implantation process with a second halo implant dose for forming lightly doped halo regions in said first PMOS active region, said second halo implant dose being substantially smaller than said first halo implant dose.

7. The method of claim 6, wherein said second halo implant dose is substantially less than 3.3E13 atoms/cm^2.

8. A method of forming a semiconductor device structure, comprising:

providing a semiconductor substrate with a first PMOS active region and a second PMOS active region, of which only said second active region has a silicon germanium layer formed thereon;

forming a first PMOS device on said first PMOS active region, said first PMOS device comprising a first gate electrode structure;

forming a second PMOS device over said second PMOS active region, said second PMOS device comprising a second gate electrode structure formed on said silicon germanium layer; and

performing a first implantation process for forming halo regions in said second PMOS active region at opposing sides of said second gate electrode structure while said first PMOS active region is protected by a masking pattern from being exposed to said first implantation process.

9. The method of claim 8, further comprising performing a second implantation process for forming halo regions in said first PMOS active region subsequent to said first implantation process, wherein an implantation dose of said second implantation process is substantially smaller than an implantation dose of said first implantation process.

10. The method of claim 8, further comprising performing one or more doping implantation processes into said first PMOS active region, wherein said first PMOS active region is only subjected to doping implantation processes implanting group 3 elements.

11. The method of claim 10, wherein said one or more doping implantation processes are substantially normal to an exposed surface of said first PMOS active region.

12. A semiconductor device structure, comprising:

a semiconductor substrate with a first PMOS active region and a second PMOS active region, of which only said second PMOS active region has a silicon germanium layer formed thereon;

a first PMOS device formed on said first PMOS active region, said first PMOS device having a first gate electrode structure; and

a second PMOS device formed over said second PMOS active region, said second PMOS device having a second gate electrode structure disposed on said silicon germanium layer.

13. The semiconductor device structure of claim 12, wherein, out of said first and second PMOS active regions, halo regions are only formed in said second PMOS active region.

14. The semiconductor device structure of claim 13, wherein said first PMOS device is of an HVT type and said second PMOS device is of one of an LVT type and an RVT type.

15. The semiconductor device structure of claim 12, wherein said first PMOS active region has first halo regions with a first dopant concentration formed therein and said second PMOS active region has second halo regions with a second dopant concentration formed therein, said first dopant concentration being substantially smaller than said second dopant concentration.

16. The semiconductor device structure of claim 15, wherein a ratio of said second dopant concentration to said first dopant concentration is at least about 2.

17. The semiconductor device structure of claim 15, wherein said first PMOS device is of an SHVT type and said second PMOS device is of one of an RVT type and an LVT type.

18. The semiconductor device structure of claim 12, wherein said first PMOS device represents one of an HVT and an SHVT type device and said second PMOS device represents one of an LVT and an RVT type device.

19. The semiconductor device structure of claim 12, wherein said first PMOS active region has dopants implanted therein which are only provided by group 3 elements.

20. The semiconductor device structure of claim 19, wherein said dopants implanted into said first PMOS active region is provided by boron.

What is claimed:

1. A method of forming a semiconductor device structure, comprising: providing a first PMOS active region and a second PMOS active region in a semiconductor substrate; forming a first masking pattern over said first PMOS active region; forming a silicon germanium layer over said second PMOS active region in accordance with said first masking pattern; removing said first masking pattern; forming gate electrode structures over said first and second PMOS active regions; forming a second masking pattern over said first PMOS active region subsequently to said formation of gate electrode structures; performing a first implantation process in the presence of said second masking pattern with a first halo implant dose for forming halo regions in said second PMOS active region; removing said second masking pattern; forming a third masking pattern over said second PMOS active region; and performing a second implantation process in the presence of said third masking pattern with a second halo implant dose for forming lightly doped halo regions in said first PMOS active region, said second halo implant dose being substantially smaller than said first halo implant dose.

2. The method of claim 1, further comprising performing one or more implantation processes for implanting dopants into said first PMOS active region, wherein said dopants are implanted along a direction substantially normal to an exposed surface of said first PMOS active region.

3. The method of claim 1, wherein said second halo implant dose is substantially less than 3.3E13 atoms/cm^2.

4. A method of forming a semiconductor device structure, comprising: providing a semiconductor substrate with a first PMOS active region and a second PMOS active region, of which only said second active region has a silicon germanium layer formed thereon; forming a first PMOS device on said first PMOS active region, said first PMOS device comprising a first gate electrode structure; forming a second PMOS device over said second PMOS active region, said second PMOS device comprising a second gate electrode structure formed on said silicon germanium layer; performing a first implantation process for forming halo regions in said second PMOS active region at opposing sides of said second gate electrode structure while said first PMOS active region is protected by a first masking pattern from being exposed

to said first implantation process; and performing a second implantation process for forming halo regions in said first PMOS active region subsequent to said first implantation process while said second PMOS region is protected by a second masking pattern, wherein an implantation dose of said second implantation process is substantially smaller than an implantation dose of said first implantation process.

5. The method of claim 4, further comprising performing one or more doping implantation processes into said first PMOS active region, wherein said one or more doping implantation processes are substantially normal to an exposed surface of said first PMOS active region.

6. A semiconductor device formed in accordance with the method of any one of the preceding claims.