

**MEMORY MODULE AND METHOD HAVING ON-BOARD DATA
SEARCH CAPABILITIES AND PROCESSOR-BASED SYSTEM USING
SUCH MEMORY MODULES**

TECHNICAL FIELD

[001] The present invention relates to a memory devices, and more particularly, to memory modules containing memory devices and having the capability within the memory modules to search data stored in the memory devices.

BACKGROUND OF THE INVENTION

[002] Processor-based systems, such as computer systems, use memory devices, such as dynamic random access memory ("DRAM") devices, to store instructions and data that are accessed by a processor. These memory devices are typically used as system memory in a computer system. In a typical computer system, the processor communicates with the system memory through a memory controller. The processor issues a memory request, which includes a memory command, such as a read command, and an address designating the location from which data or instructions are to be read. The memory controller uses the command and address to generate appropriate command signals as well as row and column addresses, which are applied to the system memory. In response to the commands and addresses, data are transferred between the system memory and the processor. The memory controller is often part of a system controller, which also includes bus bridge circuitry for coupling the processor bus to an expansion bus, such as a PCI bus.

[003] Although the operating speed of memory devices has continuously increased, this increase in operating speed has not kept pace with increases in the operating speed of processors. The increase in operating speed of memory controllers has also lagged behind the rapid increases in the operating speed of processors. The relatively slow speed of memory controllers and memory devices often limits the speed at which computer systems can function.

[004] The operating speed of computer systems is also limited by latency problems that increase the time required to read data from system memory devices. More specifically, when a memory device read command is coupled to a system memory device, such as a synchronous DRAM ("SDRAM") device, the read data are output

from the SDRAM device only after a delay of several clock periods. Therefore, although SDRAM devices can synchronously output burst data at a high data rate, the delay in initially providing the data can significantly slow the operating speed of a computer system using such SDRAM devices.

[005] The adverse affect of the above-described problems on the operation of processor-based systems using such memory devices depends to a large extent on the nature of the operations being performed by the system. For operations that are highly memory intensive, *i.e.*, frequent read and write operations, the above-described problems can be very detrimental to the operating speed of processor-based systems. For example, the speed at which a processor-based system, such as a computer system, can perform a “data mining” operation is largely a function of the speed at which a processor can access data, which is typically stored in system memory during such operations. In a data mining operation, the processor looks for specific data content, such as a specific number or word, stored in system memory. The processor performs this function by repetitively fetching items of data, and then comparing each fetched data item to the data content that is the subject of the search. Each time a data item is fetched, the processor must output a read memory command and a memory address, both of which must be coupled to the system memory. The processor must then wait until system memory device has output the read data and coupled the read data to the processor. As a result of the significant latency of system memory devices, which are typically dynamic random access (“DRAM”) devices, it can take several clock cycles for the system memory to respond to the read memory command and address and output the read data item to the processor. When a large amount of data must be searched, data mining can require a considerable period of time.

[006] One approach to increasing the operating speed of memory devices to provide faster memory intensive operations like data mining is to use multiple memory devices coupled to the processor through a memory hub. In a memory hub architecture, a system controller or memory hub controller is coupled to several memory modules, each of which includes a memory hub coupled to several memory devices. The memory hub efficiently routes memory requests and responses between the controller and the memory devices. Computer systems employing this architecture can have a higher data bandwidth because a processor can access one memory device while another memory

device is responding to a prior memory access. For example, the processor can issue a read data request to one of the memory devices in the system while another memory device in the system is preparing to provide read data to the processor. The operating efficiency of computer systems using a memory hub architecture allow them to perform memory intensive operations like data mining significantly faster than systems in which the processor accesses each of several memory devices.

[007] Although a memory hub architecture allows a processor to more rapidly access system memory devices when performing memory intensive operations such as data mining, memory hub architectures do not eliminate the problems inherent in repetitive data fetch operations. As a result, memory intensive operations like data mining can still require a considerable period of time even when a computer system uses system memory having a memory hub architecture.

[008] There is therefore a need for a system and method that allows a processor to perform data mining at a significantly faster rate by avoiding the need for a large number of repetitive memory read operations.

SUMMARY OF THE INVENTION

[009] A memory module includes a memory device and a memory hub. The memory hub includes link interface and a data mining module coupled to both the link interface and the memory device. The data mining module is operable to receive at least one item of search data through the link interface. The data mining module then repetitively couples read memory requests to the memory devices, and the memory devices respond by outputting read data to the data mining module. The data mining module then compares the read data to the search data to determine if there is a data match. In the event of a data match, a data match indication is coupled from the memory module, either as the data match occurs or after being stored in a results memory.

BRIEF DESCRIPTION OF THE DRAWINGS

[010] Figure 1 is a block diagram of a computer system having memory modules in a memory hub architecture in which embodiments of the present invention can be implemented.

[011] Figure 2 is a block diagram of a memory hub according to an embodiment of the present invention for use with the memory modules that may be used in the computer system of Figure 1 or in other processor-based systems.

[012] Figure 3 is a block diagram of one embodiment of a data mining module used in the memory hub of Figure 2.

[013] Figure 4 is a block diagram of a memory hub according to another embodiment of the present invention for use with the memory modules that may be used in the computer system of Figure 1 or in other processor-based systems.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

[014] Embodiments of the present invention are directed to a memory hub module having the capability of internally performing data mining operations. Certain details are set forth below to provide a sufficient understanding of various embodiments of the invention. However, it will be clear to one skilled in the art that the invention may be practiced without these particular details. In other instances, well-known circuits, control signals, and timing protocols have not been shown in detail in order to avoid unnecessarily obscuring the invention.

[015] A computer system 100 according to one embodiment of the invention is shown in Figure 1. The computer system 100 includes a processor 104 for performing various computing functions, such as executing specific software to perform specific calculations or tasks. The processor 104 includes a processor bus 106 that normally includes an address bus, a control bus, and a data bus. The processor bus 106 is typically coupled to cache memory 108, which, is typically static random access memory ("SRAM"). Finally, the processor bus 106 is coupled to a system controller 110, which is also sometimes referred to as a bus bridge.

[016] The system controller 110 serves as a communications path to the processor 104 for a variety of other components. More specifically, the system controller 110 includes a graphics port that is typically coupled to a graphics controller 112, which is, in turn, coupled to a video terminal 114. The system controller 110 is also coupled to one or more input devices 118, such as a keyboard or a mouse, to allow an operator to interface with the computer system 100. Typically, the computer system 100 also includes one or more output devices 120, such as a printer, coupled to the processor 104

through the system controller 110. One or more data storage devices 124 are also typically coupled to the processor 104 through the system controller 110 to allow the processor 104 to store data or retrieve data from internal or external storage media (not shown). Examples of typical storage devices 124 include hard and floppy disks, tape cassettes, and compact disk read-only memories (CD-ROMs).

[017] The system controller 110 includes a memory hub controller 128 that is coupled to several memory modules 130a,b...n, which serve as system memory for the computer system 100. The memory modules 130 are preferably coupled to the memory hub controller 128 through a high-speed link 134, which may be an optical or electrical communication path or some other type of communications path. In the event the high-speed link 134 is implemented as an optical communication path, the optical communication path may be in the form of one or more optical fibers. In such case, the memory hub controller 128 and the memory modules will include an optical input/output port or separate input and output ports coupled to the optical communication path. The memory modules 130 are shown coupled to the memory hub controller 128 in a multi-drop arrangement in which the single high-speed link 134 is coupled to all of the memory modules 130. However, it will be understood that other topologies may also be used. For example, a point-to-point coupling arrangement may be used in which a separate high-speed link (not shown) is used to couple each of the memory modules 130 to the memory hub controller 128. A switching topology may also be used in which the memory hub controller 128 is selectively coupled to each of the memory modules 130 through a switch (not shown). Other topologies that may be used will be apparent to one skilled in the art.

[018] Each of the memory modules 130 includes a memory hub 140 for controlling access to eight memory devices 148, which, in the example illustrated in Figure 1, are synchronous dynamic random access memory ("SDRAM") devices. However, a fewer or greater number of memory devices 148 may be used, and memory devices other than SDRAM devices may also be used. The memory hub 140 is coupled to each of the system memory devices 148 through a bus system 150, which normally includes a control bus, an address bus, and a data bus. However, other bus systems, such as a bus system using a shared command/address bus, may also be used

[019] Figure 2 shows a memory hub 200 according to one embodiment of the present invention, which can be used as the memory hub 140 of Figure 1. The memory hub 200 is shown coupled to four memory devices 240a-d, which, in the present example are conventional SDRAM devices. In an alternative embodiment, the memory hub 200 is coupled to four different banks of memory devices, rather than merely four different memory devices 240a-d, with each bank typically having a plurality of memory devices. However, for the purpose of providing an example, the memory hub 200 is shown coupled to four memory devices 240a-d. It will be appreciated that the necessary modifications to the memory hub 200 a greater or lesser number of memory devices or to accommodate multiple banks of memory is within the knowledge of those ordinarily skilled in the art.

[020] Further included in the memory hub 200 are link interfaces 210a-d, which may be used to couple the memory hub 200 to respective processors or other memory access devices. In the embodiment shown in Figure 1, only one memory access device, and hence only on link interface 210a, is used. The memory hub 200 also includes link interfaces 212a-d for coupling the memory module on which the memory hub 200 is located to other memory modules (not shown). These link interfaces 212a-d are not used in the embodiment of Figure 1. In any case, the link interfaces 210a-d and 212a-d are preferably coupled to a first high speed data link 220 and a second high speed data link 222, respectively. As previously discussed with respect to Figure 1, the high speed data links 220, 222 can be implemented using an optical or electrical communication path or some other type of communication path. The link interfaces 210a-d, 212a-d are conventional, and include circuitry used for transferring data, command, and address information to and from the high speed data links 220, 222. As well known, such circuitry includes transmitter and receiver logic known in the art. It will be appreciated that those ordinarily skilled in the art have sufficient understanding to modify the link interfaces 210a-d, 212a-d to be used with specific types of communication paths, and that such modifications to the link interfaces 210a-d, 212a-d can be made without departing from the scope of the present invention. For example, in the event the high-speed data link 220, 222 is implemented using an optical communications path, the link interfaces 210a-d, 212a-d will include an optical input/output port that can convert optical signals coupled through the optical communications path into electrical signals.

[021] The link interfaces 210a-d, 212a-d include circuitry that allow the memory hub 140 to be connected in the system memory in a variety of configurations. For example, the multi-drop arrangement, as shown in Figure 1, can be implemented by coupling each memory module to the memory hub controller 128 through either the link interfaces 210a-d or 212a-d. Alternatively, a point-to-point or daisy chain configuration can be implemented by coupling the memory modules in series. For example, the link interfaces 210a-d can be used to couple a first memory module and the link interfaces 212a-d can be used to couple a second memory module. The memory module coupled to a processor, or system controller, will be coupled thereto through one set of the link interfaces and further coupled to another memory module through the other set of link interfaces. In one embodiment of the present invention, the memory hub 200 of a memory module is coupled to the processor in a point-to-point arrangement in which there are no other devices coupled to the connection between the processor 104 and the memory hub 200. This type of interconnection provides better signal coupling between the processor 104 and the memory hub 200 for several reasons, including relatively low capacitance, relatively few line discontinuities to reflect signals and relatively short signal paths.

[022] The link interfaces 210a-d, 212a-d are coupled to a switch 260 through a plurality of bus and signal lines, represented by busses 214. The busses 214 are conventional, and include a write data bus and a read data bus, although a single bi-directional data bus may alternatively be provided to couple data in both directions through the link interfaces 210a-d, 212a-d. It will be appreciated by those ordinarily skilled in the art that the busses 214 are provided by way of example, and that the busses 214 may include fewer or greater signal lines, such as further including a request line and a snoop line, which can be used for maintaining cache coherency.

[023] The switch 260 is further coupled to four memory interfaces 270a-d which are, in turn, coupled to the memory devices 240a-d, respectively. By providing a separate and independent memory interface 270a-d for each memory device 240a-d, respectively, the memory hub 200 avoids bus or memory bank conflicts that typically occur with single channel memory architectures. The switch 260 is coupled to each memory interface through a plurality of bus and signal lines, represented by busses 274. The busses 274 include a write data bus, a read data bus, and a request line. However, it

will be understood that a single bi-directional data bus or some other type of bus system may alternatively be used instead of a separate write data bus and read data bus. Moreover, the busses 274 can include a greater or lesser number of signal lines than those previously described.

[024] In an embodiment of the present invention, each memory interface 270a-d is specially adapted to the memory devices 240a-d to which it is coupled. More specifically, each memory interface 270a-d is specially adapted to provide and receive the specific signals received and generated, respectively, by the memory device 240a-d to which it is coupled. Also, the memory interfaces 270a-d are capable of operating with memory devices 240a-d operating at different clock frequencies. As a result, the memory interfaces 270a-d isolate the processor 104 from changes that may occur at the interface between the memory hub 230 and memory devices 240a-d coupled to the memory hub 200, and it provides a more controlled environment to which the memory devices 240a-d may interface.

[025] The switch 260 coupling the link interfaces 210a-d, 212a-d and the memory interfaces 270a-d can be any of a variety of conventional or hereinafter developed switches. For example, the switch 260 may be a cross-bar switch that can simultaneously couple link interfaces 210a-d, 212a-d and the memory interfaces 270a-d to each other in a variety of arrangements. The switch 260 can also be a set of multiplexers that do not provide the same level of connectivity as a cross-bar switch but nevertheless can couple the some or all of the link interfaces 210a-d, 212a-d to each of the memory interfaces 270a-d. The switch 260 may also include arbitration logic (not shown) to determine which memory accesses should receive priority over other memory accesses. Bus arbitration performing this function is well known to one skilled in the art.

[026] With further reference to Figure 2, each of the memory interfaces 270a-d includes a respective memory controller 280, a respective write buffer 282, a respective cache memory unit 284, and a respective data mining module 290. The memory controller 280 performs the same functions as a conventional memory controller by providing control, address and data signals to the memory device 240a-d to which it is coupled and receiving data signals from the memory device 240a-d to which it is coupled. However, the nature of the signals sent and received by the memory controller

280 will correspond to the nature of the signals that the memory devices 240a-d are adapted to send and receive. The cache memory unit 284 includes the normal components of a cache memory, including a tag memory, a data memory, a comparator, and the like, as is well known in the art. The memory devices used in the write buffer 282 and the cache memory unit 284 may be either DRAM devices, static random access memory ("SRAM") devices, other types of memory devices, or a combination of all three. Furthermore, any or all of these memory devices as well as the other components used in the cache memory unit 284 may be either embedded or stand-alone devices.

[027] The write buffer 282 in each memory interface 270a-d is used to store write requests while a read request is being serviced. In such a system, the processor 104 can issue a write request to a system memory device 240a-d even if the memory device to which the write request is directed is busy servicing a prior write or read request. The write buffer 282 preferably accumulates several write requests received from the switch 260, which may be interspersed with read requests, and subsequently applies them to each of the memory devices 240a-d in sequence without any intervening read requests. By pipelining the write requests in this manner, they can be more efficiently processed since delays inherent in read/write turnarounds are avoided. The ability to buffer write requests to allow a read request to be serviced can also greatly reduce memory read latency since read requests can be given first priority regardless of their chronological order.

[028] The use of the cache memory unit 284 in each memory interface 270a-d allows the processor 104 to receive data responsive to a read command directed to a respective system memory device 240a-d without waiting for the memory device 240a-d to provide such data in the event that the data was recently read from or written to that memory device 240a-d. The cache memory unit 284 thus reduces the read latency of the system memory devices 240a-d to maximize the memory bandwidth of the computer system. Similarly, the processor 104 can store write data in the cache memory unit 284 and then perform other functions while the memory controller 280 in the same memory interface 270a-d transfers the write data from the cache memory unit 284 to the system memory device 240a-d to which it is coupled.

[029] The data mining module 290 is coupled to the switch 260 through a bus 292 and to a respective one of the memory devices 240a-d. The data mining module 290

receives data that is to be searched in the respective memory device 240a-d. The search data are coupled from a processor or other memory access device (not shown in Figure 2) to the data mining module 290 through a respective link interface 210a-d and the switch 260. The search data coupled to the data mining module 290 may be either a single item of data, such as a word or a number, or several different items of data. The data mining module 290 causes items of read data to be repetitively read from its respective memory device 240a-d, and it then compares each item of read data to the search data, and couples the results of each positive comparison to the processor or other memory access device through the switch 260 and link interface 210a-d. Alternatively, the results of several positive comparisons may be saved in a storage device. For example, the results data for several items of search data may be transferred after all of the data in the respective memory device 240a-d have been searched. The saved results data are then transferred to the processor or other memory access device at the same time. The results data that are transferred from the data mining module 290 are preferably the address where the positively compared read data were stored in the respective memory device 240a-d. However, if multiple data items have been searched, the results data preferably includes data indicating which item of search has been found. For example, each of several items of results data may include the item of search data that was found paired with the address in the memory device 240a-d where that item of search data was found.

[030] Further included in the memory hub 200 may be a direct memory access ("DMA") engine 296 coupled to the switch 260 through a bus 298. The DMA engine 296 enables the memory hub 200 to move blocks of data from one location in the system memory to another location in the system memory without intervention from the processor 104. The bus 298 includes a plurality of conventional bus lines and signal lines, such as address, control, data busses, and the like, for handling data transfers in the system memory. Conventional DMA operations well known by those ordinarily skilled in the art can be implemented by the DMA engine 296. The DMA engine 296 is able to read a link list in the system memory to execute the DMA memory operations without processor intervention, thus, freeing the processor 104 and the bandwidth limited system bus from executing the memory operations. The DMA engine 296 can also include circuitry to accommodate DMA operations on multiple channels, for

example, for each of the system memory devices 240a-d. Such multiple channel DMA engines are well known in the art and can be implemented using conventional technologies.

[031] Although the data mining modules 290a-d are shown in Figure 2 as being coupled directly to the respective memory devices 240a-d, other arrangements may be used. For example, the data mining modules 290a-d may be coupled to the respective memory controllers 280a-d so that the read requests are issued by the memory controllers 280a-d, and the resulting read data are either coupled directly to the data mining modules 290a-d or coupled through the memory controllers 280a-d.

[032] One embodiment of a data mining module 300 that can be used as the data mining module 290 of Figure 2 is shown in Figure 3. The data mining module 300 includes a DMA engine 302 that operates much like the DMA engine 296 in the memory module 200 (Figure 2) to transfer data to and from the memory devices 240a-d without using a processor. The DMA engine 302 is coupled to the bus 292 and is preferably configured by a processor or other memory access device (not shown in Figure 3) through one of the link interfaces 210a-d and the switch 260. For example, the DMA engine 302 may receive information specifying a range of memory addresses that are to be searched. The DMA engine 302 then couples signals to a memory sequencer 306 that causes the memory sequencer 306 to generate properly timed signals memory command and address signals for a series of sequentially conducted read operations. Alternatively, the DMA engine 302 may apply signals to the respective memory controller 280, and the memory controller 280 generates the command and address signals for a series of sequentially conducted read operations.

[033] Regardless of how the command and address signals for read operations are generated, each read operations results in an item of read data being returned to the data mining module 300. However, before commencing the read operations, one or more items of search data are coupled from a processor or other memory access devices (not shown in Figure 3) and stored in a search data memory 314. The search data memory 314 then continuously outputs the search data to one or more comparators 320. The number of comparators 320 included in the data mining module 300 preferably corresponds to the number of items of search data stored in the search data memory 314. In the data mining module shown in Figure 3, the search data memory 314 stores three

items of search data, so there are three comparators 320a-c each of which receives a respective one of the search data items stored in the search data memory 314. However, as previously mentioned, the number of search data items stored in the search data memory 314 and the number of comparators 320 provided may vary as desired. Also, a single comparator 320 could be used even though several items of search data were stored in the memory 314. In such case, the search data memory 314 would sequentially couple each item of search data to the single comparator 320, and a search for that data item would be conducted. However, this approach is less desirable because it would be necessary to repetitively read all of the data stored in the memory device 240 each time a new data item was searched.

[034] Each item of read data received from the respective memory device 240a-d is passed to all of the comparators 320a-c. Each comparator 320a-c then compares the item of read data to its respective search data item and outputs a hit indication if there is a match. In the data mining module 300 embodiment shown in Figure 3, each hit indication includes information identifying the item of search data for which there was a hit. The hit indication is coupled to a results memory 330, which may be a static random access memory ("SRAM") device. The results memory 330 is also coupled to the DRAM sequencer 306 to receive the address passed to the respective memory device 240a-d. The results memory 330 then stores both the information identifying the item of search data and the address of the read data for which there was a hit. Alternatively, where the processor or other memory access device is capable of identifying the read data stored at each address in memory, it may be unnecessary for the results memory 330 to store the information identifying the item of search data for which there was a hit.

[035] When all of the addresses in the address space of the respective memory device 240a-d have been searched, the results memory outputs its contents to the processor or other memory access device through the bus 292, which is coupled to one of the link interfaces 210a-d through the switch 260.

[036] Another example of a memory hub 350 according to the present invention is shown in Figure 4. The memory hub 350 may also be used as the memory hub 140 in the computer system 100 of Figure 1. The memory hub 350 differs from the memory hub 200 shown in Figure 2 primarily by using a single data mining module 300 to service all of the memory devices 240a-d to which the memory hub 350 is coupled.

Therefore, only one data mining module 300 is provided for the entire memory hub 350 rather than a data mining module 300 for each of the four memory interfaces 270a-d in the memory hub 200 of Figure 2. However, all of the other components of the memory hub 350 are identical to and operate in the same manner as corresponding components in the memory hub 200 of Figure 2. Therefore, in the interest of brevity, and explanation of their structure and operation will not be repeated.

[037] The single data mining module 300 in the memory hub 350 is coupled to all of the link interfaces 210a-d and to all of the memory devices 240a-d through the switch 260. The data mining module 300 operates in the memory hub 350 in essentially the same manner that it operated in the memory hub 200. However, instead of allowing simultaneous searches of the memory device 240a-d, each of the memory devices 240a-d are separately searched in sequence.

[038] From the foregoing it will be appreciated that, although specific embodiments of the invention have been described herein for purposes of illustration, various modifications may be made without deviating from the spirit and scope of the invention. Accordingly, the invention is not limited except as by the appended claims.

CLAIMS

What is claimed is:

1. A memory hub for use with a memory device, the memory hub comprising:

a link interface for receiving memory requests;

a memory device interface coupled to the link interface, the memory device interface outputting write memory requests and write data, the memory device interface further outputting read memory requests and receiving read data in response thereto; and

a data mining module coupled to the link interface, the data mining module being operable to receive at least one item of search data through the link interface, to repetitively cause read memory requests to be output from the memory hub, to receive read data responsive to each of the read memory requests, and to compare the received read data to the at least one item of search data.

2. The memory hub of claim 1, further comprising a plurality of link interfaces, a plurality of memory device interfaces, and a switch for selectively coupling one of the plurality of link interfaces and one of the plurality of memory device interfaces.

3. The memory hub of claim 1 wherein the data mining module is operable to generate the read memory requests and to output the read memory requests from the memory hub.

4. The memory hub of claim 1 wherein the data mining module comprises:

a direct memory access engine coupled to the link interface, the direct memory access engine being operable to generate the read memory requests;

a search data memory coupled to the link interface to receive and store the at least one item of search data; and

a comparator for each item of search data stored in the search data memory, each comparator being coupled to receive a respective item of search data from the search data memory and being coupled to receive the read data, the comparator being operable to compare the read data to the respective item of search data and provide a hit indication in the event of a match.

5. The memory hub of claim 4 wherein an output of the comparator is coupled to the link interface to couple the hit indication to the link interface.

6. The memory hub of claim 4 wherein the data mining module further comprises a memory device sequencer coupled to the direct memory access engine, the memory device sequencer generating a set of command and address signals for each of the read requests.

7. The memory hub of claim 4 wherein the search data memory stores a plurality of the search data items, and wherein the data mining module comprises a plurality of comparators corresponding in number to the number of search data items stored in the search data memory.

8. The memory hub of claim 4 further comprising a results memory coupled to an output of the comparator to store each of the hit indications generated by each of the comparators.

9. The memory hub of claim 8 wherein the results memory is operable to store a memory device address corresponding to the read data that resulted in each of the hit indications.

10. The memory hub of claim 9 wherein the results memory is further operable to store with each of the memory device addresses a corresponding item of search data.

11. The memory hub of claim 1 wherein the link interface, the memory device interface, and the data mining module are fabricated as an integrated circuit on a common semiconductor substrate.

12. A memory module, comprising:

a plurality of memory devices; and

a memory hub, comprising:

a link interface for receiving memory requests for access to at least one of the memory devices;

a memory device interface coupled to the link interface and to the memory devices, the memory device interface coupling write memory requests and write data to the memory devices, the memory device interface further coupling read memory requests to the memory devices and coupling read data from the memory devices; and

a data mining module coupled to at least one of the memory devices, the data mining module being operable to receive at least one item of search data through the link interface, to repetitively cause read memory requests to be output from the memory hub, to receive read data responsive to each of the read memory requests, and to compare the received read data to the at least one item of search data.

13. The memory module of claim 12 wherein the data mining module is operable to generate the read memory requests and to output the read memory requests from the memory hub.

14. The memory module of claim 12 wherein the memory hub further comprises a plurality of link interfaces, a plurality of memory device interfaces coupled to a respective memory device, and a switch for selectively coupling one of the plurality of link interfaces and one of the plurality of memory device interfaces.

15. The memory module of claim 14 wherein one of the data mining modules is provided for each of the memory device interfaces, each of the data mining modules being coupled to the memory device to which the respective memory device interface is coupled.

16. The memory module of claim 14 wherein the memory module includes a single data mining module that is coupled to each of the memory device interfaces through the switch.

17. The memory module of claim 12 wherein the data mining module comprises:

- a direct memory access engine coupled to the link interface, the direct memory access engine being operable to generate the read memory requests for coupling to the memory devices;

- a search data memory coupled to the link interface to receive and store the at least one item of search data; and

- a comparator for each item of search data stored in the search data memory, each comparator being coupled to receive a respective item of search data from the search data memory and being coupled to receive the read data from the memory devices, the comparator being operable to compare the read data to the respective item of search data and provide a hit indication in the event of a match.

18. The memory module of claim 17 wherein an output of the comparator is coupled to the link interface to couple the hit indication to the link interface.

19. The memory module of claim 17 wherein the data mining module further comprises a memory device sequencer coupled to the direct memory access engine and to the memory devices, the memory device sequencer generating a set of command and address signals for coupling to the memory devices for each of the read requests.

20. The memory module of claim 17 wherein the search data memory stores a plurality of the search data items, and wherein the data mining module comprises a plurality of comparators corresponding in number to the number of search data items stored in the search data memory.

21. The memory module of claim 17 further comprising a results memory coupled to an output of the comparator to store each of the hit indications generated by each of the comparators.

22. The memory module of claim 21 wherein the results memory is operable to store a memory device address indicative of a location in the memory devices where read data that resulted in each of the hit indications was stored.

23. The memory module of claim 22 wherein the results memory is further operable to store with each of the memory device addresses a corresponding item of search data that matched read stored at the respective address.

24. The memory module of claim 12 wherein the plurality of memory devices comprises a plurality of synchronous random access memory devices.

25. The memory module of claim 12 wherein the link interface, the memory device interface, and the data mining module are fabricated as an integrated circuit on a common semiconductor substrate.

26. The memory module of claim 26 wherein the common semiconductor substrate further comprises the memory devices.

27. A memory module, comprising:

a memory device; and

a memory hub, comprising:

a link interface for receiving memory requests for access to the memory device;

a memory device interface coupled to the link interface and to the memory device, the memory device interface coupling write memory requests and write data to the memory device, the memory device interface further coupling read memory requests to the memory device and coupling read data from the memory device;

a direct memory access engine coupled to the link interface, the direct memory access engine being operable to generate the read memory requests for coupling to the memory device;

a search data memory coupled to the link interface to receive and store the at least one item of search data; and

a comparator for each item of search data stored in the search data memory, each comparator being coupled to receive a respective item of search data from the search data memory and being coupled to receive the read data from the memory device, the comparator being operable to compare the read data to the respective item of search data and provide a hit indication in the event of a match.

28. The memory module of claim 27 wherein the memory module comprises a plurality of memory devices, and wherein the memory hub further comprises a plurality of link interfaces, a plurality of memory device interfaces coupled to a respective memory device, and a switch for selectively coupling one of the plurality of link interfaces and one of the plurality of memory device interfaces.

29. The memory module of claim 27 wherein an output of the comparator is coupled to the link interface to couple the hit indication to the link interface.

30. The memory module of claim 27 wherein the data mining module further comprises a memory device sequencer coupled to the direct memory access engine and to the memory devices, the memory device sequencer generating a set of command and address signals for each of the read requests for coupling to the memory device.

31. The memory module of claim 27 wherein the search data memory stores a plurality of the search data items, and wherein the memory hub comprises a plurality of comparators corresponding in number to the number of search data items stored in the search data memory.

32. The memory module of claim 27 further comprising a results memory coupled to an output of the comparator to store each of the hit indications generated by each of the comparators.

33. The memory module of claim 27 wherein the results memory is operable to store a memory device address indicative of a location in the memory devices where read data that resulted in each of the hit indications was stored.

34. The memory module of claim 33 wherein the results memory is further operable to store with each of the memory device addresses a corresponding item of search data that matched read stored at the respective address.

35. The memory module of claim 27 wherein the plurality of memory devices comprises a plurality of synchronous random access memory devices.

36. The memory module of claim 27 wherein the link interface, the memory device interface, the direct memory access engine, the search data memory, and the comparator for each item of search data stored in the search data memory are fabricated as an integrated circuit on a common semiconductor substrate.

37. The memory module of claim 36 wherein the common semiconductor substrate further comprises the memory device.

38. A processor-based system, comprising:
a processor having a processor bus;
a system controller coupled to the processor bus, the system controller having a system memory port and a peripheral device port;
at least one input device coupled to the peripheral device port of the system controller;
at least one output device coupled to the peripheral device port of the system controller;
at least one data storage device coupled to the peripheral device port of the system controller; and
a memory module coupled to the system memory port of the system controller, the memory module comprising:
a plurality of memory devices; and

a memory hub, comprising:

a link interface for receiving memory requests for access to at least one of the memory devices;

a memory device interface coupled to the link interface and to the memory devices, the memory device interface coupling write memory requests and write data to the memory devices, the memory device interface further coupling read memory requests to the memory devices and coupling read data from the memory devices; and

a data mining module coupled to at least one of the memory devices, the data mining module being operable to receive at least one item of search data through the link interface, to repetitively cause read memory requests to be output from the memory hub, to receive read data responsive to each of the read memory requests, and to compare the received read data to the at least one item of search data.

39. The processor-based system of claim 38 wherein the data mining module is operable to generate the read memory requests and to output the read memory requests from the memory hub.

40. The processor-based system of claim 38 wherein the memory hub further comprises a plurality of link interfaces, a plurality of memory device interfaces coupled to a respective memory device, and a switch for selectively coupling one of the plurality of link interfaces and one of the plurality of memory device interfaces.

41. The processor-based system of claim 40 wherein one of the data mining modules is provided for each of the memory device interfaces, each of

the data mining modules being coupled to the memory device to which the respective memory device interface is coupled.

42. The processor-based system of claim 40 wherein the memory module includes a single data mining module that is coupled to each of the memory devices through the switch.

43. The processor-based system of claim 38 wherein the data mining module comprises:

- a direct memory access engine coupled to the link interface, the direct memory access engine being operable to generate the read memory requests for coupling to the memory devices;

- a search data memory coupled to the link interface to receive and store the at least one item of search data; and

- a comparator for each item of search data stored in the search data memory, each comparator being coupled to receive a respective item of search data from the search data memory and being coupled to receive the read data from the memory devices, the comparator being operable to compare the read data to the respective item of search data and provide a hit indication in the event of a match.

44. The processor-based system of claim 43 wherein an output of the comparator is coupled to the link interface to couple the hit indication to the link interface.

45. The processor-based system of claim 43 wherein the data mining module further comprises a memory device sequencer coupled to the direct memory access engine and to the memory devices, the memory device sequencer generating a set of command and address signals for coupling to the memory devices for each of the read requests.

46. The processor-based system of claim 43 wherein the search data memory stores a plurality of the search data items, and wherein the data mining module comprises a plurality of comparators corresponding in number to the number of search data items stored in the search data memory.

47. The processor-based system of claim 43 further comprising a results memory coupled to an output of the comparator to store each of the hit indications generated by each of the comparators.

48. The processor-based system of claim 47 wherein the results memory is operable to store a memory device address indicative of a location in the memory devices where read data that resulted in each of the hit indications was stored.

49. The processor-based system of claim 48 wherein the results memory is further operable to store with each of the memory device addresses a corresponding item of search data that matched read stored at the respective address.

50. The processor-based system of claim 38 wherein the plurality of memory devices comprises a plurality of synchronous random access memory devices.

51. The processor-based system of claim 38 wherein the link interface, the memory device interface, and the data mining module are fabricated as an integrated circuit on a common semiconductor substrate.

52. The processor-based system of claim 51 wherein the common semiconductor substrate further comprises the memory devices.

53. A processor-based system, comprising:

- a processor having a processor bus;
- a system controller coupled to the processor bus, the system controller having a system memory port and a peripheral device port;
- at least one input device coupled to the peripheral device port of the system controller;
- at least one output device coupled to the peripheral device port of the system controller;
- at least one data storage device coupled to the peripheral device port of the system controller; and
- a memory module coupled to the system memory port of the system controller, the memory module comprising:
 - a memory device; and
 - a memory hub, comprising:
 - a link interface for receiving memory requests for access to the memory device;
 - a memory device interface coupled to the link interface and to the memory device, the memory device interface coupling write memory requests and write data to the memory device, the memory device interface further coupling read memory requests to the memory device and coupling read data from the memory device;
 - a direct memory access engine coupled to the link interface, the direct memory access engine being operable to generate the read memory requests for coupling to the memory device;
 - a search data memory coupled to the link interface to receive and store the at least one item of search data; and
 - a comparator for each item of search data stored in the search data memory, each comparator being coupled to receive a respective item of search data from the search data

memory and being coupled to receive the read data from the memory device, the comparator being operable to compare the read data to the respective item of search data and provide a hit indication in the event of a match.

54. The processor-based system of claim 53 wherein the memory module comprises a plurality of memory devices, and wherein the memory hub further comprises a plurality of link interfaces, a plurality of memory device interfaces coupled to a respective memory device, and a switch for selectively coupling one of the plurality of link interfaces and one of the plurality of memory device interfaces.

55. The processor-based system of claim 53 wherein an output of the comparator is coupled to the link interface to couple the hit indication to the link interface.

56. The processor-based system of claim 53 wherein the data mining module further comprises a memory device sequencer coupled to the direct memory access engine and to the memory devices, the memory device sequencer generating a set of command and address signals for each of the read requests for coupling to the memory device.

57. The processor-based system of claim 53 wherein the search data memory stores a plurality of the search data items, and wherein the memory hub comprises a plurality of comparators corresponding in number to the number of search data items stored in the search data memory.

58. The processor-based system of claim 53 further comprising a results memory coupled to an output of the comparator to store each of the hit indications generated by each of the comparators.

59. The processor-based system of claim 58 wherein the results memory is operable to store a memory device address indicative of a location in the memory devices where read data that resulted in each of the hit indications was stored.

60. The processor-based system of claim 59 wherein the results memory is further operable to store with each of the memory device addresses a corresponding item of search data that matched read stored at the respective address.

61. The processor-based system of claim 53 wherein the plurality of memory devices comprises a plurality of synchronous random access memory devices.

62. The processor-based system of claim 53 wherein the link interface, the memory device interface, the direct memory access engine, the search data memory, and the comparator for each item of search data stored in the search data memory are fabricated as an integrated circuit on a common semiconductor substrate.

63. The processor-based system of claim 62 wherein the common semiconductor substrate further comprises the memory device.

64. A method of searching for items of search data stored in a memory device that is located in a memory module, the method comprising:

passing at least one item of search data to the memory module;

storing the at least one item of search data from within the memory module;

sequentially initiating a plurality of read memory requests in the memory module;

sequentially coupling the read memory requests to the memory device;

receiving read data at the memory module responsive to each of the read memory requests;

comparing the received read data to the at least one item of search data within the memory module to determine if there is a data match;

generating a results indication responsive to each data match; and

coupling the results indication from the memory module.

65. The method of claim 64 wherein the act of generating a results indication responsive to each data match comprises providing a memory device address indicative of a location in the memory devices where read data that resulted in each of the data matches was stored.

66. The method of claim 65 wherein the act of generating a results indication responsive to each data match further comprises providing with each memory device address a corresponding item of search data that was matched.

67. The method of claim 64, further comprising storing the results indication responsive to each data match prior to coupling the results indication from the memory module.

68. In a processor-based system having a processor coupled to a system controller having a system memory port, a method of searching for items of search data stored in a system memory device that is located in a memory module, the method comprising:

coupling at least one item of search data from the processor to the memory module;

storing the at least one item of search data in the memory module;

sequentially initiating a plurality of read memory requests from within the memory module;
coupling the read memory requests to the memory device;
coupling read data from the memory device responsive to each of the read memory requests;
comparing the read data to the at least one item of search data within the memory module to determine if there is a data match;
generating a results indication responsive to each data match; and
coupling the results indication from the memory module to the processor.

69. The method of claim 68 wherein the act of generating a results indication responsive to each data match comprises providing a memory device address indicative of a location in the memory devices where read data that resulted in each of the data matches was stored.

70. The method of claim 69 wherein the act of generating a results indication responsive to each data match further comprises providing with each memory device address a corresponding item of search data that was matched.

71. The method of claim 68, further comprising storing the results indication within the memory module responsive to each data match prior to coupling the results indication from the memory module to the processor.

72. The method of claim 68 wherein the act of coupling the read memory requests to the memory device and the act of coupling the read data from the memory device are performed entirely within the memory module.