IP PROTECTION

BACKGROUND

[0001] Miniaturization of portable consumer products such as MP3 players, mobile phones, and digital camera is driving the need for smaller devices such as integrated circuits (IC) with high memory density and more functionality. As the size of the device becomes smaller, this however leads to higher production cost.

[0002] To reduce the fabrication cost, Multi-Projects-Wafer (MPW) is proposed as it offers the solution to integrate onto wafers a number of different designs modules which may also include intellectual property (IP) resources from various vendors or parties. Nevertheless, there could be risks where intellectual property (IP) resources from the various parties are exposed to third parties including competitors.

[0003] From the foregoing discussion, it is desirable to produce devices with low production cost and sufficient IP protection. It is also desirable to ensure IP protection during the delivery of the devices.

SUMMARY OF THE INVENTION

[0004] A method of forming a device is disclosed. The method includes providing a MPW mask having a plurality of chiplets pertaining to a plurality of IP owners. Non-relevant chiplet or chiplets of an IP owner are implemented with IP protection. A substrate is patterned using the MPW mask to form a device. The method further includes delivering the device to a relevant IP owner. The device includes the non-relevant chiplets of the IP owner, wherein IP protection reduces disclosure of IP information of the non-relevant chiplets to the relevant IP owner.

[0005] These and other objects, along with advantages and features of the present invention herein disclosed, will become apparent through reference to the following description and the accompanying drawings. Furthermore, it is to be understood that the features of the various

embodiments described herein are not mutually exclusive and can exist in various combinations and permutations.

BRIEF DESCRIPTION OF THE DRAWINGS

[0006] In the drawings, like reference characters generally refer to the same parts throughout the different views. Also, the drawings are not necessarily to scale, emphasis instead generally being placed upon illustrating the principles of the invention. In the following description, various embodiments of the present invention are described with reference to the following drawings, in which:

[0007] Fig. 1 shows a cross-sectional view of upper levels of a device;

[0008] Figs. 2a-b show different MPW masks;

[0009] Figs. 3a-b show other embodiments of MPW masks;

[0010] Figs. 4a-b show a wafer and device formed by a MPW mask set;

[0011] Figs. 5a-b show MPW masks implemented with IP protection;

[0012] Figs. 6a-b show an embodiment of a MPW mask with IP protection;

[0013] Figs. 7a-b show another embodiment of a MPW mask with IP protection;

[0014] Figs. 8a-b show yet another embodiment of a MPW mask with IP protection;

[0015] Fig. 9 shows a cross-sectional view of upper levels of an embodiment of a device;

[0016] Fig. 10 shows an embodiment of a process flow for implementing IP protection;

[0017] Figs. 11a-e show an embodiment of IP protection;

[0018] Fig. 12 shows another embodiment of IP protection;

[0019] Fig. 13 shows a process flow of implementing IP protection; and

[0020] Figs. 14a-b show wafers delivered to different IP owners.

DETAILED DESCRIPTION

[0021] The fabrication of devices, such as integrated circuits (ICs), involves the formation of features on a substrate that make up circuit components, such as transistors, resistors and capacitors. The devices are interconnected, enabling the device to perform the desired functions. Interconnections are formed by forming contacts and conductive lines in a dielectric layer using, for example, damascene techniques. The features and interconnections are formed by repeatedly depositing and patterning layers on the wafer. The devices may have multiple interconnection layers. The structures of the different layers of the device are created or patterned using respective mask and etch techniques.

[0022] The various features and interconnections are strategically placed on the device to minimize the use of space and/or optimize performance. The placement of various features and interconnections is referred to as a product or device layout. The layers which form the components are in the lower levels while the interconnections are in the upper levels of the device layout. The interconnections may be provided in a plurality of interconnect levels.

[0023] To pattern the substrate, including a layer or layers on the substrate, a reticle is used. The reticle contains the desired pattern which is to be transferred to a softmask, such as a photoresist, on the substrate. To transfer the pattern of the reticle to the softmask, a lithographic system is used, exposing the softmask with an exposure source through the reticle. After exposure, the softmask is developed to transfer the pattern on the reticle to the softmask. To improve lithographic resolution, an anti-reflective coating (ARC) may be employed below the soft mask.

[0024] Different masks or reticles are employed to form different layers or features of the device. For example, an active mask may be used to form the active regions of the device. The active mask, for example, may be referred to as an "RX" mask. Other masks may be used to form the different components, such as transistors, including p and n-type transistors. Multiple masks may be used to form multiple metal interconnect levels. An interconnect level may

include contact plugs and metal lines formed in a dielectric layer, such as an interlevel dielectric (ILD) layer. Separate masks may be provided for the via and metal line levels. The trench and vias may be formed using, for example, dual damascene techniques. Other techniques for forming vias and trenches may also be useful. The interconnects may be formed from a conductive material, such as copper, tungsten, aluminium or alloy or a combination thereof. Other types of conductive materials may also be used to form the interconnect levels. It is understood that the via and conductive line levels may be formed of the same or different materials.

[0025] In one embodiment, a pad interconnect level is provided as a top or final interconnect level of the device. The pad level is related to forming bond pad connections. The pad interconnect level includes a via pad level and a pad level. The via pad level may be referred to as the "VV" level while the pad level may be referred to as the "LB" level. A VV mask and a LB mask may be provided corresponding to the VV and LB levels. The VV and LB levels may be aluminium levels. In other embodiments, the VV and LB levels may be other types of metal levels, such as copper or copper-alloy. Other types of metals may be used for the VV and LB levels. Providing VV and LB levels of different materials may also be useful. A passivation layer, such as polyimide, is provided over the LB level. The passivation layer may also include other types of materials. The passivation layer may be referred to as the "PV" level. A PV mask may be provided corresponding to the PV level. For example, if a wire bonding process is employed, the PV level may be referred to as the "DV" level. On the other hand, if a flip chip process such as a Controlled Collapse Chip Connection (C4) is adopted, the PV level may be referred to as the "LV" level. It is understood that other designations may be employed to refer to the different levels.

[0026] The passivation layer is patterned to form openings for forming external electrical connections. For example, the openings may be for wire bonds or contact bumps in the case of flip chip applications.

[0027] Fig. 1 shows a cross section of a portion of a device 100. As shown, the device is formed on a substrate 105. The device includes a pad interconnect level 130. The pad interconnect level includes a pad level 150 disposed above a pad via level 140. Below the pad via level is a last metal interconnect level 120. The last metal interconnect level may be referred to as M_X level, where X is the high number in a device. The pad level includes one or more conductive pads 154 formed in a pad dielectric layer 152. The conductive pads are coupled to pad vias 144 in a pad via dielectric layer 142 therebelow. The pad vias may provide interconnections between the conductive lines 124 in the last metal level and conductive pads. A passivation layer 160 is disposed over the pad interconnect level. The passivation layer includes openings 164 to expose the conductive pads.

[0028] The device may include other device levels (not shown) to form components and other interconnects of the device. For example, the device may include components such as transistors, capacitors, and interconnect levels to provide the desired function.

A first party, such as a designer of devices or design houses, may provide a second party, such as device manufacturers or foundries, with information related to the device. A device designer, for example, may be referred to as an "IP provider". The information is used to produce a set of masks or reticles used to manufacture a desired device.

[0029] In one embodiment, the masks used to form a device are multi-project wafer (MPW) masks which include multiple devices. For example, the mask set used to form a device is a MPW mask set used to form more than one type of device on a wafer.

[0030] Figs. 2a-b show embodiments of MPW masks 200. Referring to Fig. 2a, the MPW mask is configured to form first and second devices or chiplets 210 and 220. In Fig. 2b, the

MPW mask is configured to form first, second, third and fourth chiplets 210, 220, 230 and 240. Providing MPW masks which form other number of chiplets may also be useful. In one embodiment, the MPW mask may be for 2n number of chiplets, where $n \geq 1$. In other embodiments, other number of chiplets > 1 may be formed on the MPW masks, including odd numbers. In one embodiment, the chiplets on the MPW masks are from at least 2 or more IP providers.

[0031] Figs. 3a-b show embodiments of MPW masks 300 which includes chiplets from different first parties. For example, Fig. 3a shows a first chiplet 310 from a first IP provider and a second chiplet 320 from a second IP provider. Fig. 3b, for example shows a first chiplet 310 from a first IP provider, a second chiplet 320 from a second IP provider, a third chiplet 330 from a third IP provider and a fourth chiplet from a fourth IP provider. It is understood that a MPW mask has at least two first parties. For example, in the case where the MPW masks have more than 2 chiplets, some chiplets may be from the same first party. The masks are used to form devices on a wafer which includes all the chiplets.

[0032] Fig. 4a shows a semiconductor wafer 400 containing devices formed from a MPW mask set. The semiconductor wafer, for example, comprises a silicon wafer. Other types of wafers are also useful. For example, the wafer may be a p-type, n-type, silicon-on-insulator or silicon germanium wafer. Depending on the type of device, the wafer may comprise a non-semiconductor material. The wafer may include a notch 421 to indicate the crystal orientation of the wafer. Other techniques for indicating the crystal orientation may also be useful. Additional indicators may also be included to indicate the dopant type of the wafer.

[0033] The wafer includes an active surface 411 on which devices 415 are formed. A plurality of devices may be formed on the wafer in parallel. The devices, for example, are arranged in rows along a first (x) direction and columns along a second (y) direction. The devices are subsequently singulated into individual dies, assembled and tested.

[0034] Fig. 4b shows a device 415 on the wafer in greater detail. As shown, the device formed by the MPW mask set includes first and second chiplets 420 and 430 from respective first parties or two IP providers. Wafers which may be processed by a second party, such as a foundry, are delivered to respective first parties. The wafers sent to both first parties contain the same devices or information. For example, the wafers sent to both parties contain chiplets of both parties. As such, the IP of one party may be accessed by the other party. For example, the IP of both parties may be accessed by either party.

[0035] In one embodiment, chiplets on a device which are not related to a party are IP protected to prevent disclosure of IP to non-relevant parties. The use of IP protection ensures that only the IP owner or a relevant party may access the IP of the chiplet. IP protection may include modifying the chiplets of non-relevant parties. For example, non-relevant chiplets are modified to obscure their IP.

[0036] Figs. 5a-b show devices 500 formed with a MPW mask set. The devices include first and second chiplets 510 and 520 for first and second first parties or IP owners. For example, the first chiplet 510 is designed by the first IP owner and the second chiplet 520 is designed by the second IP owner. In such case, the first chiplet is not relevant to the second IP owner and the second chiplet is not relevant to the first IP owner. Referring to Fig. 5a, the device includes the first chiplet 510 with no IP protection and the second chiplet 520 with IP protection. Wafers containing a plurality of such devices are sent to the first IP owner. On the other hand, wafers with devices such as that shown in Fig 5b in which the first chiplet 510 with IP protection and the second chiplet without IP protection are sent to the second IP owner.

[0037] In one embodiment, one or more masks of a MPW mask set are selected for implementing IP protection. The MPW mask set includes Y number of masks used for different levels of the device. Typically, Y is about 40 to 60 to form a device. Other values for Y may also be useful, depending on the types of devices formed or processes. The last mask used in

forming the device is equal to Y while the first mask used is equal to 1. In some cases, some masks may be reused for different processes. The number of masks selected for implementing IP protection for non-relevant chiplets is M, where M is ≥ 1 and less than Y.

[0038] When a nth mask of a MPW mask set is selected for IP protection, where n is a whole number from 1 to Y, the nth mask has a different version for different chiplets in the device of the MPW mask set. Preferably, the nth mask has a different version for different IP owners of the chiplets in the device. For example, in the case of two different IP owners having chiplets in the device of the MPW mask set, two different n^{th} mask are provided. In the event that an IP owner has more than one chiplet in the device, it may not be necessary to provide different masks for the chiplets owned by a common IP owner.

[0039] As the value of M increases, more masks are needed to form the devices for the different chiplets of IP owners. The number M, in one embodiment, should be a relatively low number to minimize the number of additional masks needed to implement IP protection. In one embodiment, M is from about 1 – 3. Providing other values of M may also be useful, depending on, for example, protection and process application requirements.

[0040] In one embodiment, the mask or masks selected for IP protection is related to the final processing steps of forming the device. In one embodiment, the nth mask selected to implement IP protection is related to the final processing steps, where n = Y to Y-2. For example, the mask selected can be any one of the masks related to the final three masks used in processing the device. In other embodiments, some or all of the final three masks used in processing the device may be selected for implementing IP protection. In yet other embodiments, more masks or masks at other stages of processing may be selected for IP protection or a combination thereof.

[0041] Regarding masks used in the final stages of a process, there may be masks employed in forming the pad via, pad, and passivation levels. For example, such masks may include the

VV, LB, and PV masks. As for the PV mask, it may be related to the DV or LV level, depending on the application. The PV mask or reticle, for example, may be R_Y, LB may be R_{Y-1} and VV may be R_{Y-2}. In one embodiment, VV, LB, PV or a combination thereof are selected for IP protection. Selecting other reticles for IP protection in addition to or in lieu of VV, LB, PV may also be useful.

[0042] In one embodiment, chiplets on a device which are not related to a party are IP protected to prevent disclosure of IP to non-relevant parties. The use of IP protection ensures that only the IP owner or a relevant party may access the IP of the chiplet. IP protection may include modifying the chiplets of non-relevant parties. For example, non-relevant chiplets are modified to obscure their IP.

[0043] In one embodiment, the mask selected for IP protection has chiplets of non-relevant IP providers implemented with IP protection. For example, mask data of non-relevant chiplets are manipulated to obscure the actual design of the IP owners. Manipulation of mask data may be achieved by additive or subtractive procedure or a combination thereof. In an additive procedure, data may be added to the original mask data which is designed by the IP owner; in a subtractive procedure, data may be removed from the original mask data which is designed by the IP owner. In the case of a combination of procedures, multiple procedures are employed. For example, data may be removed and additional data may be incorporated to provide modified data which is different from the original mask data designed by the IP owner. In other embodiments, multiple procedures may include any number of procedures ≥ 2. The multiple procedures may include any number of additive or subtractive procedures or a combination thereof.

[0044] Figs. 6a-b show embodiments of VV masks of a MPW set. As shown, the masks of the MPW set contain two chiplets 610 and 620 of two IP providers IP_1 and IP_2. It is understood that the MPW mask set may contain more than 2 chiplets from more than two IP providers.

[0045] Referring to Fig. 6a, the VV mask includes a via pattern 615 for the first chiplet. The via pattern is used to form vias in a substrate or wafer which correspond to contacts in the VV level. The via pattern is designed by IP_1. However, the second chiplet is modified to include IP protection. In one embodiment, the second chiplet includes no via pattern or no via data. For example, using this mask results in a blanket dielectric layer without any via openings in the VV level of the second chiplet. Other types of modifications of the VV level may also be employed to implement IP protection of the second chiplet. This VV mask is used to form wafers which are delivered to IP_1. By implementing IP protection on the second chiplet, IP of IP_2 will be protected from disclosure to IP_1.

[0046] In Fig. 6b, the VV mask is similar to that described in Fig. 6a except that the first chiplet is implemented with IP protection while the second chiplet is provided with the via pattern as designed by IP_2. The VV mask of Fig. 6b is used to form wafers which are delivered to IP_2. By implementing IP protection on the first chiplet, IP of IP_1 will be protected from disclosure to IP_2.

[0047] Figs. 7a-b show embodiments of LB masks of a MPW set. As shown, the masks of the MPW set contain two chiplets 710 and 720 of two IP providers IP_1 and IP_2. It is understood that the MPW mask set may contain more than 2 chiplets from more than two IP providers.

[0048] Referring to Fig. 7a, the LB mask includes a pad pattern 715 for the first chiplet. The pad pattern is used to form pads in a substrate or wafer which correspond to pads in the LB level. The pad pattern is designed by IP_1. However, the second chiplet is modified to include IP protection. In one embodiment, the second chiplet includes a dummy via fill pattern. For example, using this mask results in a plurality of dummy via openings in the LB level of the second chiplet. Other types of modifications of the LB level may also be employed to implement IP protection of the second chiplet. This LB mask is used to form wafers which are

delivered to IP_1. By implementing IP protection on the second chiplet, IP of IP_2 will be protected from disclosure to IP_1.

[0049] In Fig. 7b, the LB mask is similar to that described in Fig. 7a except that the first chiplet is implemented with IP protection while the second chiplet is provided with the pad pattern as designed by IP_2. The LB mask of Fig. 7b is used to form wafers which are delivered to IP_2. By implementing IP protection on the first chiplet, IP of IP_1 will be protected from disclosure to IP_2.

[0050] Figs. 8a-b show embodiments of LV masks of a MPW set. As shown, the masks of the MPW set contain two chiplets 810 and 820 of two IP providers IP_1 and IP_2. It is understood that the MPW mask set may contain more than 2 chiplets from more than two IP providers.

[0051] Referring to Fig. 8a, the LV mask includes a pad opening pattern 815 for the first chiplet. The pad opening pattern is used to form openings in the passivation layer to expose the pad thereunder. The pad opening pattern is designed by IP_1. However, the second chiplet is modified to include IP protection. In one embodiment, the second chiplet includes no pad opening pattern or no data. For example, the use of this mask forms a blanket passivation layer without any openings in the LV level of the second chiplet. Other types of modifications of the LV level may also be employed to implement IP protection of the second chiplet. The MPW mask set with the LV mask is used to form wafers which are delivered to IP_1. By implementing IP protection on the second chiplet, IP of IP_2 will be protected from disclosure to IP_1.

[0052] In Fig. 8b, the LV mask is similar to that described in Fig. 8a except that the first chiplet is implemented with IP protection while the second chiplet is provided with the pad opening pattern as designed by IP_2. The MPW mask set with the LV mask of Fig. 8b is used to form wafers which are delivered to IP_2. By implementing IP protection on the first chiplet, IP of IP_1 will be protected from disclosure to IP_2.

[0053] As described, Figs. 6-8 show various additive and subtractive processes applied to different masks of the MPW mask set. It is understood that one or more of any combination of IP protection may be applied to the masks of the MPW mask set. In some embodiments, masks $R_Y - R_{Y-2}$ are implemented with IP protection. For example, the VV, LB and LV masks are implemented with IP protection. In other embodiments, at least one of the $R_Y - R_{Y-2}$ masks is implemented with IP protection. In yet other embodiments, other mask or masks, in addition or in lieu of $R_Y - R_{Y-2}$ masks may be implemented with IP protection.

[0054] Fig. 9 shows a cross-sectional view of an embodiment of a non-related chiplet 900 implemented with IP protection. As shown, the device includes a pad interconnect level 130. The pad interconnect level includes a pad or LB level 150 disposed above a pad via or VV level 140. Below the pad via level is a last metal interconnect level 120. A passivation layer or PV level 160 is disposed over the pad interconnect level.

[0055] In one embodiment, IP protection is implemented in VV, LB and PV levels of the device for non-related chiplets. As shown, the VV level is implemented with a subtractive IP protection procedure. In one embodiment, the subtractive procedure comprises removing mask data, as described in Figs. 6a-b. The LB process is implemented with subtractive and additive IP protection procedures, as described in Figs. 7a-b. For example, a dummy via fill pattern 954 may be implemented. As for the PV level, it is implemented with a subtractive IP protection procedure, as described in Figs. 8a-b. Other reticles or other combination of additive and subtractive IP protection procedures may be implemented for the reticle or reticles.

[0056] Fig. 10 shows another embodiment of an IP protection procedure 1000 for non-relevant chiplets. The IP protection procedure includes a plurality of procedures. For example, first and second mask designs are provided at step 1010 and 1020. The first and second mask designs, in one embodiment, are modified mask designs which correspond to mask levels. For example, the mask levels may be derived from any different metal levels. The mask levels may

be from a chiplet or created for the purpose of IP protection. Providing other modified mask designs may also be useful.

[0057] In one embodiment, the first mask design includes a plurality of parallel metal line separated by spaces or dummy line patterns in a first or y direction. The metal line patterns may correspond to metal lines in a designated level. The metal lines, for example, comply with the design rules of the designated level. The design rules define, for example, minimum line width and space width, which equals to the minimum pitch. Additionally, there may be a minimum density of the line patterns. In one embodiment, the designated level may be the LB level. Other metal level may also be useful. In some embodiment, the metal lines may be created for the purpose of IP protection.

[0058] As for the second mask design, it may include a plurality of modified metal lines. The modified metal lines, for example, may take into consideration the data of the original vias of the VV level. The via design should comply with design rule requirements. The metal lines may be modified based on the information of the underlying vias and extending them to form metal lines in a second or x direction. The second direction, for example, is perpendicular to the first direction of the metal lines of the first mask. In one embodiment, the modified metal lines are extended to at least the width of the space or dummy line patterns of the first mask. Providing other extension amounts may also be useful.

[0059] In other embodiment, the second mask design includes metal lines. The metal lines, for example, are arranged in a second or x direction. In one embodiment, the metal lines should at least cover the vias of the VV level. Other configurations of the second mask design may also be useful. For example, the metal lines of the second mask design may be arranged in different directions to cover the vias.

[0060] At step 1030, the first and second mask designs are merged to produce a merged mask design. To provide the merged mask design, the first and second mask designs may be

overlaid. The merged mask design is further modified to provide a modified merged design at step 1040. In one embodiment, any spacing less than a minimum threshold is removed. For example, the minimum threshold may be less than the space width. Providing other minimum threshold in which spaces are removed may also be useful.

[0061] The modified merged mask design is then used to form a mask designated for IP protection at step 1050. In one embodiment, the modified merged mask design is applied to non-relevant chiplets of the LB mask. The modified merged mask design, as shown, shorts the vias in the VV level. Preferably, the modified merged mask design shorts all vias in the VV level. Applying the modified merged mask design to other masks of the MPW mask set may also be useful.

[0062] Figs. 11a-e show an embodiment of a process for implemented IP protection to non-relevant chiplets of a MPW mask. Referring to Fig. 11a, data related to non-relevant chiplets of a first mask 1110 is shown. The first mask includes a plurality of line patterns in a first direction. The line pattern, for example, includes parallel lines 1112 separated by spaces or dummy line patterns 1114 in a first or y direction. The metal line patterns, for example, may correspond to metal lines in a designated mask level. In one embodiment, the metal lines may be for the LB level. Other metal level may also be useful.

[0063] The metal lines should comply with the design rules of the level. The design rules define, for example, minimum line width of the lines and minimum space width for the spaces. The line width and space width is equal to the minimum pitch. The line pattern may be equal to the minimum line width while the spacing is greater than the minimum spacing. In addition, there may be a minimum density requirement of the line patterns. For example, the minimum line density may be 30%. An exemplary design rule for the LB level is listed in Table I below.

Table I

Line width	4 μm
Space width	2 μm
Density	30%

[0064] As shown, the first mask is provided with a line pattern in which the line width is about 4 μm with a line spacing of about 6 μm. This results in a line pitch of 10 μm. Providing other line widths and spacing widths may also be useful.

[0065] Fig. 11b shows a second mask pattern 1120. The second mask pattern, for example, comprises a modified metal line pattern 1124. For example, the modified metal lines may take into consideration the data of the original vias 1122 of a VV level. The pattern of the second mask should comply with the design rules. The width of the modified metal line, for example, may include the size of the via and 0.5 μm/edge in dimension. In one embodiment, the metal lines are modified based on the information of the underlying vias and extending them to form metal lines in a second or x direction. The second direction, for example, is perpendicular to the first direction of the metal lines of the first mask. In one embodiment, the modified metal lines are extended to at least the width of spacing or dummy line patterns of the first mask. Providing other extension amounts may also be useful.

[0066] In other embodiment, the second mask design includes metal lines. The metal lines, for example, are arranged in a second or x direction. In one embodiment, the metal lines should at least cover the vias of the VV level. Other configurations of the second mask design may also be useful. For example, the metal lines of the second mask design may be arranged in different directions to cover the vias.

[0067] Fig. 11c shows the pattern resulting from the merging of the first and second mask data of Figs. 11a-b. When the masks, for example, the LB masks, are merged, at least the vias 1122 of the VV level are covered by the merged metal lines to avoid defect generation, such as etch punch through.

[0068] The merged data of the first and second masks is further modified, as shown in Fig. 11d to produce a modified merged mask 1140. In one embodiment, the merged data is modified by removing spaces 1134 which are less than a threshold value. In one embodiment, the threshold value, for example, may be equal to the minimum space width. For example, in the case where the minimum space width is 2 μm, spaces which are less than 2 μm are removed. Providing other minimum threshold value may also be useful.

[0069] Fig. 11e shows an example of a modified merged mask 1140 under low magnification. As shown, the modified merged mask includes lines 1112 and spaces 1114 merged with modified metal lines 1124. Spaces 1134 which are less than the defined threshold value are removed.

[0070] Fig. 12 shows another embodiment of a non-relevant chiplet 1200 implemented with IP protection. As shown, the chiplet includes test pads or probe pads 1230. The test pads are used for testing or characterizing the device. The test pads may be provided at all metal levels. For example, different pads may be provided to test components or circuits 1220 of the chiplet. The pads may include conductive lines 1240 which couple the pads to the component to be tested. This allows probing and test on the pads.

[0071] In one embodiment, the test pads are shorted by a conductive line 1260. For example, all the test pads are electrically coupled by the conductive line 1260. The conductive line, for example, includes metal such as copper, aluminium, etc. Providing a conductive line with other types of materials may also be useful.

[0072] In some embodiments, some of the test pads are shorted or electrically coupled. Shorting test pads prevents characterizing the chiplet by non-IP owners. In one embodiment, test pad conductors are provided to electrically couple a plurality of test pads to render the test pads inoperable.

[0073] As described, IP protection may be used to protect IP of an IP provider, for example, in the context of MPW. The IP protection may be provided at different mask levels. The various IP protections described may be employed individually or in any combination. Additionally, the IP protection may be employed at any mask level, including multiple mask levels.

[0074] Fig. 13 shows a process flow 1300 of implementing IP protection for non-relevant chiplets on mask or masks of a MPW mask set. In one embodiment, it is determined that the MPW mask includes N number of IP providers at step 1310. The process is initialized. For example, X is initialized to a value of 1 at step 1320. At step 1330, a mask is selected for implementing IP protection. The selected mask is processed. For example, data of non-relevant chiplets in the selected mask is manipulated to implement IP protection at step 1340. At step 1350, X is incremented by 1.

[0075] At step 1360, it is determined whether the IP implementation for the selected mask has been completed. For example, it determines whether X is equal to the number of IP providers (X = N). In the event where X is not equal to N, the process returns to step 1340. Additional processing is performed to provide IP protection for other IP providers. For example, if there are two IP providers on the MPW mask, two iterations of IP protection is performed to provide two versions of the selected mask. One version protects the IP of the first IP provider and the other to protect the IP of the second IP provider. On the other hand, if X is equal to N, processing for IP protection is completed for the selected mask.

[0076] The process continues to step 1370 to determine if there is another mask which is selected for IP protection. If there is another mask selected for IP protection, the process returns to step 1320. On the other hand, if no other mask is selected for IP protection, IP protection implementation is completed at step 1380.

[0077] Figs. 14a-b show wafers 1400 which have been processed by masks implemented with IP protection. As shown, the wafers include devices 1405 formed by MPW masks having first and second chiplets 1410 and 1420 of first and second IP providers. For simplification, the wafer is shown with two devices. It is understood that the wafer may include other number of devices as well as the devices including other number of chiplets.

[0078] In Fig. 14a, the second chiplet is implemented with IP protection, as indicated by the shaded chiplet, while the first chiplet includes real data of the first IP owner. This processed wafer is delivered to the first IP owner for testing and evaluation. However, the IP of the second IP provider is protected from disclosure to the first IP provider due to IP protection. As for the wafer of Fig. 14b, the first chiplet is implemented with IP protection while the second chiplet includes real data of the second IP owner. This processed wafer is delivered to the second IP owner for testing and evaluation. However, the IP of the first IP provider is protected from disclosure to the first IP provider due to IP protection.

[0079] The MPW mask or reticle developed can be used to form semiconductor devices or integrated circuits (ICs). For example, the reticle can be used to pattern a substrate to form the features which serve as components on the substrate. The components are interconnected to form devices or ICs with the desired function. The substrate, for example, can be a wafer in which a plurality of devices or ICs are formed. After processing of the wafer is completed, the devices are diced, separating the wafer into individual dies. Continued processing can be performed, such as assembly, testing and packaging to complete forming the devices or ICs.

[0080] The invention may be embodied in other specific forms without departing from the spirit or essential characteristics thereof. The foregoing embodiments, therefore, are to be considered in all respects illustrative rather than limiting the invention described herein. Scope of the invention is thus indicated by the appended claims, rather than by the foregoing description, and all changes that come within the meaning and range of equivalency of the claims are intended to be embraced therein.

What is claimed is:

CLAIMS

1. A method of forming a device comprising:

providing a MPW mask having a plurality of chiplets pertaining to a plurality of IP owners, wherein non-relevant chiplet or chiplets of an IP owner are implemented with IP protection;

patterning a substrate using the MPW mask to form a device;

delivering the device to a relevant IP owner, the device includes the non-relevant chiplets of the IP owner, wherein IP protection reduces disclosure of IP information of the non-relevant chiplets to the relevant IP owner.

2. The method of claim 1 wherein the device is a prototype device used to define a final product.

3. The method of claim 1 wherein the IP protection is provided by modifying the non-relevant chiplet or chiplets of the IP owner.

4. The method of claim 3 wherein modifying the non-relevant chiplet or chiplets comprises:

manipulating mask data of non-relevant chiplet or chiplets.

5. The method of claim 4 wherein manipulating the mask data comprises an additive procedure or a substrative procedure or a combination thereof.

6. The method of claim 5 wherein the additive procedure includes adding data to an original mask data designed by the IP owner.

7. The method of claim 5 wherein the subtractive procedure includes removing data from an original mask data designed by the IP owner.

8. The method of claim 4 wherein manipulating the mask data includes modifying a mask of a via pad level, a pad level, a passivation layer level or a combination thereof.

9. The method of claim 8 wherein modifying the mask of the via pad level includes providing no via pattern or no via data to the non-relevant chiplet or chiplets.

10. The method of claim 8 wherein modifying the mask of the pad level includes providing a plurality of dummy via fill pattern to the non-relevant chiplet or chiplets.

11. The method of claim 8 wherein modifying the mask of the passivation layer level includes providing no opening pattern to the non-relevant chiplet or chiplets.

12. The method of claim 1 wherein the IP protection is provided by modifying mask designs of a mask level.

13. The method of claim 12 wherein modifying the mask design of the mask level includes:

providing first and second modified mask designs, wherein the first modified mask design includes a plurality of metal lines separated by spaces or dummy lines, and the second modified mask design taking into consideration data of an original via pattern of a via level; and

merging the first and second modified mask designs to form a modified merged mask.

14. The method of claim 1 wherein the chiplet includes a plurality of test pads and test components.

15. The method of claim 14 includes conductive lines which couple the test pads to the test components.

16. The method of claim 14 wherein the IP protection is provided by shorting the plurality of test pads.

17. The method of claim 16 wherein the plurality of test pads are shorted by a conductive line.

18. The method of claim 17 wherein the conductive line comprises copper or aluminium.

19. A method of forming a device comprising:

providing a MPW mask having a plurality of chiplets pertaining to a plurality of IP owners, wherein non-relevant chiplet or chiplets of an IP owner are implemented with IP protection;

patterning a substrate using the MPW mask to form a prototype device; and

delivering the prototype device to a relevant IP owner, the prototype device includes the non-relevant chiplets of the IP owner, wherein IP protection reduces disclosure of IP information of the non-relevant chiplets to the relevant IP owner; and

continue processing of the prototype device to form the desired function of the device.

20. A device comprising:

a substrate prepared by a MPW mask having a plurality of chiplets pertaining to a plurality of IP owners, wherein non-relevant chiplet or chiplets of an IP owner are implemented with IP protection.