CLAIMS

1. A semiconductor power device comprising:

a drain region;

a first region contacting said drain region and having a same conductivity type as a conductivity type of said drain region, said first region being more lightly doped compared to a doping of said drain region;

a source region;

a second region in contact with said first region and said source region;

a gate region;

a gate insulator layer positioned at least in part between said gate region and said second region;

a body electrode configured to provide bias to said second region; and

a source electrode configured to provide bias to said source region;

wherein said drain region is located below said first region;

wherein independent control of said second region and said source region are enabled.

2. The semiconductor power device of claim 1, wherein, when in a conducting mode, application of a positive voltage to said second region while about zero voltage is applied to said source region, results in a higher current flow from said drain region to said source region, compared to configurations where said second region is shorted to said source region.

3. The semiconductor power device of claim 1, wherein, when in a conducting mode, a positive voltage is applied to said gate region, a positive voltage is applied to said drain region, about zero voltage is applied to said source region, and a positive voltage is applied to said second region.

4. The semiconductor power device of claim 1, wherein a positive bias applied to said second region turns on an intrinsic lateral bipolar transistor, wherein said source region functions as an emitter region of the intrinsic lateral bipolar transistor, said second region

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functions as a base region of the intrinsic lateral bipolar transistor, and said first region and said drain region function as a collector region of said intrinsic lateral bipolar transistor.

5. The semiconductor power device of claim 1, wherein, when said semiconductor power device is turned off, a negative bias is applied to said second region.

6. The semiconductor power device of claim 1,

wherein said drain region comprises a substrate;

wherein said first region comprises a drift region; and

wherein said gate region and said gate insulator layer are formed inside a V-shaped groove cutting said source region, said second region, and into said drift region.

7. The semiconductor power device of claim 1,

wherein said drain region comprises a substrate;

wherein said first region comprises a drift region; and

wherein said gate region and said gate insulator layer are formed in a U-shaped trench.

8. The semiconductor power device of claim 1, wherein current flows vertically from said drain region to said source region in a conducting state.

9. The semiconductor power device of claim 1,

wherein said drain region comprises a substrate;

wherein said first region comprises a drift region having a same conductivity type as a conductivity type of said substrate and being more lightly doped than said substrate;

said semiconductor power device further comprising a vertical region in contact with said second region and said drift region, said vertical region having a different conductivity type from said conductivity type of said drift region.

10. A method of operating a semiconductor power device having a drain region, a first region contacting said drain region and having a same conductivity type as a conductivity type of said drain region and being more lightly doped than said drain region, wherein said drain

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region is located below said first region, a source region, a second region in contact with said first region and said source region, a gate region, a gate insulator layer positioned at least in part between said gate region and said second region, a body electrode configured to provide bias to said second region, and a source electrode configured to provide bias to said source region, said method comprising:

applying a first bias from said body electrode to said second region; and

applying a second bias from said source electrode to said source region;

wherein said first and second biases are independently controlled.

11. The method of claim 10, wherein said method includes turning on said semiconductor power device by applying a positive voltage to said gate region and a positive voltage to said drain region,

wherein the applying said second bias includes applying a bias of about zero voltage, and

wherein the applying said first bias includes applying a positive voltage;

wherein a higher current flow from said drain region to said source region results, compared to if said body electrode had been grounded.

12. The method of claim 10, wherein the applying said first bias to said second region includes turning on an intrinsic lateral bipolar transistor where said source region functions as an emitter region, said second region functions as a base region, and said first region and drain region function as a collector region of the intrinsic lateral bipolar transistor.

13. A method of operating a semiconductor power device having a drain region, a first region contacting said drain region and having a same conductivity type as a conductivity type of said drain region and being more lightly doped than said drain region, a source region, a second region in contact with said first region and said source region, a gate region, a gate insulator layer positioned at least in part between said gate region and said second region, a body electrode configured to provide bias to said second region, and a source electrode configured to provide bias to said source region, said method comprising:

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applying a negative bias to said second region when turning off said semiconductor power device.

14. The method of claim 13, wherein said applying said negative bias to said second region includes reducing a leakage current between said drain region and said source region when said semiconductor power device is turned off.

15. The method of claim 13, wherein said applying said negative bias to said second region includes improving a switch-off time of said semiconductor power device.

16. The method of claim 13, further comprising applying a negative bias to said gate region in conjunction with said applying said negative bias to said second region.

17. The method of claim 13, wherein said applying said negative bias includes applying a negative voltage bias.

18. The method of claim 13, wherein said applying said negative bias includes applying a negative current bias.

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