3D INTEGRATED CIRCUIT PACKAGE AND METHOD OF FABRICATION THEREOF

ABSTRACT

A method of fabricating a 3D integrated circuit structure comprising the steps of: providing a wafer having a plurality of wafer integrated circuits formed thereon, each of said wafer integrated circuits being provided with a plurality of wafer contact elements; providing a plurality of die elements, each of said die elements being configured to be connected electrically to one of said wafer integrated circuits, said die elements each having a plurality of die contact elements; with the die elements at respective predetermined locations on the surface of the wafer the locations of the die contact elements corresponding to locations of said wafer contact elements of the wafer integrated circuits; providing a positioning member in predetermined juxtaposition with said wafer, the positioning member having a plurality of formations at locations of the positioning member corresponding to locations of said plurality of wafer integrated circuits, said formations defining respective sets of lateral boundaries arranged to constrain movement of respective die elements when provided on said wafer such that respective corresponding contact elements of the wafer integrated circuits and die elements are aligned with one another, the method further comprising the step of placing each one of a plurality of die elements on said wafer within one of a set of respective lateral boundaries defined by said formations, and bonding said die elements to said wafer.

(FIG. 1)