

**TIME MULTIPLEXING PIXEL FRAME BUFFER VIDEO OUTPUT
ABSTRACT OF THE DISCLOSURE**

A method and apparatus for multiplexing pixel data from a frame buffer to a RAMDAC to reduce the number of pins required. For many graphics operations optimal performance is achieved by storing an entire 32-bit pixel in a single RAM chip. When displaying video data from a frame buffer, pixels must be read out serially from the frame buffer at real-time speeds. A frame buffer memory with 16 pins for serial video output is used. An entire 32-bit pixel is stored in a single RAM chip. For a 32-bit pixel containing four byte (8-bit) quantities designated X, B, G and R, on the first clock cycle, the X and B bytes are made available on the 16 pins of the frame buffer. On the next clock cycle, the G and R bytes are made available. Thus, over two cycles the entire 32-bit pixel is output from the frame buffer to a RAMDAC which samples the X and B bytes on 16 input pins. The RAMDAC stores these X and B bytes in an internal register. On the next clock cycle it samples the G and R bytes. The DAC then reassembles the X, B, G and R bytes into a single 32-bit pixel for conversion into video. In this manner, 32-bit pixels are communicated across a 16-bit pixel data bus.

(Figure 3)