A METHOD OF REACQUIRING CLOCK SYNCHRONIZATION ON A NON-TRACKING HELICAL SCAN TAPE DEVICE

Field of the Invention

The present invention pertains generally to magnetic tape drives, and more particularly to a method of reacquiring clock synchronization in a non-tracking helical scan tape device.

Related Patents

The present invention is related to co-pending U.S. patent application entitled "Method And Apparatus For Logically Rejecting Previously Recorded Track Residue From Magnetic Media", invented by McAuliffe et al., and having an internal docket number of 9086/103 and a serial number of 09/192,794, filed concurrently herewith on November 16, 1998, and co-pending U.S. patent application entitled "Method And System For Monitoring And Adjusting Tape Position Using Control Data Packets", invented by McAuliffe et al., and having an internal docket number of 9086/107 and a serial number of 09/193,030, filed concurrently herewith on November 16, 1998, and co-pending U.S. patent application entitled "Rogue Packet Detection And Correction Method For Data Storage Device", invented by McAuliffe et al., and having an internal docket number of 9086/105 and a serial number of 09/192,809, filed concurrently herewith on November 16, 1998, and co-pending U.S. patent application entitled "Variable Speed Recording Method and Apparatus for a Magnetic Tape Drive", invented by Beavers et al., and having an internal docket number of

9086/101 and a serial number of 09/176,079, filed on October 20, 1998, and co-pending U.S. patent application entitled "Overscan Helical Scan Head for Non-Tracking Tap Subsystems Reading at up to 1X Speed and Method for Simulation of Same", invented by Blatchley et al., and having an internal docket number of 9086/104 and a serial number of 09/176,013, filed on October 20, 1998, and co-pending U.S. patent application entitled "Fine Granularity Rewrite Method and Apparatus for Data Storage Device", invented by Zaczek, and having an internal docket number of 9086/106 and a serial number of 09/176,015, filed on October 20, 1998, and co-pending U.S. patent application entitled "Multi-level Error Detection and Correction Technique for Data Storage Recording Device", invented by McAuliffe et al., and having an internal docket number of 9086/102 and a serial number of 09/176,014, filed on October 20, 1998, all of which are commonly owned and all of which are hereby incorporated by reference.

Background of the Invention

A traditional magnetic storage device relies on a track-following architecture in which the tape drive attempts to follow a previously written track when reading it back by maintaining a very precise alignment between the path traced by the read heads and the written tracks on a tape.

In a track-following architecture, the read channel circuitry employs a phase locked loop (PLL) which locks a synchronization clock signal to the read signal (i.e., the incoming data from the read heads) in order to properly perform track packet detection. In track-following storage devices, the PLL acquires lock

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of the clock synchronization signal once at the beginning of the read session, and maintains lock for the entire session.

Recently, non-track-following storage devices have been developed. In these non-tracking storage devices, the previously written track is not followed continuously. Instead the read head may begin on one track and drift over to an adjacent track during the read operation. In this situation, the read signal will degrade during the crossover period, and clock synchronization may be lost. If the frequency of the clock synchronization signal drifts too far during this crossover period, it will prevent reacquisition of lock when approaching the next adjacent track. A similar effect can happen when reading through a long magnetic defect on the tape.

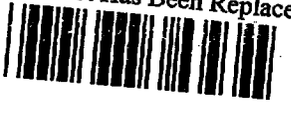
It is difficult to reliably detect when the read heads are deviating from a track based solely on the read head signal amplitude. If the read head is partially over the track that it is departing from, and in addition is partially over an adjacent track being approached, the overall signal amplitude may not be detectably reduced. However, the signal quality would prevent the data from either track from being successfully read.

Accordingly, a need exists for a method for detecting when a read head is moving off track and for reacquiring clock synchronization in a non-tracking storage device when the read head moves off track.

Summary of the Invention

The present invention is a novel method of reacquiring clock synchronization in a non-tracking storage device when the quality of the read

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signal goes below a predetermined threshold. In accordance with the invention, the packet error detection status is monitored. During a normal successful read, a phase locked loop (PLL) receives the read signal comprising data recovered from the tape. A read quality detector utilizes the packet error detection status to determine whether the read packet error count exceeds a predetermined error count threshold. When the error threshold is reached or exceeded, the read channel is disabled and PLL is relocked to a reference frequency. The read channel is then re-enabled and the process repeated to monitor whether the read head is on or off track.

In accordance with one embodiment of the invention, if the packet decoder detects one or more good packets, the quality of the read signal is considered to be acceptable. If subsequently no good packets out of a predetermined number of subsequent recovered packets are detected, the quality of the read signal is considered unacceptable. This may be caused because the read head is off track or over a defect region of the tape. The read quality detector compares the read packet error count to a predetermined error count threshold. When the error threshold is reached or exceeded, the read quality detector shuts down the read channel, switches the input to the PLL from the read signal to known reference frequency, and waits a predetermined amount of time in order for the PLL to relock to the reference frequency. At the end of the wait period, the read quality detector re-enables the read channel and switches the input to the PLL back to the read signal.

Brief Description of the Drawing

The invention will be better understood from a reading of the following detailed description taken in conjunction with the drawing in which like reference designators are used to designate like elements, and in which:

FIG. 1 is a block diagram of a read channel for a magnetic recording system;

FIG. 2(a) is a side view of a portion of tape comprising a plurality of tracks illustrating a read head that is on track;

FIG. 2(b) is a timing diagram illustrating the recovery of data when the read head is on track;

FIG. 3(a) is a side view of a portion of tape comprising a plurality of tracks illustrating a read head that is off track;

FIG. 3(b) is a timing diagram illustrating the recovery of data when the read head is off track;

FIG. 4 is a block diagram of one embodiment of a clock synchronization signal reacquisition system in accordance with the invention;

FIG. 5 is a block diagram of one embodiment of a read quality detector circuit for determining whether clock synchronization reacquisition should be reacquired; and

FIG. 6 is a flowchart illustrating one embodiment of a method in accordance with the invention for determining whether clock synchronization should be reacquired.

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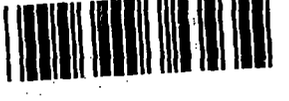
Detailed Description

A novel method for detecting when the read head is drifting off track in a non-tracking storage device and for reacquiring clock synchronization after the read head has moved off track is described in detail hereinafter. The invention is described in the context of a helical scan tape drive, but those skilled in the art will appreciate that the method of the invention may be applied in any non-tracking storage device.

FIG. 1 is a block diagram of a read channel 10 for a magnetic recording system. Read channel 10 comprises an electromagnetic read head 12 having means for detecting the magnetic fields stored by the particles on a magnetic media such as tape 2 and for converting the received electromagnetic signals to electronic signals. A preamplifier 14 then receives the electronic signal from read head 12, which is typically in the mV range, and amplifies it typically to the hundreds of mV range. A filter/equalizer 16 receives the amplified signal from preamplifier 14 to equalize the channel response and filter out unwanted noise. A peak detector 18 generates a digital pulse train from the equalized output of equalizer 16. The digital pulse train is phase locked to a synchronization clock signal SYNC by phase locked loop (PLL) 20, and then decoded into packets by packet decoder 22.

FIG. 2(a) is a side view of a portion of tape 2 comprising a plurality of tracks 4a, 4b, 4c, illustrating the position of read head 12 at three different times t1, t2, t3, when it is aligned completely over a given track 12b, hereinafter referred to as "on track". As illustrated, at each subsequent moment in time, t1,

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t2 and t3, read head 12 is completely aligned over track 4b. This configuration lends itself to the suitability of frequency-mode clock synchronization as described with reference to FIG. 2(b).

FIG. 2(b) is a timing diagram illustrating the recovery of an example DATA pattern "1000101000101" from tape 2 when the read head is on track. During the recording of the data pattern DATA to tape, it was clocked out to the tape by the drive's write channel one bit per fixed interval in time (e.g., 58.5 Mbits/sec). A binary bit value of "1" results in an analog pulse being written to tape. This is accomplished by creating a magnetic field that alternates the polarity of the magnetic particles on the tape 2. When a binary bit value of "0" is written to tape 2, the magnetic polarity of the last binary "1" is maintained. During data recovery, peak detector 18 receives the analog read signal READ_SIGNAL, detects the analog pulse peaks to determine when a binary one occurs, and generates a digital pulse for each detect analog pulse peak. Accordingly, when reading back data pattern DATA from tape 2, digital pulse train READ_PULSE comprises a digital pulse aligned with each peak detected from analog read signal READ_SIGNAL. With this methodology, the location of binary "1"s is easily detectable; however, the number of binary "0"s in between each binary "1" is not easily detectable because there are no detectable signal separators between adjacent binary "0"s.

Accordingly, a clock synchronization signal SYNC is phase-locked to the data pulse train READ_PULSE by PLL 20. When data is recovered from tape 2, the clock synchronization signal SYNC is locked to the frequency of the data by

PLL 20. Various methods are known in the art to provide phase-lock of a synchronization signal to an incoming data signal.

FIG. 3(a) is a side view of a portion of tape 2 comprising a plurality of tracks 4a, 4b, 4c, illustrating the position of read head 12 at three different times t1, t2, t3, when the read head 12 is not tracking. As illustrated, at time t1, read head 12 is completely aligned over track 4b. At time t2, read head 12 has drifted towards adjacent track 4c, and is positioned approximately half over track 4b and half over track 4c. At time t3, read head 12 has drifted even further away from track 4b such that it is positioned completely over adjacent track 4c.

In this embodiment, as is a typical occurrence in a non-tracking storage device, the read head 12 drifts across two or more adjacent tracks during a single pass of the read head 12 over the tape 2. When the position of the read head 12 is only partially over or is completely off of a particular track, it is considered to be "off track" with respect to that particular track. As the amount of signal amplitude detected by the read head, and hence the ratio of detected signal to actual signal, reduces, the signal quality and hence data reliability degrades.

FIG. 3(b) is a timing diagram illustrating the degradation of the read signal READ_SIGNAL as the read head 12 drifts off track. As with track-following architecture drives, when the data pattern DATA was recorded onto tape 2, it was clocked out to the tape by the drive's write channel one bit per fixed interval in time.

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When the read head 12 is on track, as illustrated in FIGS. 2(a) and 2(b), the analog read signal READ_SIGNAL is clean and has suitable amplitude for each analog pulse as illustrated in FIG. 2(b). Accordingly, the clock synchronization signal SYNC follows the frequency F1 of the data. If the read head moves off track, however, such as at time t2 in FIG. 3(a), the analog read signal READ_SIGNAL begins to deteriorate, as shown in FIG. 3(b) at 25 with extra perturbations and noisy peaks. If the analog read signal READ_SIGNAL deteriorates too far, the PLL 20 loses lock and drifts in frequency. When the PLL loses lock, the clock synchronization signal SYNC cannot follow the data, resulting in unknown locations of the binary "0"s. As the read head 12 keeps moving off a track (e.g., 4b) and approaches the next track (e.g., 4c), the PLL 20 needs to lock back onto the data pulse train READ_PULSE generated by peak detector 18 from data recovered from the next track 4c. However, if during the crossover (e.g., at time t2) between adjacent tracks (e.g., 4b and 4c) the PLL 20 loses lock and the frequency of the clock synchronization signal SYNC drifts too far (illustrated at F2), the PLL 20 can never reacquire lock of the clock synchronization signal SYNC.

FIG. 4 is a block diagram of one embodiment of a system 40 for reacquiring clock signal synchronization implemented in accordance with the invention. In system 40 PLL 20 locks the clock synchronization signal SYNC 58 to one of either the digital read signal READ_PULSE 60 or a reference frequency signal REF 54 that is preferably equal to the standard recording frequency of the drive. A switch 45 receives both of, and outputs one of, read

signal READ_PULSE 60 and reference frequency signal REF 54 in response to a select signal. In the preferred embodiment, the select signal is a read gate signal READ_GATE 52 that is also used to control the timing of the read head signal with respect to the position of the read head 12 over the tape 2. The output of switch 45 serves as the input signal of PLL 20 to which the clock synchronization signal SYNC 58 is locked.

Read gate signal READ_GATE 52 is a read head enable signal. When read gate signal READ_GATE 52 is asserted, read head 12 reads data from the tape. When read gate signal READ_GATE 52 is deasserted, read head 12 is disabled from reading data from the tape 2, or in the alternative, data detected by read head 12 when READ_GATE 52 is deasserted is simply ignored.

System 40 also includes a read quality detector 42, which may be implemented in hardware, software, or a combination of both. Read quality detector 42 monitors a packet status 56 and controls the state of read gate signal READ_GATE 52 according to a set of rules, discussed hereinafter.

Packet decoder 22 includes a packet reconstruction circuit 48 and packet error detection and/or correction logic 46. Packet reconstruction circuit 48 extracts each incoming data bit from digital pulse train READ_PULSE 60 in synchronization with the clock synchronization signal SYNC 58 to reconstruct each data packet coming off the tape 2. Packet error detection and/or correction logic 46 detects and/or corrects errors in the reconstructed packet 55 and indicates a status 56 of the reconstructed packet 55. The packet status 56 may be stored in one or more registers (not shown) that are accessed by read

quality detector 42, or may be sent as a signal or signals to read quality detector 42.

Read quality detector 42 monitors the packet status 56 for each detected packet and determines whether read head 12 is on or off track. During an off track condition, the packet error detection/correction logic 46 detects a lot more packet errors. This fact is used in the invention to ascertain whether the read head 12 is on or off track.

FIG. 5 is a block diagram of one embodiment of a read quality detector 42 for monitoring the quality of the read signal received from the read head. In this embodiment, packet status signal 56 is a signal GOOD_PACKET that pulses logically high if the reconstructed packet 55 is error free; packet status signal GOOD_PACKET remains a logical low if the packet error detection/correction logic 46 detects an error in reconstructed packet 55. Read quality detector 42 comprises a counter 80 that receives a reconstructed packet clock PACKET_CLK that pulses once each time packet reconstructor 58 reconstructs a packet 55. Counter 80 has a reset input RESET that receives packet status signal GOOD_PACKET. In operation, counter 80 increments once for each PACKET_CLK signal pulse. If no errors are detected in reconstructed packet 55, packet status signal GOOD_PACKET will also pulse, thereby clearing the count value of counter 80 to zero. Accordingly, when the read head is on track and good (i.e., error-free) packets are being detected, the count value in counter 80 will generally remain at or close to zero. However, as the read head moves off track, or when the read head passes over a magnetic

defect on tape, the quality of the signal degrades and the number of detected packet errors increases. Accordingly, GOOD_PACKET signal does not reset counter 80, and therefore the count value in counter 80 increases.

Read quality detector 42 includes a comparator 82 which compares the count value in counter 80 to a predetermined error count threshold ERROR_THRESHOLD. In the illustrative embodiment, ERROR_THRESHOLD is set to five such that clock synchronization is reacquired each time the packet error correction/detection logic 46 detects five consecutive "bad" packets.

Comparator 82 monitors the count value in counter 80, which represents the total number of consecutive packets that contained errors since the last good packet was seen by the read head. If the count value exceeds the predetermined error count threshold ERROR_THRESHOLD, the read gate signal READ_GATE 52 is deasserted, thereby disabling the read channel and switching the input to PLL 20 the input to PLL 20 to the reference frequency REFERENCE, causing PLL 20 to relock to reference frequency REFERENCE. In the preferred embodiment, REFERENCE is preferably the recording frequency of the drive. Read quality detector 42 causes the select signal READ_GATE 52 to remain deasserted for a period of time long enough to allow the PLL 20 to relock to the reference frequency REFERENCE. In the illustrative embodiment, this amount of time is the equivalent of the amount of time it takes the read channel packet reconstructor 48 to reconstruct one-and-a-half packets.

Once PLL 20 is relocked to the reference frequency REF, the read gate signal READ_GATE 52 is reasserted and the packet errors are once again

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monitored to determine whether the read head 12 is on or off track. The process is repeated each time the packet error detection logic 46 detects an error in a number of consecutive reconstructed packets that matches the error threshold ERROR_THRESHOLD.

FIG. 6 is a flowchart of one embodiment of the method performed by read quality detector 42. In a step 602, the count value in counter 80 is cleared to zero and the clock synchronization signal is locked to the reference frequency, preferably the standard recording frequency of the storage device. This is accomplished by switching the input to the PLL 20 to the reference frequency REFERENCE and waiting long enough (in the illustrative embodiment, one-and-a-half packet clock cycle periods) for the PLL 20 to achieve lock. The read channel is enabled in step 604. This is accomplished by asserting the read gate signal READ_GATE 52, which starts up the digital read pulse train READ_PULSE again. The assertion of read gate signal READ_GATE 52 also switches the input to the PLL 20 to the read pulse train READ_PULSE 60 to allow PLL 20 to attempt to lock on the data itself. A packet is reconstructed and the count value is incremented in step 606. Error detection is performed on the reconstructed packet in step 608. If no error is detected in the packet, the counter 80 is reset and the count value is cleared to zero in step 610. Another packet is processed and steps 606 through 608 are then repeated. If an error is detected in the reconstructed packet, however, in step 612, the count value is compared to a predetermined error count threshold.

If the error count is less than the error count threshold, another packet is processed and steps 606 through 612 are repeated.

If the error count meets or exceeds the predetermined error count threshold, reacquisition of clock synchronization is triggered. This is accomplished by shutting down the read channel and switching the input of the PLL 20 to receive the reference frequency REFERENCE in step 614. In the illustrative embodiment, the read channel is shut down by deasserting read gate signal READ_GATE 52. A predetermined delay passes in step 616 to allow the PLL 20 to acquire lock on the reference frequency. Counter 80 is then cleared in step 618, and the read channel is started back up again with step 604. The process repeats continuously while the storage device is reading data from the tape.

It will be appreciated by those skilled in the art that the method for determining the quality of the read signal via the packet error status may be otherwise variously embodied without deviating from the scope and spirit of the invention, and that the method presented herein is by way of illustration only and not limitation.

Although the invention has been described in terms of the illustrative embodiments, it will be appreciated by those skilled in the art that various changes and modifications may be made to the illustrative embodiments without departing from the spirit or scope of the invention. It is intended that the scope of the invention not be limited in any way to the illustrative embodiment

shown and described but that the invention be limited only by the claims appended hereto.

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WHAT IS CLAIMED IS:

1. A read quality detector (42) for detecting the quality of a read signal (60) in a non-tracking storage device, said non-tracking storage device comprising a packet error detector (46) which detects an error in a packet (55) and generates a packet error status (56) indicative of whether or not an error was detected in said packet (55), said read quality detector (42) comprising:

a packet error status monitor (80, 82) which monitors said packet error status (56) over a predetermined number of a plurality of consecutive packets (55) reconstructed from said read signal (60) and generates a read quality signal (52) indicative of the quality of said read signal (60) based on the number of said plurality of consecutive packets (55) in which an error was detected.

2. A read quality detector in accordance with claim 1, comprising:

a counter (80) which maintains a packet error count, said packet error count representing said number of said plurality of consecutive packets (55) in which an error was detected; and

a comparator (82) which compares said packet error count to an error count threshold (ERROR_THRESHOLD) to generate said read quality signal (52).

3. A clock synchronization reacquisition apparatus (40) for a non-tracking storage device comprising a read channel which generates a read signal (60) based on detection of data from a storage medium in said non-

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tracking storage device and which reconstructs data packets (55) from said read signal (60), comprising:

a read quality detector (42) which monitors a packet error status (56) associated with each of a respective one of a predetermined number of a plurality of consecutive packets (55) reconstructed from said read signal (60), said packet error status (56) indicative of whether or not an error was detected in said reconstructed packet (55) associated with said packet error status (56), said read quality detector (42) generating a read quality signal (52) indicative of the quality of said read signal (60) based on the number of said plurality of consecutive packets (55) in which an error was detected;

a phase locked loop (PLL) (20) which receives an input signal (60, 54) and generates a clock synchronization signal (58) that is locked to said input signal (54, 60); and

a switch (45) which receives said read signal (60) and a reference frequency signal (54) and outputs one or the other of said read signal (60) or said reference frequency signal (54) as said input signal of said PLL (20) in response to said read quality signal (60).

4. A clock synchronization reacquisition apparatus in accordance with claim 3, comprising:

a packet error detector (46) which detects an error in a reconstructed packet (55) and generates said packet error status (56) indicative of whether or not an error was detected in said reconstructed packet (55).

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5. A clock synchronization reacquisition apparatus in accordance with claim 3, wherein:

said read quality detector comprises:

a counter (80) which maintains a packet error count, said packet error count representing said number of said plurality of consecutive packets (55) in which an error was detected; and

a comparator (82) which compares said packet error count to an error count threshold (ERROR_THRESHOLD) to generate said read quality signal (52).

6. A method for reacquiring synchronization of a clock synchronization signal (58) with a data signal (60) in a non-tracking storage device, said non-tracking storage device comprising a read channel (10), said read channel (10) comprising a read head (12) which generates a data signal based on detection of data from a storage medium (2) in said non-tracking storage device, a phase locked loop (PLL) (20) which locks receives one of either a reference frequency (54) or said data signal (60) and generates said clock synchronization signal (58) locked to said one of either said reference frequency (54) or said data signal (60), and a packet reconstructor (48) which reconstructs data packets (55) from said data signal (60) in synchronization with said clock synchronization signal (58), said method comprising:

switching (604) said PLL to receive said data signal (60);

monitoring (608) a packet error status (56) associated with each of a respective one of a predetermined number of a plurality of consecutive packets (55) reconstructed from said read signal (60), said packet error status (56) indicative of whether or not an error was detected in said reconstructed packet (55) associated with said packet error status (56);

detecting (612) an unacceptable read quality condition, said unacceptable read quality condition based on the number of said plurality of consecutive packets in which an error was detected; and

upon detection of said unacceptable read quality condition:

switching (614) said PLL to receive said reference frequency;

locking (614) said clock synchronization signal to said reference frequency; and

repeating said method.