

Claims

1. A die comprising:

a processor including a first side, a second side, a third side opposite the first side, and a fourth side opposite the second side;

a first input/output (I/O) tile adjacent to the second side of the processor, wherein the first I/O tile is communicatively coupled with the processor, the first I/O tile includes a first edge and a second edge opposite the first edge, the first edge is aligned to the first side of the processor and the second edge extends beyond the third side of the processor; and

a second I/O tile adjacent to the third side of the processor, wherein the second I/O tile is communicatively coupled with the processor, the second I/O tile includes a third edge and a fourth edge opposite the third edge, the third edge is aligned to the second side of the processor and the fourth edge extends beyond the fourth side of the processor.

2. The die of claim 1, wherein the first I/O tile is to facilitate transmission of an electronic signal between the processor and another component of an electronic device to which the die is communicatively coupled.

3. The die of claim 1, wherein the processor is a processor core.

4. The die of claim 1, further comprising a second processor adjacent to the first I/O tile, wherein the first I/O tile is further communicatively coupled with the second processor.

5. The die of claim 1 comprising a third I/O tile adjacent to the fourth side of the processor, wherein the third I/O tile is communicatively coupled with the processor, the third I/O tile includes a fifth edge and a sixth edge opposite the fifth edge, the fifth edge is aligned to the third side of the processor and the sixth edge extends beyond the first side of the processor.

6. A die comprising:

a substrate;

a processor core coupled with the substrate, the processor core including a first side, a second side, a third side opposite the first side, and a fourth side opposite to the second side;

a first input/output (I/O) tile coupled with the substrate adjacent to the second side of the processor core, wherein the first I/O tile is communicatively coupled with the processor core by a first bridge, the first I/O tile includes a first edge and a second edge opposite the first edge, the first edge is aligned to the first side of the processor core and the second edge extends beyond the third side of the processor core; and

a second I/O tile coupled with the substrate adjacent to the third side of the processor core, wherein the second I/O tile is communicatively coupled with the processor core by a second bridge, the second I/O tile includes a third edge and a fourth edge opposite the third edge, the third edge is aligned to the second side of the processor core and the fourth edge extends beyond the fourth side of the processor core.

7. The die of claim 6, wherein the first bridge is an embedded multi-die interconnect bridge (EMIB).

8. The die of claim 7, wherein the EMIB is in the substrate.

9. The die of claim 6, further comprising a second processor core coupled with the substrate, wherein the second processor core is communicatively coupled with the first I/O tile by a third bridge.

10. The die of claim 6, wherein the first I/O tile is to facilitate communication between the processor core and a component to which the die is communicatively coupled.

11. The die of claim 10, wherein the second I/O tile is to facilitate communication between the processor core and the component.

12. The die of claim 6 comprising a third I/O tile adjacent to the fourth side of the processor, wherein the third I/O tile is communicatively coupled with the processor core, the third I/O tile includes a fifth edge and a sixth edge opposite the fifth edge, the fifth edge is aligned to the third side of the processor core and the sixth edge extends beyond the first side of the processor core.

13. An electronic device comprising:

a printed circuit board (PCB); and

a die coupled with the PCB, wherein the die includes:

a processor core including a first side, a second side, a third side opposite the first side, and a fourth side opposite to the second side;

a first input/output (I/O) tile adjacent to the second side of the processor core, wherein the first I/O tile is communicatively coupled with the processor core and is to facilitate communication between the processor core and the PCB, the first I/O tile includes a first edge and a second edge opposite the first edge, the first edge is aligned to the first side of the processor core and the second edge extends beyond the third side of the processor core; and

a second I/O tile adjacent to the third side of the processor core, wherein the second I/O tile is communicatively coupled with the processor core and is to facilitate communication between the processor core and the PCB, the second I/O tile includes a third edge and a fourth edge opposite the third edge, the third edge is aligned to the second side of the processor core and the fourth edge extends beyond the fourth side of the processor core.

14. The electronic device of claim 13, wherein the first I/O tile is communicatively coupled with the processor core by an embedded multi-die interconnect bridge (EMIB).

15. The electronic device of claim 14, wherein the second I/O tile is communicatively coupled with the processor core by the EMIB.

16. The electronic device of claim 14, wherein the second I/O tile is communicatively coupled with the processor core by a second EMIB.

17. The electronic device of claim 13 comprising a third I/O tile adjacent to the fourth side of the processor, wherein the third I/O tile is communicatively coupled with the processor core, the third I/O tile includes a fifth edge and a sixth edge opposite the fifth edge, the fifth edge is aligned to the third side of the processor core and the sixth edge extends beyond the first side of the processor core.