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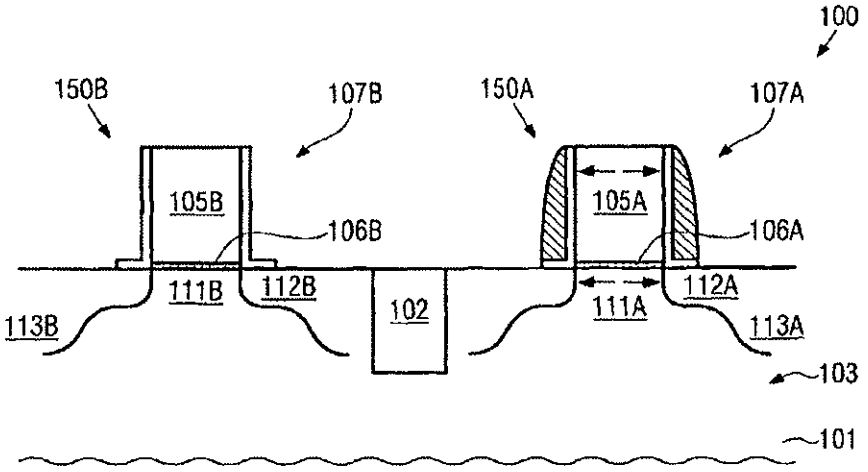
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(54) Title: METHOD FOR FORMING A STRAINED TRANSISTOR BY STRESS MEMORIZATION BASED ON A STRESSED IMPLANTATION MASK



(57) Abstract: By using an implantation mask having a high intrinsic stress, stress memorization technique (SMT) sequences may be provided in which additional lithography steps may be avoided. Consequently, a strain source may be provided without significantly contributing to the overall process complexity.

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