

CLAIMS

[Claim 1]- A semiconductor device comprising:

a substrate;

a first semiconductor element disposed on the substrate;

5 a first sealing layer disposed to cover a region in which the first semiconductor element is disposed in the substrate and sealing the first semiconductor element; and

a second semiconductor element disposed to cover a surface in the first sealing layer opposite to the side of the substrate and having a larger area than an area of the first semiconductor element, wherein

10 the first sealing layer is composed of a cured product of a thermosetting resin composition and a melt viscosity ~~at 120°C~~ of the thermosetting resin composition is ~~2500~~5000 to 11500 Pa·s at 120°C.

[Claim 2]- The semiconductor device according to claim 1, wherein
15 the thermosetting resin composition contains a low-molecular-weight component having a molecular weight of 10 to 1000 and a high-molecular-weight component having a molecular weight of 100000 to 1000000,

a content M1 of the low-molecular-weight component is 23 to
20 35 parts by mass with respect to 100 parts by mass of a mass of resin components contained in the thermosetting resin composition, and

a content M2 of the high-molecular-weight component is 25 to 45 parts by mass with respect to 100 parts by mass of the mass of resin components contained in the thermosetting resin composition.

25 [Claim 3]- The semiconductor device according to claim 2, wherein a total amount of the low-molecular-weight component and the

high-molecular-weight component is 54 to 76 parts by mass with respect to 100 parts by mass of the mass of resin components contained in the thermosetting resin composition.

[Claim 4]- The semiconductor device according to any one of claims 1 to 3, further comprising:

a circuit pattern formed on a surface of the substrate; and

a first wire electrically connecting the first semiconductor element and the circuit pattern to each other.

[Claim 5]- The semiconductor device according to claim 4, further comprising:

a second wire electrically connecting the second semiconductor element and the circuit pattern to each other; and

a second sealing layer sealing the second semiconductor element and the second wire.

[Claim 6]- The semiconductor device according to any one of claims 1 to 5, further comprising a third semiconductor element stacked above the second semiconductor element.

[Claim 7]- A thermosetting resin composition being used in a manufacturing process of a semiconductor device,

the manufacturing process including a step of performing a curing treatment in which the thermosetting resin composition is heated and bringing at least one of at least a part of a wire and a semiconductor element into a state of being embedded in the thermosetting resin composition after the curing treatment, wherein

a melt viscosity at ~~120°C~~ of the thermosetting resin composition is ~~2500~~5000 to 11500 Pa·s at 120°C.

[Claim 8]- The thermosetting resin composition according to claim 7, comprising:

a low-molecular-weight component having a molecular weight of 10 to 1000; and

5 a high-molecular-weight component having a molecular weight of 100000 to 1000000, wherein

a content M1 of the low-molecular-weight component is 23 to 35 parts by mass with respect to 100 parts by mass of a mass of resin components contained in the thermosetting resin composition, and

10 a content M2 of the high-molecular-weight component is 25 to 45 parts by mass with respect to 100 parts by mass of the mass of resin components contained in the thermosetting resin composition.

[Claim 9]- The thermosetting resin composition according to claim 8, wherein a total amount of the low-molecular-weight component and
15 the high-molecular-weight component is 54 to 76 parts by mass with respect to 100 parts by mass of the mass of resin components contained in the thermosetting resin composition.

[Claim 10]- A dicing-die bonding integrated tape comprising:

a pressure-sensitive adhesive layer; and

20 an adhesive layer composed of the thermosetting resin composition according to any one of claims 7 to 9.