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COMPLETE SPECIFICATION

Method of Forming Patterns in Epitaxial Layers of Semiconductor and Devices Made thereby

We FAIRCHILD CAMERA AND INSTRUMENT CORPORATION of 300 Robbins Lane, Syosset, Long Island, New York, United States of America, a corporation organized and existing under the laws of the State of Delaware, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

The invention relates to a new method of forming patterns within epitaxial layers of semiconductor material; new devices are made by this method. In particular, the invention provides a method of forming regions within an epitaxial layer by diffusion out from a substrate either during or subsequent to the epitaxial growth. New devices including isolation regions, improved epitaxial transistors, and isolated epitaxial transistors are made by the method of this invention.

The recent trend in the semiconductor industry is towards integrated semiconductor circuitry. Integrated semiconductor circuits have more than one semiconductor device built into the same block of semiconductor material. Often a large number of such devices are so integrated, thereby achieving a substantial reduction in overall size of the circuit. In integrated circuits it is often essential that each semiconductor device be electrically isolated from the rest. In the past, an isolating region was sometimes diffused transversely through a wafer of semiconductor material of the opposite conductivity type to form two isolated regions upon opposite sides of the isolating region. The junctions between the isolated regions and the isolating region may be reverse-biased to provide more complete electrical isolation, or the isolating region may be left floating without an electrical connection to it.

There are two severe problems with this method of isolation. First, the diffused impurities of the isolating region not only diffuse transversely with respect to the wafer, but also diffuse laterally within it. This concomitant lateral diffusion cannot be prevented. It causes a portion of the final isolating region to be considerably wider than it was initially. This unnecessary width uses up valuable space on the block of semiconductor material. Because of it, a larger area must be allocated to each isolating region.

Second, when the isolating region is diffused completely through the substrate, a large junction is formed. If the junction is reverse-biased for improved isolation, a capacitance is created in the area of the junction. Where the junction surface area is large, the junction capacity is increased. This is not desirable for two reasons. First, this effective junction capacitor has to be either completely discharged or charged before the transistor can be switched from the non-conducting to the conducting state or vice versa, respectively. This increased switching time is undesirable in switching transistors. Second, the increased capacitance hinders high-frequency operation. Therefore, it would be advantageous to develop a way of providing smaller isolating regions, thus reducing junction size and capacity, decreasing switching time, and improving high-frequency operation.

Briefly, this invention provides a new way of forming patterns in an epitaxial layer of semiconductor material as follows: a pattern of impurities is formed on a substrate; an epitaxial layer of semiconductor material is formed over the substrate and over the pattern of impurities by methods well known in the art; and concurrent with growing the

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epitaxial layer, or thereafter if desired, the pattern of impurities is diffused into the epitaxial layer to form an impurity pattern within the epitaxial layer. It has been found that using this method it is possible to form very narrow isolation regions in a thin epitaxial layer. These small regions or walls have a low junction capacity, resulting in transistors which have faster switching time and improved high-frequency operation.

Epitaxial transistors may also be made by the method of the invention. These transistors have an additional low resistivity region between the substrate and the collector which is formed as a pattern on the substrate and diffused into the epitaxial layer according to the method of this invention. This additional region provides at least two substantial advantages. First, it acts as a sink for minority carriers, reducing minority carrier lifetime in the collector. The switching time of the transistor is therefore reduced. Second, a reduction in collector spreading resistance is achieved in certain applications of the transistor. When the substrate is of the opposite conductivity type from the collector (as it usually is when the transistor is isolated), and the junction between the substrate and the collector is reverse-biased to increase the effective isolation (as it conventionally is), all the collector current must pass through the narrow epitaxial high-resistivity collector region in order to reach the collector terminal normally placed on the top surface of the device. Current cannot flow into the substrate, as it could have if the device had had a substrate of the same conductivity type as the collector. It is not advisable to decrease the collector resistivity because that decreases the breakdown voltage of the device and increases the collector-base capacitance. Therefore, such a device has a high collector spreading resistance and a concomitantly high saturation voltage. A high saturation voltage is undesirable since an ideal switch has zero voltage drop across it when it is in the "ON" state; also a high saturation voltage results in increased power dissipation. Adding a low resistivity region beneath the collector, provides a low resistance path for this collector current, thereby decreasing the collector spreading resistance and the saturation voltage without reducing the breakdown voltage.

The method of this invention and a few of the many devices, particularly epitaxial transistors and isolated epitaxial transistors, which are made by this method, will be better understood from the following more detailed description taken in conjunction with the accompanying drawings, in which:

FIG 1 is a somewhat schematic, greatly enlarged plan view of a substrate having a pattern of impurities prediffused into its surface;

FIG 2 is a transverse section taken along line 2—2 of FIG 1;

FIG 3 is a greatly enlarged, somewhat schematic transverse section showing the substrate of FIGS 1 and 2 with an epitaxial layer deposited on it;

FIG 4 is a greatly enlarged, somewhat schematic transverse section showing the device of FIG 3 after diffusion of the pattern of impurities into the epitaxial layer;

FIG 5 is a greatly enlarged, somewhat schematic transverse section showing an alternative device constructed in accordance with this invention;

FIG 6 is a somewhat schematic, greatly enlarged plan view of a grid pattern formed in an epitaxial layer by the method of this invention;

FIG 7 is a somewhat schematic, greatly enlarged, plan view of an epitaxial transistor having a pattern of impurities in an epitaxial layer made by the method of this invention;

FIG 8 is a tranverse section taken along line 8—8 of FIG 7;

FIG 9 is a greatly enlarged, somewhat schematic plan view of an isolated epitaxial transistor constructed in accordance with this invention;

FIG 10 is a transverse section taken along the line 10—10 of FIG 9;

FIG 11 is a greatly enlarged, somewhat schematic transverse section showing another device constructed in accordance with the invention;

FIG 12 is a greatly enlarged, somewhat schematic plan view showing an epitaxial transistor constructed in accordance with the invention having low resistivity strips beneath the collector; and

FIGS 13 and 14 are transverse sections taken along lines 13—13 and 14—14, respectively, of FIG 12.

Referring now to FIGS 1 and 2, a pattern of impurities 1 is formed on substrate 2. This is usually done by masking the surface of the substrate with a material resistant to diffusion. When the substrate is silicon, silicon dioxide is the preferred mask. Holes are etched in the mask where the pattern is required, by photoengraving processes known in the art. The surface of the substrate is then subjected to a gaseous atmosphere containing the desired impurities. These impurities diffuse into the unmasked portions of the surface of substrate 2. The diffusion time and depth depend upon the resistivity and depth of the pattern desired. The use of this method of forming the impurity pattern, however, is not essential to the invention. Alternatively, the impurity pattern may be deposited on the substrate in any manner, as by painting or spraying a slurry or mixture containing the impurity element or its oxides. In the example illustrated, the impurities used were P-type, such as gallium, aluminum, boron, or indium.

If an N-type pattern were desired, N-type impurities, such as antimony, arsenic, or phosphorus would be used. The choice of specific impurity used often depends upon its diffusion rate.

Referring to FIG 3, an epitaxial layer 3 is now formed on the substrate 2 and deposited impurity pattern 1. Various methods of forming this epitaxial layer are known in the art. They are described in Hunter, L.P., *Handbook of Semiconductor Electronics*, 2d Ed., Subchapter 7.11 (York, Pennsylvania, 1962).

Referring to FIG 4, the time and temperature used in the growth of the epitaxial layer 3 is often such that region 4 is diffused completely through the epitaxial layer while it is being grown. Heating causes these impurities to diffuse. The amount of the concurrent diffusion is governed by the time and temperature chosen for epitaxial growth and the diffusion rate of the impurities used. If the surface of the device is to be subsequently oxidized for protection, some diffusion will also occur at that time. Therefore, where complete diffusion does not occur during epitaxial growth, it is sometimes completed during subsequent oxidation; if not, a separate diffusion step is required to complete the pattern. When region 4 has been completely diffused outwardly to the surface of the epitaxial layer 3, region 5 is effectively isolated by region 4. A transistor may be located in this isolated region 5, if desired. It will be effectively isolated from the portion 5a of the epitaxial layer 5 located outside of isolating region 4.

Another method is illustrated in FIG 5. A first pattern of impurities 6 is formed on substrate 7 as described above. Epitaxial layer 8 is then grown on the substrate 7 and impurity pattern 6. In the method illustrated, the impurities do not diffuse completely through the epitaxial layer during its growth. A second matching pattern of impurities 9 is formed on top of the epitaxial layer 8 in alignment with the first pattern 6. During diffusion, the first pattern 6 diffuses outwardly to meet the second pattern 9 which diffuses inwardly. The two diffusing regions meet, forming the same isolating region 4 shown in FIG 4.

FIG 6 shows another impurity pattern 10 which has been formed in an epitaxial layer. A device may be placed in each of the N-type spaces 11 of the checkerboard so that each device is electrically isolated from the rest by the P-type grid pattern 10. Of course, the conductivity types may be reversed.

Isolating regions used to isolate separate devices on the same body of semiconductor are just one impurity pattern which may be formed by the method of the invention. Another such pattern, shown in FIGS 7 and 8, is used to make epitaxial transistors. These transistors have an extra low-resistivity region 12, formed in substrate 13 and epitaxial layer 14 by the method of the invention. The resistivity of a region formed in this way can be made lower than is easily possible by heavily doping the substrate during its growth. A low-resistivity region beneath the collector provides a path for charged carriers in the collector, thereby substantially reducing the saturation resistance of the device. This prevents the voltage drop otherwise caused by this unnecessary resistance.

The devices of FIGS 7 and 8 are made by forming a pattern of impurities on substrate 13, as done in previous examples, which will be diffused to form region 12. Epitaxial layer 14 of the same conductivity type as these impurities is then grown upon the substrate 13 and the deposited pattern of the impurities. During or after the epitaxial growth, these impurities are diffused into the epitaxial layer 14 to form low-resistivity N+ region 12, shaped as shown. P-type base region 15 and N-type emitter region 16 are then formed in the N-type epitaxial layer 14 by methods well known in the art.

It is understood that by an N region, what is meant is a region of N-type conductivity having a concentration of N-type impurities of from about 10^{15} to 7×10^{19} atoms per cc. An N+ region has a doping level from about 7×10^{19} up to the solubility limit of the impurity used, which in practice may be about 2×10^{21} with arsenic, for example.

There are substantial advantages to having substrate 13 of the opposite conductivity type from region 12. If they are of opposite conductivity type, there is a PN junction between them. When this junction is reverse-biased, there is force upon the stored minority carriers in the collector, causing them to be swept through region 12 and across this reverse-biased junction. Region 12 acts as a sink for these minority carriers which pass from the base region 15 (in which they are majority carriers) into the collector region of the transistor. The high concentration of impurities in low resistivity region 12 traps these minority carriers, improving their chances of recombination with carriers of the opposite type. Additionally, many are swept across the PN junction and removed that way. This decreases the switching time when the transistor is used for switching.

An even greater reduction in switching time can be obtained if the transistor is also doped with a compensating element, e.g., gold, particularly in the region near the base-collector junction. Such compensating elements serve as minority carrier traps to decrease carrier lifetime in the same way as does region 12. However, there are disadvantages associated with the use of a compensating element. The resistivity in both the base and collector regions is raised by the presence of the gold, causing a high satura-

tion resistance. This results in a higher collector-emitter saturation voltage, as described earlier. Finally, gold doping in the base region causes recombination of minority charge carriers in that region, as well, thus increasing the base current when the device is conducting. This reduces the device's current gain, which is particularly undesirable when the transistor is used as an amplifier.

It has been found that the switching characteristics of the epitaxial transistor shown in FIGS 7 and 8 (with a P-type substrate), without any additional doping with a compensating element, are substantially equivalent to those of a conventional epitaxial transistor which has gold doping but no low resistivity region 12. This turns out to be particularly desirable because of the above-mentioned disadvantages inherent in using a compensating element.

Referring now to FIGS 9 and 10, regions 17, 18, 19, and epitaxial layer 20 are formed on substrate 21 in the same manner as was done above in FIGS 7 and 8. Additionally, however, isolating region 22 is formed by the method of the invention. If desired, the impurities forming this region 22 may be deposited along with the impurities forming region 17. They may then be diffused to form region 22 at the same time as region 17 is formed.

Region 17 should be a thin layer or epitaxial layer 20 would have to be undesirably thick in order to leave room to diffuse in the base and emitter regions 18 and 19 above it. Therefore, care must be taken if regions 17 and 22 are to be diffused simultaneously, that region 22 diffuses all the way through the epitaxial layer while region 17 diffuses only a relatively short distance. One way of achieving this is to diffuse region 22 both from above and below, as described earlier, in order to shorten the required diffusion time. Another way is to use impurities for region 17 which are much slower-diffusing than the impurities for region 22. Still a third way is to prediffuse the impurities for region 17 into the substrate before the region 22 impurities are deposited. This decreases the concentration of the region 17 impurities at the substrate surface. Since diffusion rate of these impurities into the epitaxial layer is proportional to their concentration at the substrate surface, their diffusion rate into the epitaxial layer is slowed. Any of these methods, as well as a combination, may be used. Specifically, where phosphorus is the region 17 impurity, pre-diffusion into the substrate is highly desirable. Where antimony is used, diffusion is slower and hence pre-diffusion of region 17 is not always required, depending, of course, on the diffusion rate of the impurities used for isolating region 22. Isolating region 22 isolates the portion 23 of the epitaxial layer 20 in which the transistor is located from the remainder 24 of the epitaxial layer.

Another device constructed in accordance with this invention is shown in FIG 11. This device is the same as that shown in FIGS 9 and 10, except that a lower resistivity P+ substrate 25 is used. It has two epitaxial layers upon it. The lower layer 26 is P-type, the same as previously used for the substrate, and the upper layer 27 is N-type. The impurity pattern required to form both isolating region 28 and low-resistivity region 29 is formed on lower layer 26 as described earlier in this specification. This is done between the epitaxial growth of lower layer 26 and upper layer 27. The isolating region 28 is diffused not only upwardly through the upper N-type epitaxial layer, but also downwardly through lower P-type epitaxial layer 26 to contact the P+ substrate 25. Preferably, the isolating region 28 is also low resistivity. This embodiment has the advantage of providing a low resistivity connection between the bottom surface of the device (to which connections are often made) and the isolating region 28. This low resistivity connection substantially increases the transconductance of the isolation region.

Another device constructed in accordance with the invention is shown in FIGS 12, 13, and 14. This embodiment illustrates a rectangular configuration of a transistor, rather than circular. The particular shape chosen is not essential to the invention; it may be left as a matter of choice by the practitioner. This embodiment is similar to that shown in FIGS 9 and 10, except that there are a plurality of spaced low-resistivity regions 30 which are formed by the method of this invention. The advantage of having a plurality of spaced low-resistivity regions rather than one solid region is as follows: When the junction between the substrate 31 (P-type in the illustration) and the collector 32 of the opposite conductivity type from the substrate is reverse-biased, the minority carriers in the base which are not caused to recombine in the low-resistivity regions 30 are swept into the substrate across the PN junction, as explained above. This transfer of carriers furnishes an alternate way of removing stored carries to reduce switching time. The removal, however, is more effective across a PN junction than across a PN+ junction. Therefore, in this embodiment, the spaced N+ low-resistivity regions 30 provide a sink to cause minority carriers to recombine while the spaces between them provide a path for removal of those carriers which do not so recombine. A geometrical configuration such as the one illustrated in FIGS 12, 13, and 14, makes optimum use of these two complementary effects.

In order to demonstrate the substantial advantages provided by the invention, the fol-

lowing comparative examples are presented:

EXAMPLE 1

Two identical isolated epitaxial transistors of the type shown in FIGS 9 and 10 were prepared. Each had the conventional emitter, base, and collector regions of N, P, and N-type conductivity, respectively. Each transistor was isolated from the surrounding semiconductor material by an isolating region of P-type conductivity. This isolating region formed a PN junction with the collector. The only difference between the two transistors was that only one of them had the low-resistivity region of N-type conductivity between the collector region and the isolating region (as shown in FIGS 9 and 10). The other one did not. Both had their isolation regions grounded to form the reverse-biased junction beneath the collectors.

The switching time of the two transistors was measured on a Tektronix type-R switching time tester. The device without the additional low-resistivity region of the invention had switching time of 80—95 nanoseconds; the device with the additional low resistivity region had a switching time of 14—16 nanoseconds. Thus, at least a five-fold reduction in switching time was achieved with the device constructed in accordance with the invention.

Additionally, the saturation voltages of the two devices were measured, using a 5 ma. collector current and a 1 ma. base current. With the device lacking the low-resistivity region, the collector-emitter saturation voltage was 1.5—5.0 volts. With the device constructed in accordance with the invention, it was 0.18—0.20 volts. This lower saturation voltage is desired in switching application. Furthermore, in the "ON" position, the power loss (which is proportional to the saturation voltage) is substantially reduced in the device constructed in accordance with the invention.

EXAMPLE II

This example compares a transistor as shown in FIGS 9 and 10 with a conventional transistor which does not have the additional low-resistivity region of the invention. However, the conventional transistor has been doped with a compensating element (gold) to improve its switching characteristics.

The switching time of the two transistors was measured on a Tektronix type-R switching-time tester, with the isolation regions connected to ground. The switching times for both devices were comparable: the device having the extra low-resistivity region of the invention had a switching time of about 18 nanoseconds; the prior art gold-doped device had a switching time about 14 nanoseconds.

The essential difference between the characteristics of the two devices was in their saturation resistances. The conventional devices having the gold doping had a saturation resistance of about 800 ohms; the device having the low-resistivity region of the invention, and no gold, had a saturation resistance of only 40 ohms. This higher saturation resistance of the conventional device causes an undesirably high collector-emitter saturation voltage. Therefore, the device constructed in accordance with this invention is a more perfect switch because it can be switched to a lower voltage; yet it still has the improved switching speed previously obtained only with gold doping.

WHAT WE CLAIM IS:—

1. A method of forming epitaxial semiconductor devices having a monocrystalline substrate of semiconductor material with an epitaxial layer disposed thereon comprising the steps of depositing a pattern of impurity upon a surface of the substrate, forming the epitaxial layer upon the same substrate surface, thereby diffusing the impurity into the epitaxial layer and, if necessary, heating the substrate to complete the diffusion of the impurity into the epitaxial layer.

2. The method as claimed in claim 1, wherein said impurity is disposed on the substrate by diffusion into the substrate.

3. The method as claimed in claim 1, wherein said impurity is diffused completely through the epitaxial layer.

4. The method as claimed in claim 1, 2 or 3 wherein the same type of impurity is additionally diffused into an exposed surface of the epitaxial layer in the same pattern and in alignment with the impurity pattern at the substrate-epitaxial layer interface until the impurity is diffused together through the epitaxial layer.

5. The method as claimed in claim 1,2, 3, or 4, wherein the substrate is of one conductivity type and an impurity is deposited with the epitaxial layer to make the layer of the opposite conductivity type from the conductivity type of the substrate.

6. The method as claimed in claim 5 and including the step of forming the impurity pattern as a closed figure and limiting the impurity to one producing the same conductivity type as the substrate and diffusing the impurity completely through the epitaxial layer to form at least one isolation zone surrounding an isolated zone of opposite conductivity type.

7. The method as claimed in claim 1 or 2 and including the step of forming upon the substrate a pattern of impurities which form a first conductivity type in said semiconductor material, depositing upon the substrate and aforesaid impurities an epitaxial layer of the same conductivity type as that

lowing comparative examples are presented:

EXAMPLE 1

Two identical isolated epitaxial transistors of the type shown in FIGS 9 and 10 were prepared. Each had the conventional emitter, base, and collector regions of N, P, and N-type conductivity, respectively. Each transistor was isolated from the surrounding semiconductor material by an isolating region of P-type conductivity. This isolating region formed a PN junction with the collector. The only difference between the two transistors was that only one of them had the low-resistivity region of N-type conductivity between the collector region and the isolating region (as shown in FIGS 9 and 10). The other one did not. Both had their isolation regions grounded to form the reverse-biased junction beneath the collectors.

The switching time of the two transistors was measured on a Tektronix type-R switching time tester. The device without the additional low-resistivity region of the invention had switching time of 80—95 nanoseconds; the device with the additional low resistivity region had a switching time of 14—16 nanoseconds. Thus, at least a five-fold reduction in switching time was achieved with the device constructed in accordance with the invention.

Additionally, the saturation voltages of the two devices were measured, using a 5 ma. collector current and a 1 ma. base current. With the device lacking the low-resistivity region, the collector-emitter saturation voltage was 1.5—5.0 volts. With the device constructed in accordance with the invention, it was 0.18—0.20 volts. This lower saturation voltage is desired in switching application. Furthermore, in the "ON" position, the power loss (which is proportional to the saturation voltage) is substantially reduced in the device constructed in accordance with the invention.

EXAMPLE II

This example compares a transistor as shown in FIGS 9 and 10 with a conventional transistor which does not have the additional low-resistivity region of the invention. However, the conventional transistor has been doped with a compensating element (gold) to improve its switching characteristics.

The switching time of the two transistors was measured on a Tektronix type-R switching-time tester, with the isolation regions connected to ground. The switching times for both devices were comparable: the device having the extra low-resistivity region of the invention had a switching time of about 18 nanoseconds; the prior art gold-doped device had a switching time about 14 nanoseconds.

The essential difference between the characteristics of the two devices was in their saturation resistances. The conventional devices having the gold doping had a saturation resistance of about 800 ohms; the device having the low-resistivity region of the invention, and no gold, had a saturation resistance of only 40 ohms. This higher saturation resistance of the conventional device causes an undesirably high collector-emitter saturation voltage. Therefore, the device constructed in accordance with this invention is a more perfect switch because it can be switched to a lower voltage; yet it still has the improved switching speed previously obtained only with gold doping.

WHAT WE CLAIM IS:—

1. A method of forming epitaxial semiconductor devices having a monocrystalline substrate of semiconductor material with an epitaxial layer disposed thereon comprising the steps of depositing a pattern of impurity upon a surface of the substrate, forming the epitaxial layer upon the same substrate surface, thereby diffusing the impurity into the epitaxial layer and, if necessary, heating the substrate to complete the diffusion of the impurity into the epitaxial layer.

2. The method as claimed in claim 1, wherein said impurity is disposed on the substrate by diffusion into the substrate.

3. The method as claimed in claim 1, wherein said impurity is diffused completely through the epitaxial layer.

4. The method as claimed in claim 1, 2 or 3 wherein the same type of impurity is additionally diffused into an exposed surface of the epitaxial layer in the same pattern and in alignment with the impurity pattern at the substrate-epitaxial layer interface until the impurity is diffused together through the epitaxial layer.

5. The method as claimed in claim 1,2, 3, or 4, wherein the substrate is of one conductivity type and an impurity is deposited with the epitaxial layer to make the layer of the opposite conductivity type from the conductivity type of the substrate.

6. The method as claimed in claim 5 and including the step of forming the impurity pattern as a closed figure and limiting the impurity to one producing the same conductivity type as the substrate and diffusing the impurity completely through the epitaxial layer to form at least one isolation zone surrounding an isolated zone of opposite conductivity type.

7. The method as claimed in claim 1 or 2 and including the step of forming upon the substrate a pattern of impurities which form a first conductivity type in said semiconductor material, depositing upon the substrate and aforesaid impurities an epitaxial layer of the same conductivity type as that

formed by said impurities, diffusing the impurities into the substrate to form a zone of lower resistivity than the remainder of the epitaxial layer, and diffusing into the epitaxial layer impurities forming a transistor base zone above said low-resistance zone and an emitter zone in the base zone.

8. The method as claimed in claim 1 or 2 and including the step of disposing upon a surface of the substrate of a first conductivity type a first impurity of opposite conductivity-forming type to that of the substrate, and a second impurity of the same conductivity-forming type as that of the substrate, the second impurity being disposed in a pattern surrounding the first impurity and out of contact therewith depositing the epitaxial layer upon the substrate and impurities with an impurity therein forming a layer of opposite conductivity type to that of the substrate, diffusing the first impurity into the epitaxial layer and the second impurity through the epitaxial layer to thereby form a collector zone in the epitaxial layer with a low resistance zone of the same conductivity type contiguous therewith and separated from the rest of the layer by an isolation zone of opposite conductivity type, and diffusing base and emitter zones into the collector zone in said epitaxial layer.

9. The method as claimed in claim 8, wherein said second impurity has a faster diffusion rate than the first impurity, and the substrate and epitaxial layer are heated for a sufficient period of time to diffuse the second impurity completely through the epitaxial layer while the first impurity diffuses only slightly into the epitaxial layer.

10. An epitaxial transistor manufactured in accordance with the method claimed in any of the preceding claims, wherein emitter, base and collector regions are formed in the epitaxial layer with the collector lowermost therein, and a fourth region of the same conductivity type as the collector but having a lower resistivity than the collector is disposed on the substrate side of the collector in contact with the substrate.

11. The transistor as claimed in claim 10, wherein the fourth region is separated into a plurality of individual unconnected zones.

12. The transistor as claimed in claim 10 or 11 wherein an additional isolation zone of the same conductivity type as the substrate is provided and extends through the epitaxial layer out of contact with the first four regions therein.

13. The method of forming epitaxial semiconductor devices substantially as described.

14. An epitaxial transistor substantially as described with reference to the accompanying drawings.

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