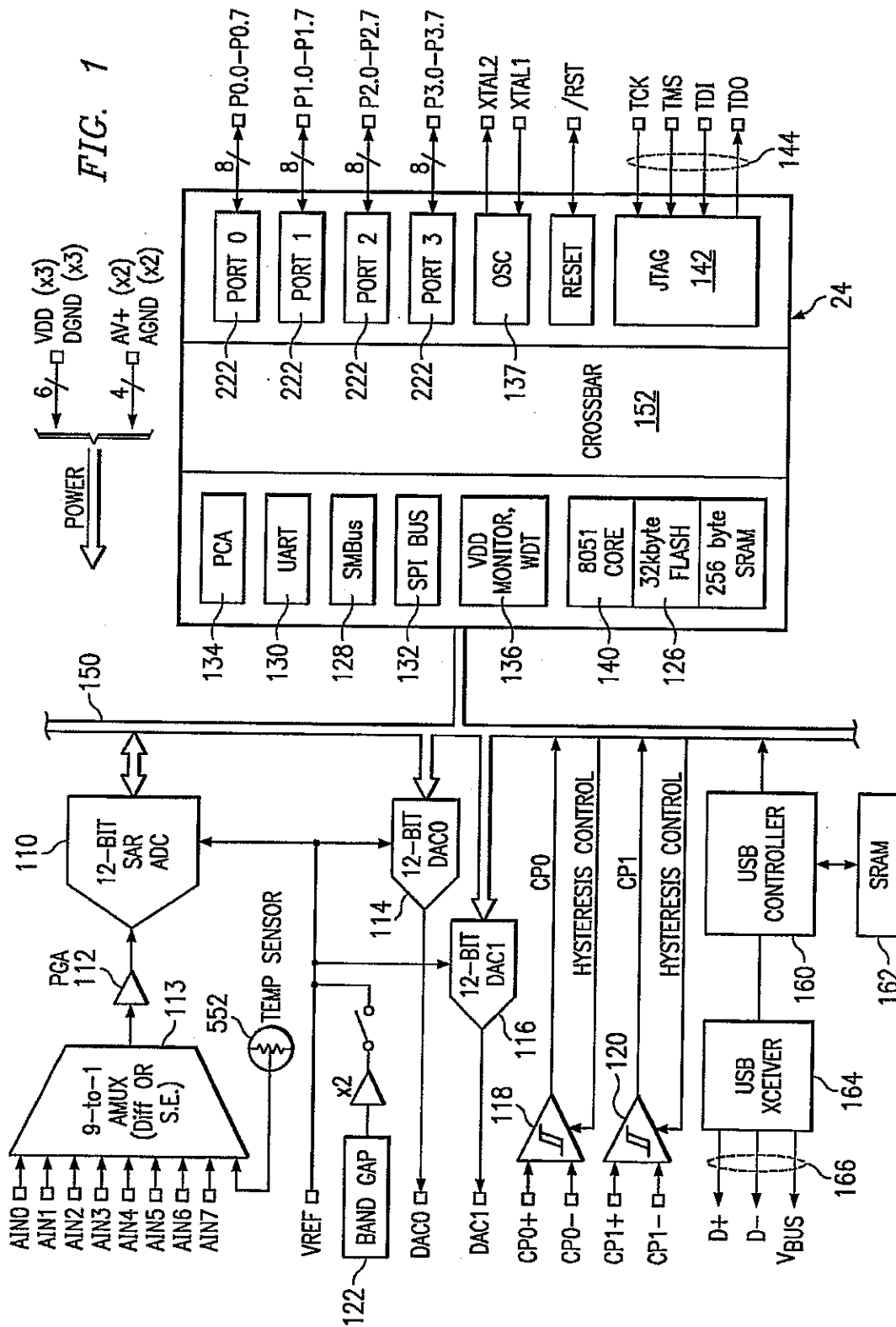
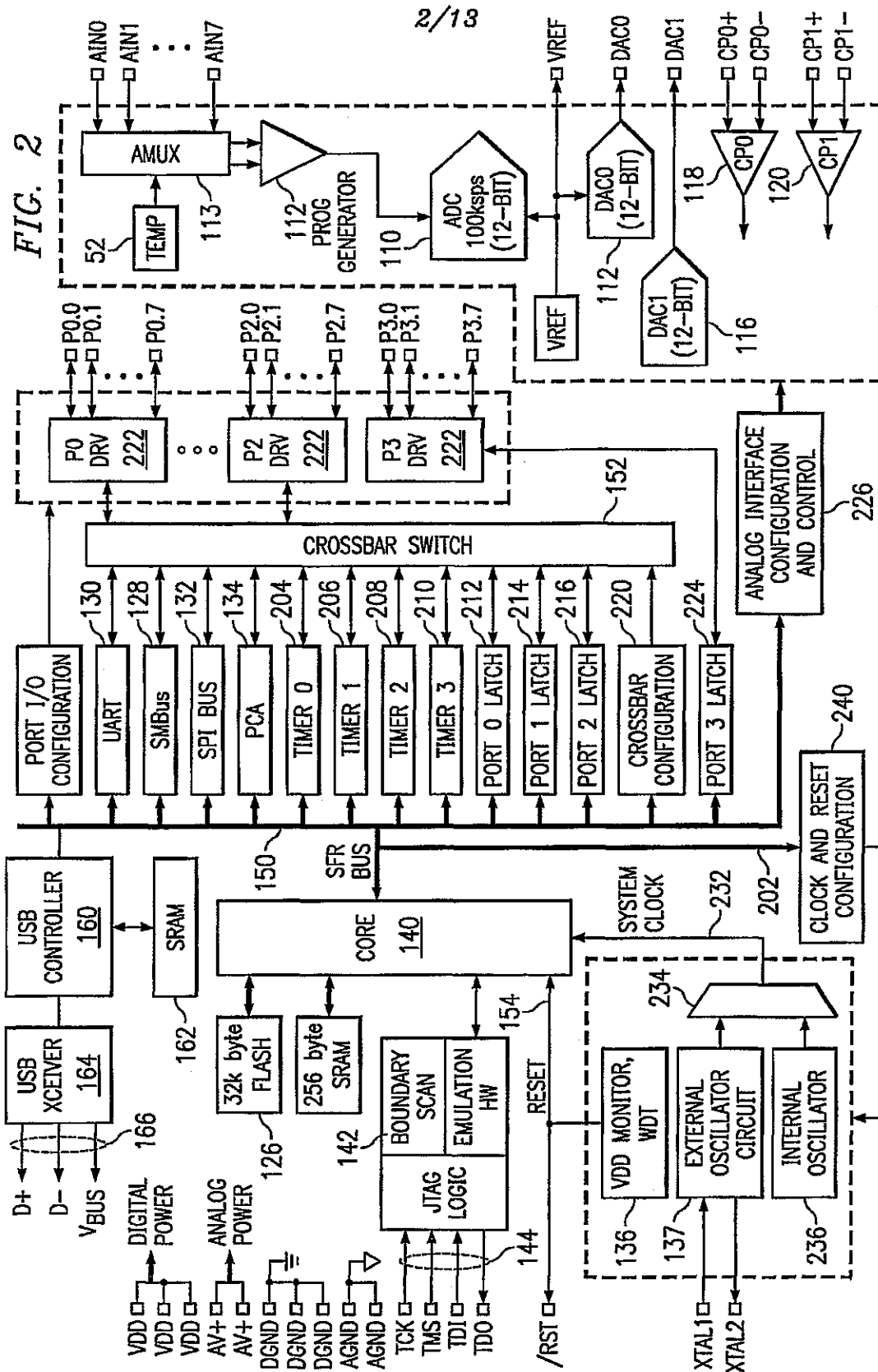
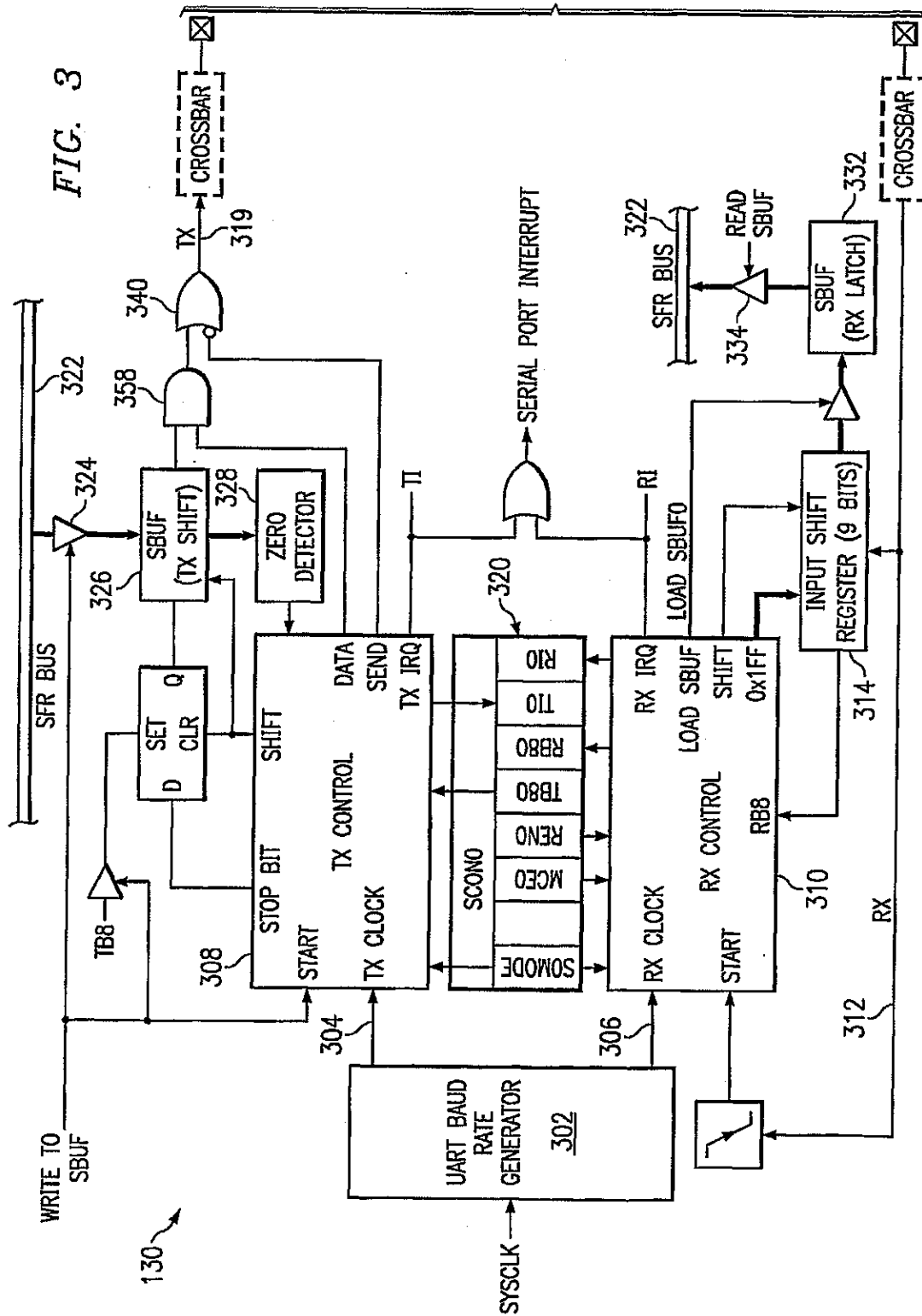






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FIG. 3A

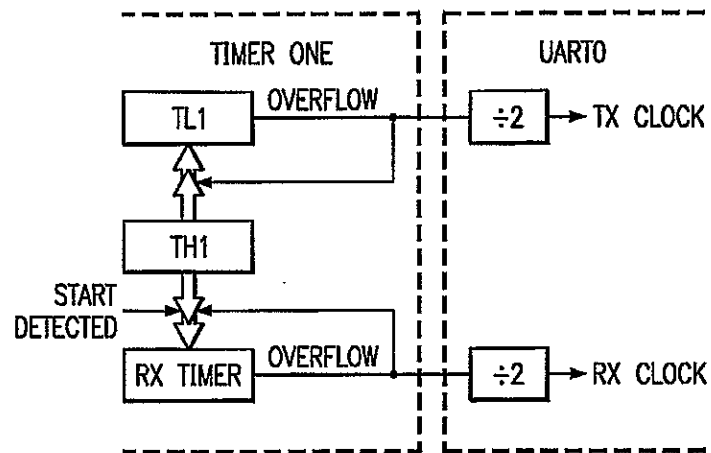


FIG. 4

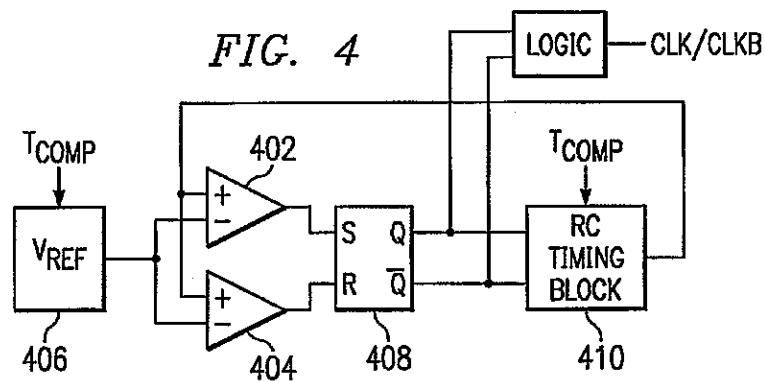
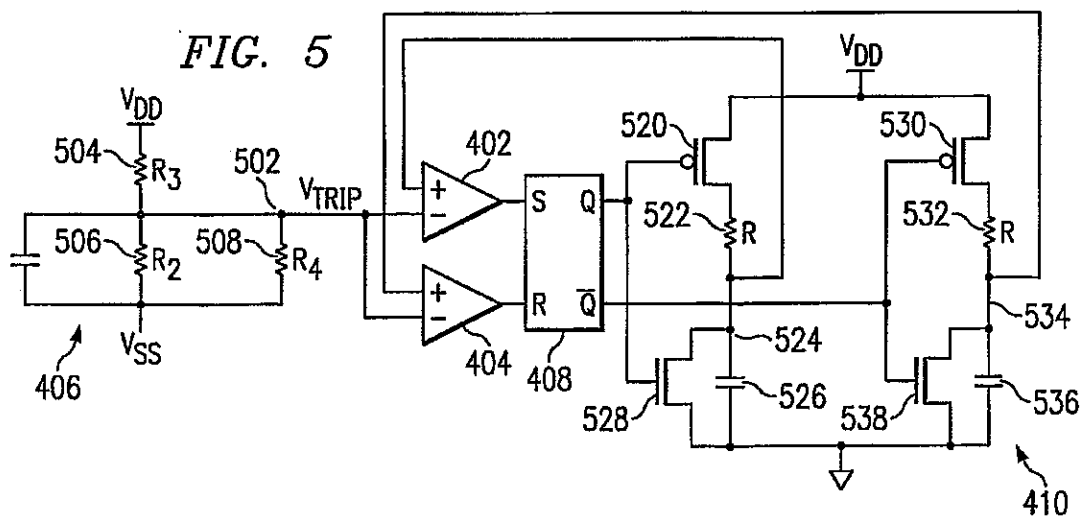


FIG. 5



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FIG. 6

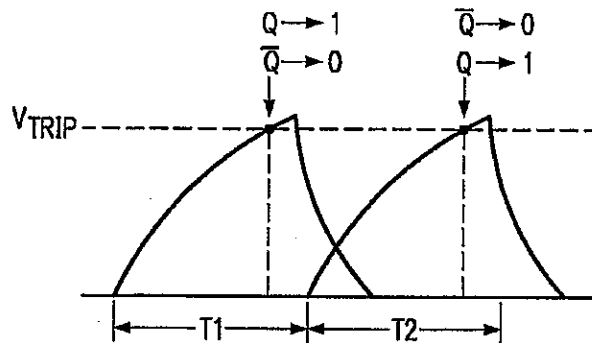


FIG. 7

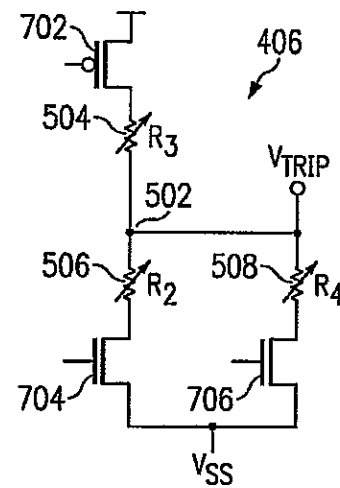


FIG. 8

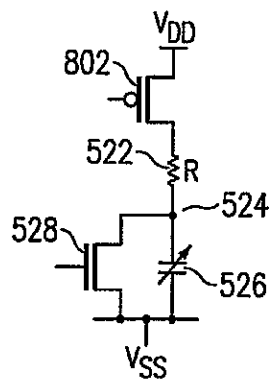


FIG. 9

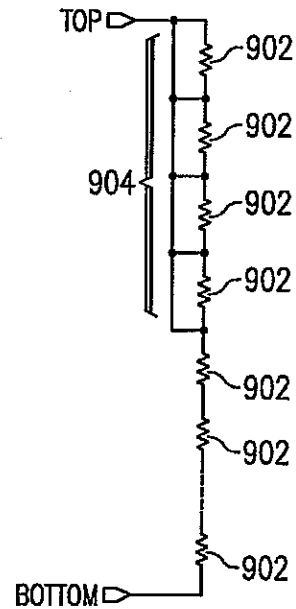
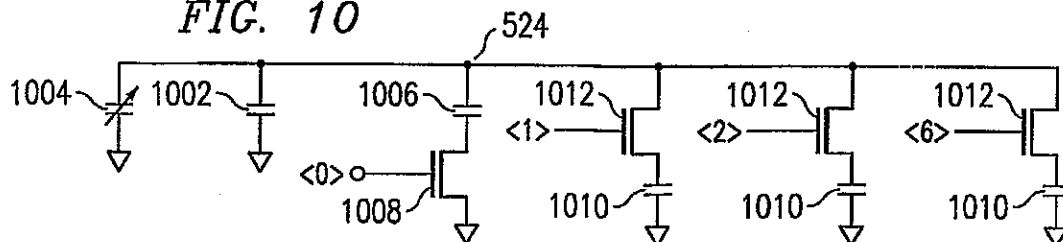
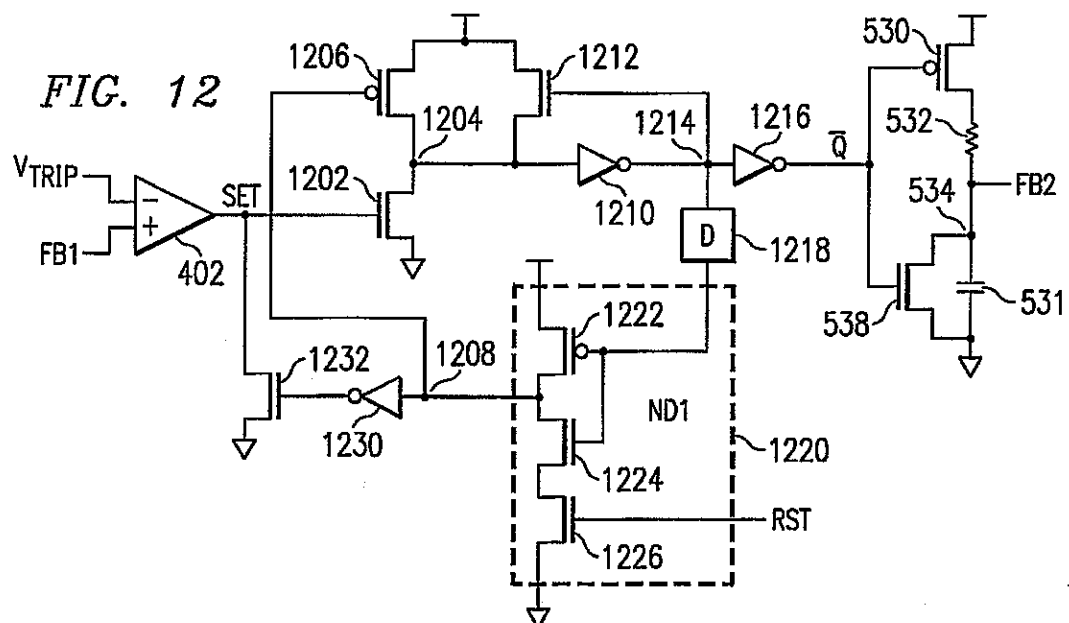
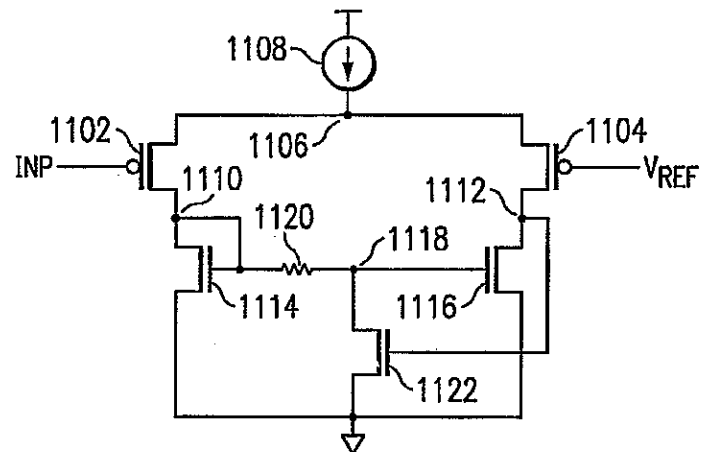
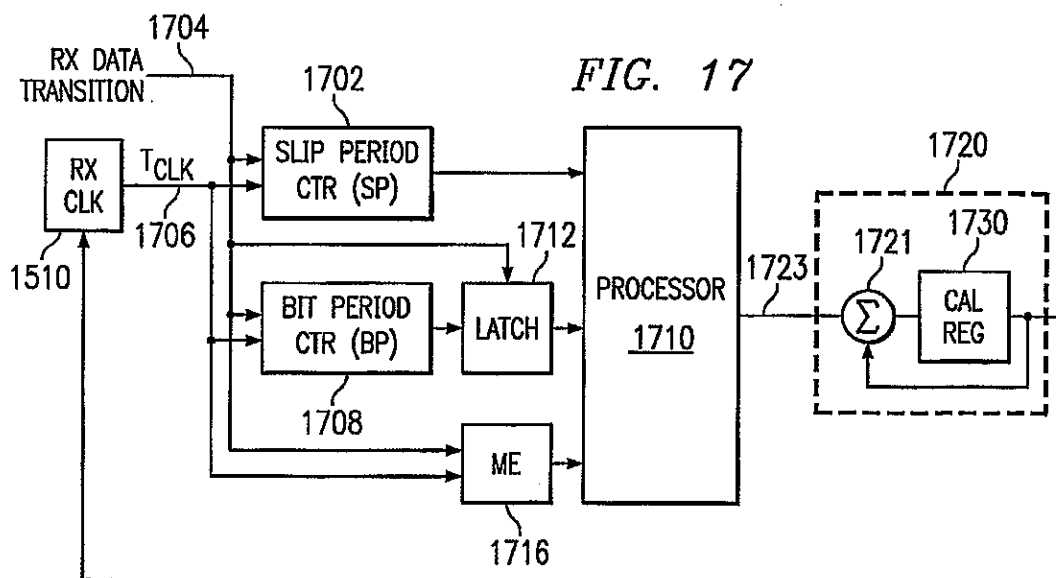
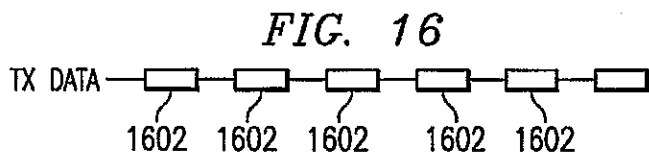
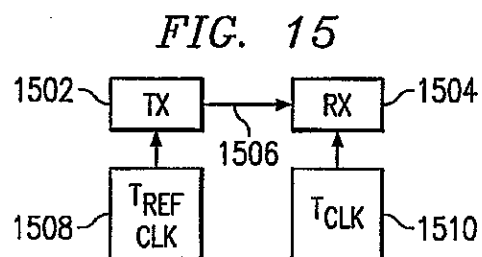
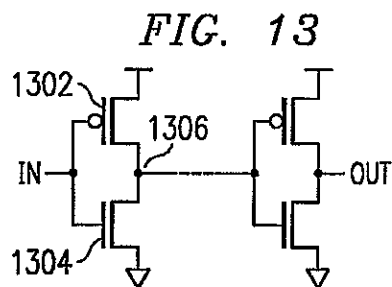
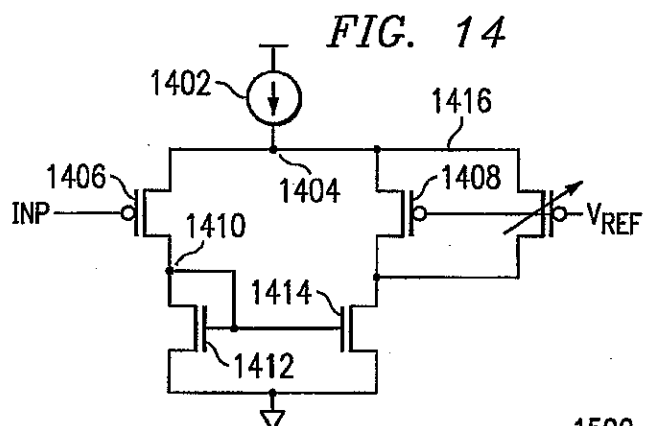


FIG. 10





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FIG. 18

|    |   |   |   |   |   |   |   |   |   |   |    |    |    |    |    |     |
|----|---|---|---|---|---|---|---|---|---|---|----|----|----|----|----|-----|
| SP | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | ... |
| PH | 0 | 1 | 2 | 3 | 0 | 1 | 2 | 3 | 0 | 1 | 2  | 3  | 0  | 1  | 2  |     |

FIG. 19

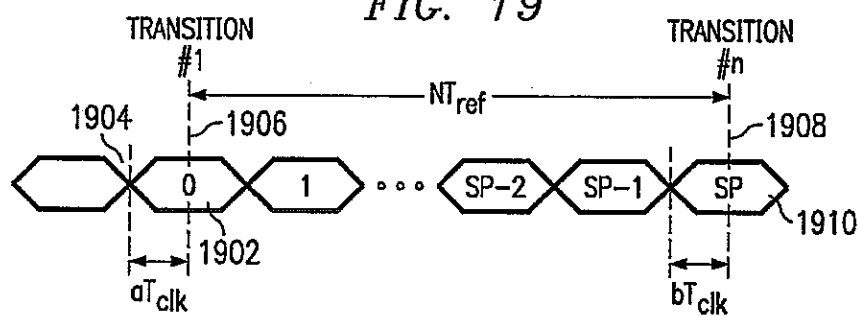


FIG. 20

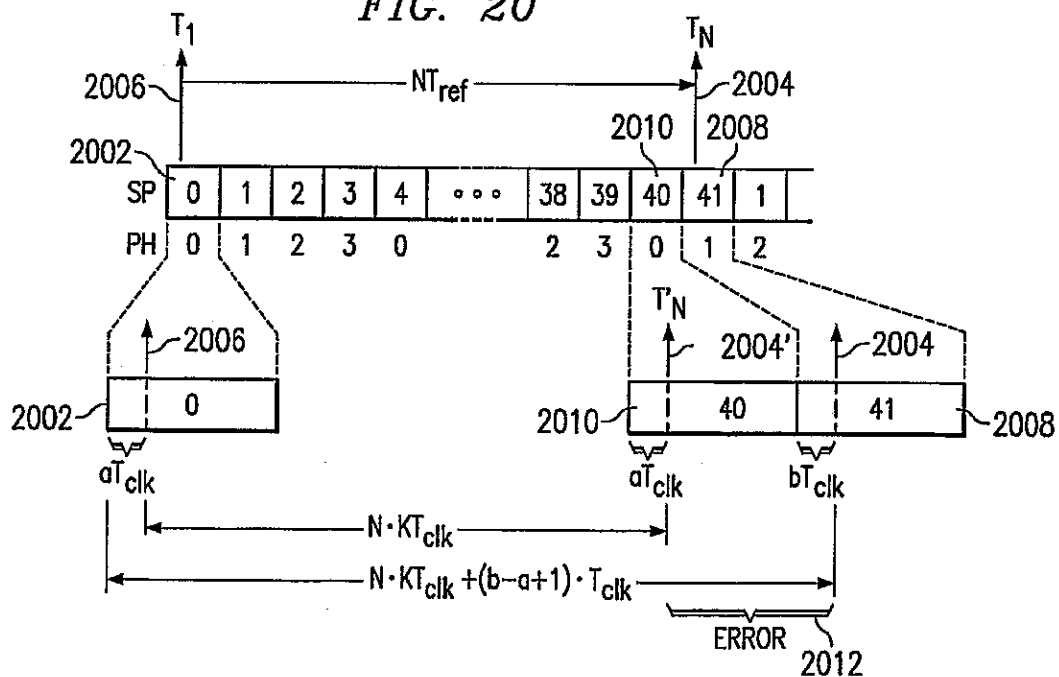
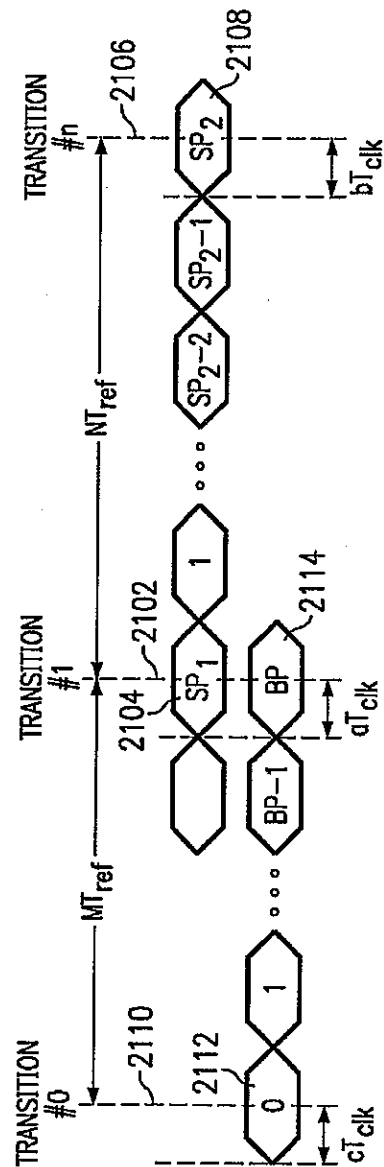
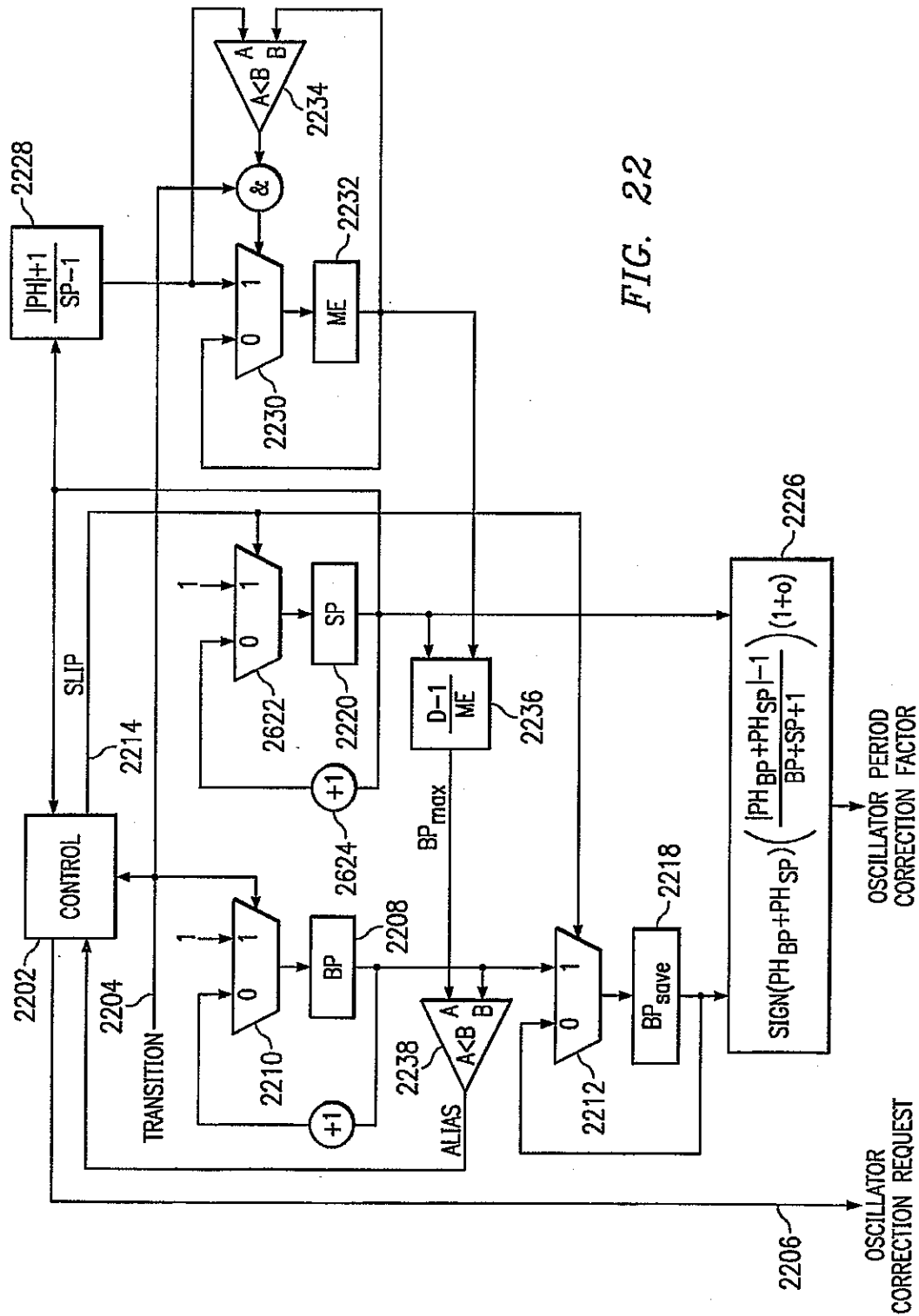


FIG. 21

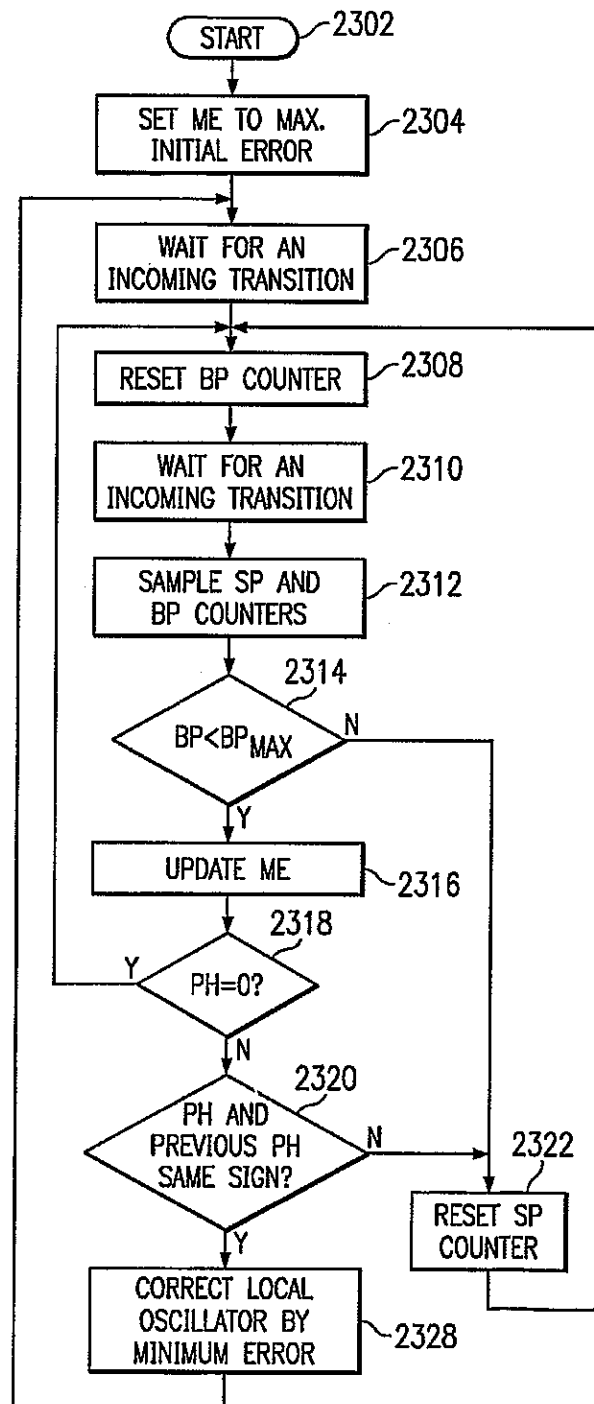


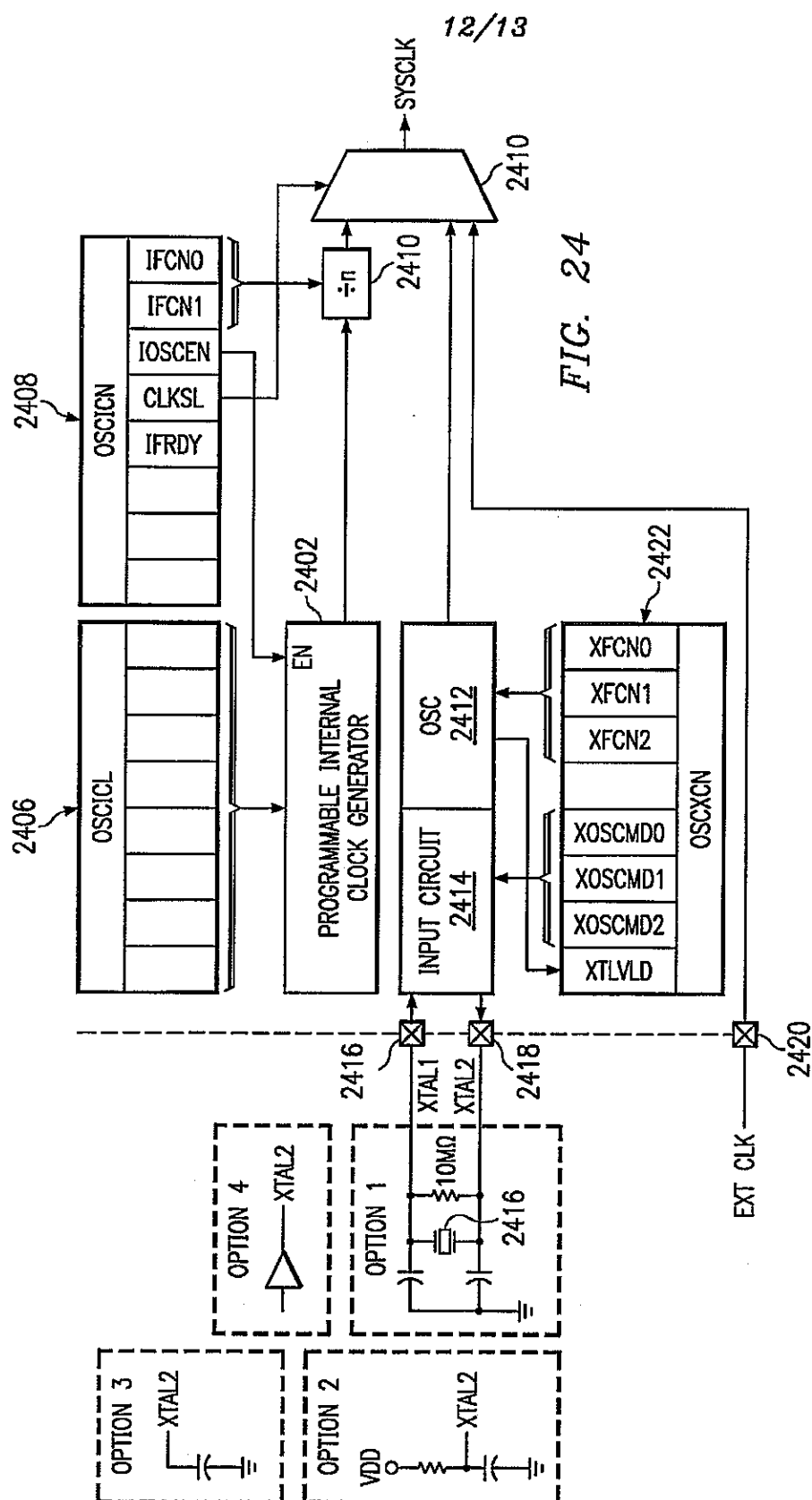
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FIG. 23





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FIG. 25

| R/W  | R/W  | R/W  | R/W  | R/W  | R/W  | R/W  | R/W  | RESET VALUE   |
|------|------|------|------|------|------|------|------|---------------|
| -    |      |      |      |      |      |      |      | VARIABLE SFR  |
| BIT7 | BIT6 | BIT5 | BIT4 | BIT3 | BIT2 | BIT1 | BIT0 | ADDRESS: 0xB3 |

Bit7: UNUSED. Read=0. Write=don't care.  
 Bits 6-0: OSCICL: Internal Oscillator Calibration Register.  
 This register determines the internal oscillator period

FIG. 26

| R/W  | R/W  | R/W  | R     | R/W   | R/W    | R/W   | R/W   | RESET VALUE   |
|------|------|------|-------|-------|--------|-------|-------|---------------|
| -    | -    | -    | IFRDY | CLKSL | IOSCEN | IFCN1 | IFCN0 | 00010100 SFR  |
| BIT7 | BIT6 | BIT5 | BIT4  | BIT3  | BIT2   | BIT1  | BIT0  | ADDRESS: 0xB2 |

Bits7-5: UNUSED. Read=000b, Write=don't care.  
 Bit4: IFRDY: Internal Oscillator Frequency Ready Flag.  
 0: Internal Oscillator is not running at programmed frequency.  
 1: Internal Oscillator is running at programmed frequency.  
 Bit3: CLKSL: System Clock Source Select Bit.  
 0: SYSCLK derived from the Internal Oscillator, and scaled as per the IFCN bits.  
 1: SYSCLK derived from the External Oscillator circuit.  
 Bit2: IOSCEN: Internal Oscillator Enable Bit.  
 0: Internal Oscillator Disabled.  
 1: Internal Oscillator Enabled.  
 Bits1-0: IFCN1-0: Internal Oscillator Frequency Control Bits.  
 00: SYSCLK derived from Internal Oscillator divided by 8.  
 01: SYSCLK derived from Internal Oscillator divided by 4.  
 10: SYSCLK derived from Internal Oscillator divided by 2.  
 11: SYSCLK derived from Internal Oscillator divided by 1.