(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
3 July 2003 (03.07.2003)

PCT

(10) International Publication Number
WO 03/054964 A2

(51) International Patent Classification[7]: H01L 27/115, 21/8246

(21) International Application Number: PCT/US02/39781

(22) International Filing Date:
11 December 2002 (11.12.2002)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
10/022,798 20 December 2001 (20.12.2001) US

(71) Applicants: **ADVANCED MICRO DEVICES, INC.** [US/US]; One AMD Place, Mail Stop 68, Sunnyvale, CA 94088-3453 (US). **FUJITSU LIMITED** [JP/JP]; 1-1, Kamikodanaka 4-chome, Nakahara-ku, Kuwasaki-shi, Kanagawa 211 (JP).

(72) Inventors: **OGURA, Jusuke**; 10183 Denison Avenue, Cupertino, CA 95014 (US). **RAMSBEY, Mark, T.**; 402 Cumulus Avenue, Sunnyvale, CA 94087 (US). **HALLIYAL, Arvind**; 20679 Shelly Drive, Cupertino, CA 95014 (US). **KRIVOKAPIC, Zoran**; 2321 De Varona Place, Santa Clara, CA 95050 (US). **NGO, Minh, Van**; 40986 Canyon Heights Drive, Fremont, CA 94539 (US). **TRIPSAS, Nicholas, H.**; 6017 Crossmont Court, San Jose, CA 95120 (US).

(74) Agent: **COLLOPY, Daniel, R.**; Advanced Micro Devices, Inc., One AMD Place, Mail Stop 68, Sunnyvale, CA 94088-3453 (US).

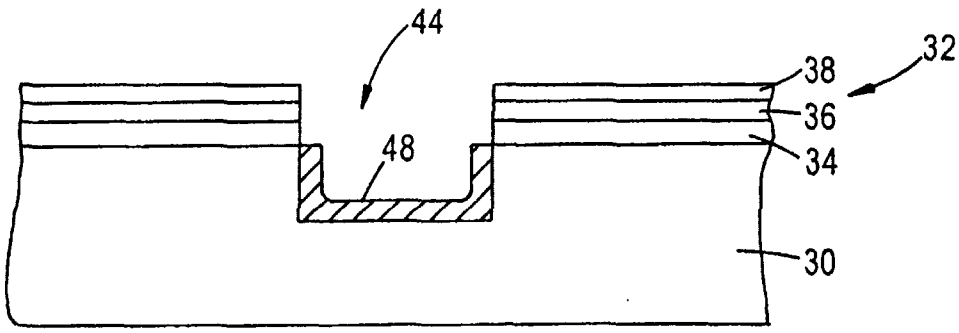
(81) Designated States *(national)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, UZ, VN, YU, ZA, ZW.

(84) Designated States *(regional)*: ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, SI, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:
— *without international search report and to be republished upon receipt of that report*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: MONOS DEVICE HAVING BURIED METAL SILICIDE BIT LINE



(57) Abstract: A MONOS device and method for making the device has a charge trapping dielectric layer (32), such as an oxide-nitride-oxide (ONO) layer (34, 36, 38), formed on a substrate (30). A recess (44) is created through the ONO layer (32) and in the substrate (30). A metal silicide bit line (48) is formed in the recess (44) and bit line oxide (54) is formed on top of the metal silicide. A word line (56) is formed over the ONO layer (32) and the bit line oxide (54), and a low resistance silicide (58) is provided on top of the word line (56). The silicide (58) is formed by laser thermal annealing, for example.

WO 03/054964 A2