FIG. 1

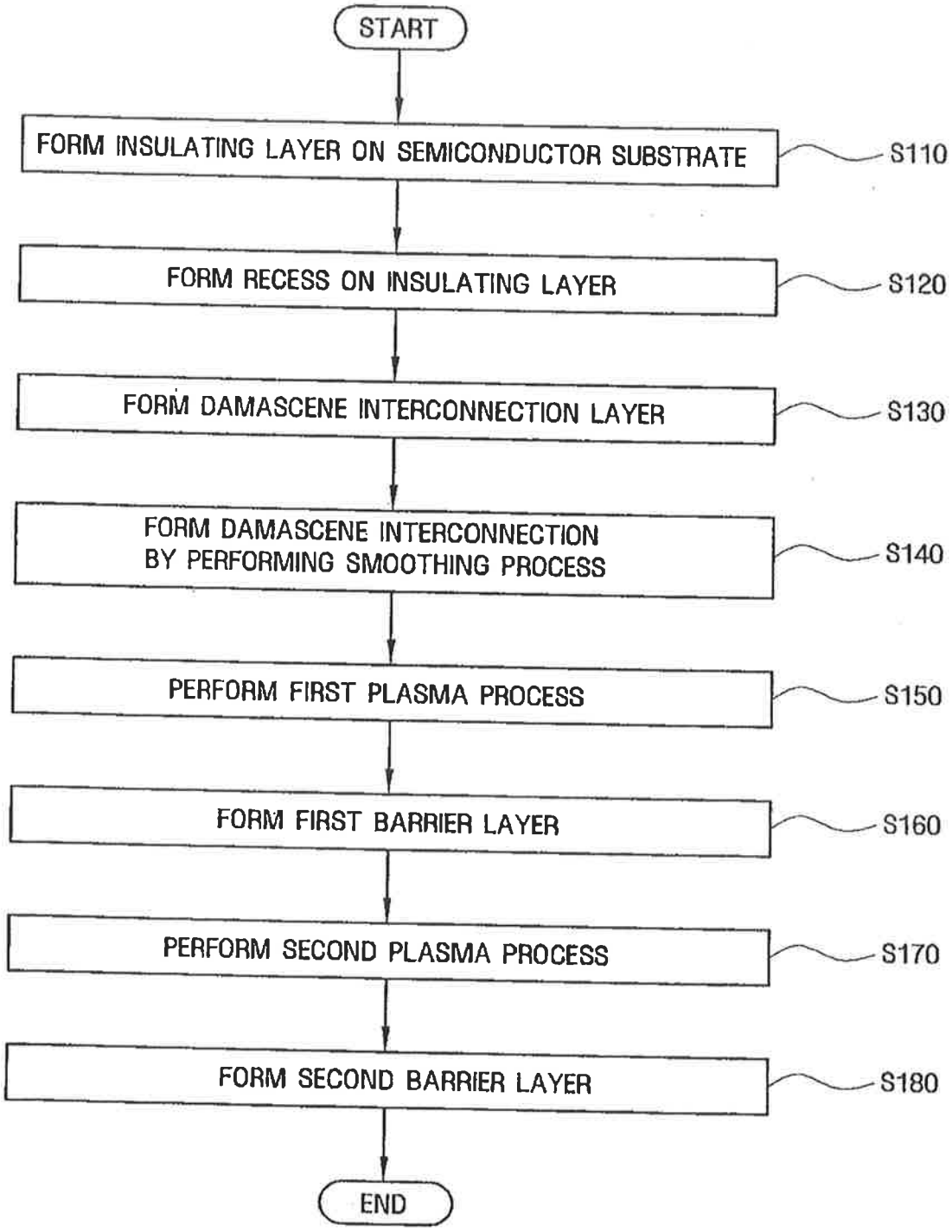

START
FORM INSULATING LAYER ON SEMICONDUCTOR SUBSTRATE
S110
FORM RECESS ON INSULATING LAYER
S120
FORM DAMASCENE INTERCONNECTION LAYER
S130
FORM DAMASCENE INTERCONNECTION BY PERFORMING SMOOTHING PROCESS
S140
PERFORM FIRST PLASMA PROCESS
S150
FORM FIRST BARRIER LAYER
S160
PERFORM SECOND PLASMA PROCESS
S170
FORM SECOND BARRIER LAYER
S180
END

FIG. 2

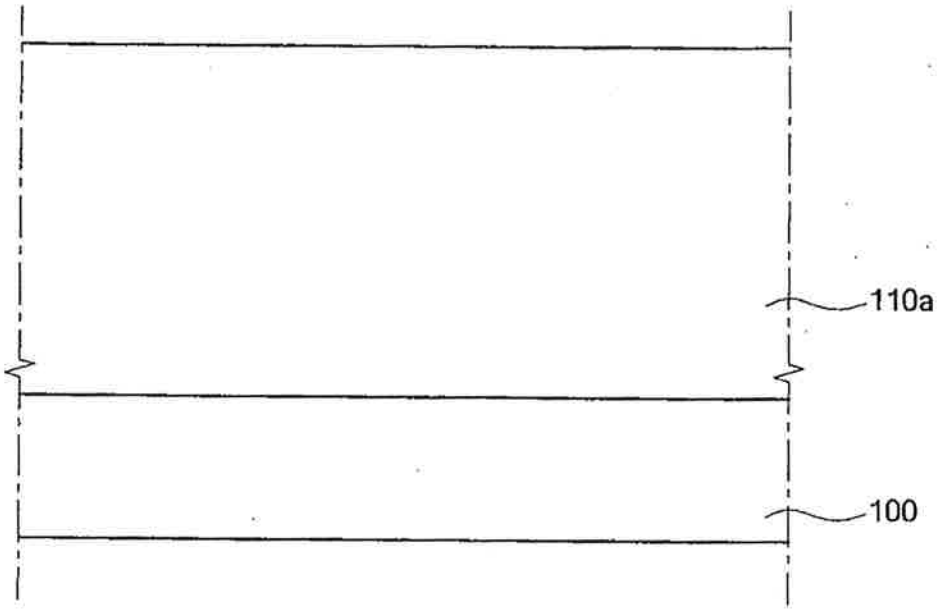


FIG. 3

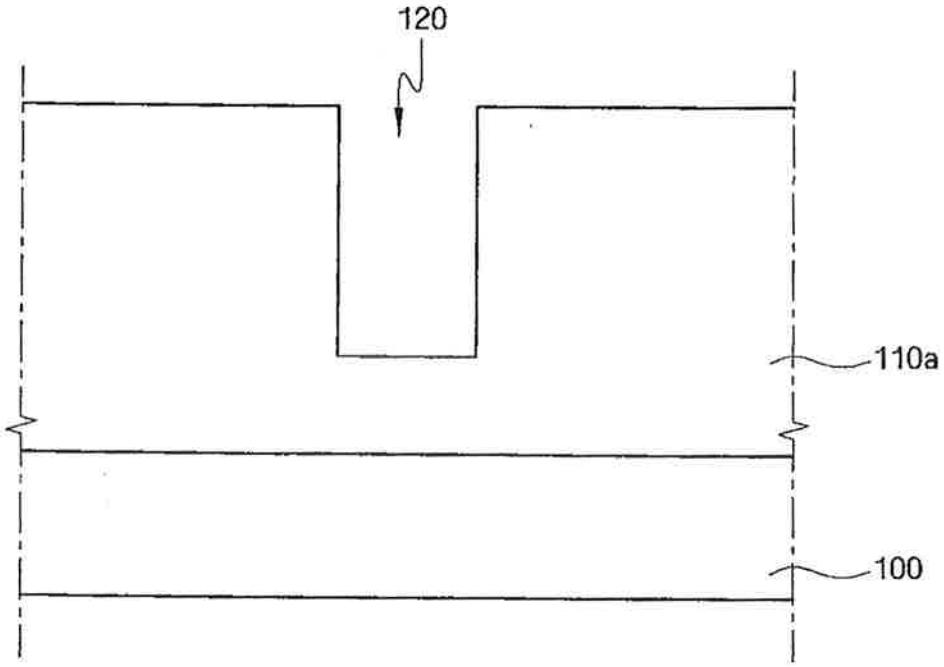


FIG. 4

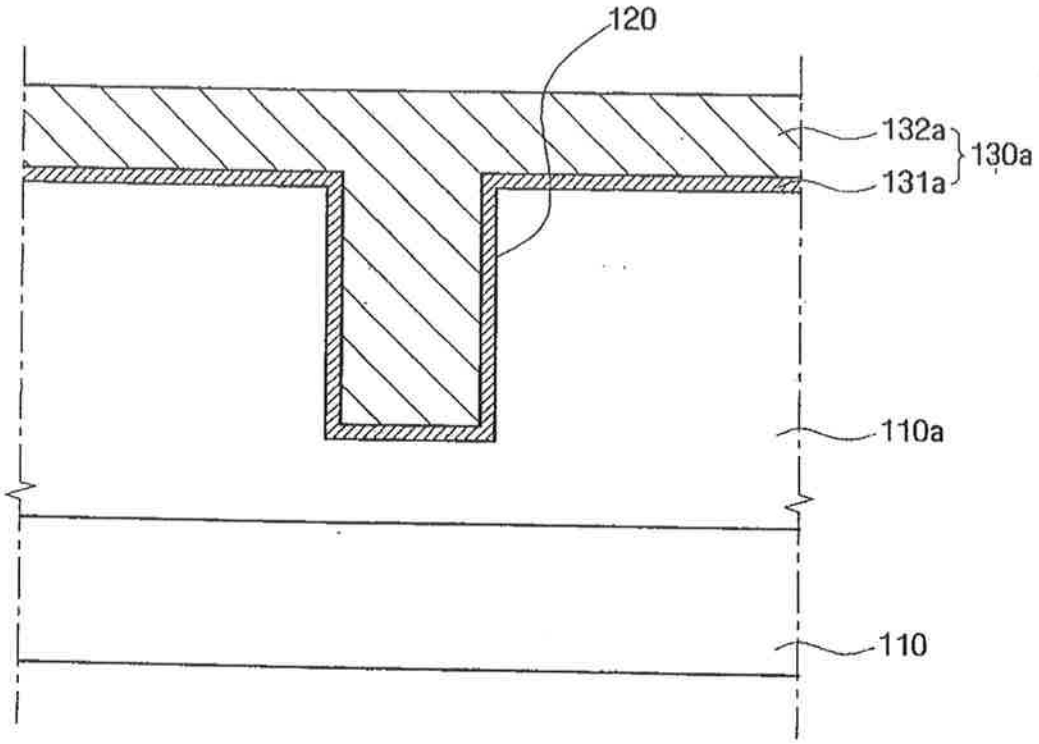


FIG. 5

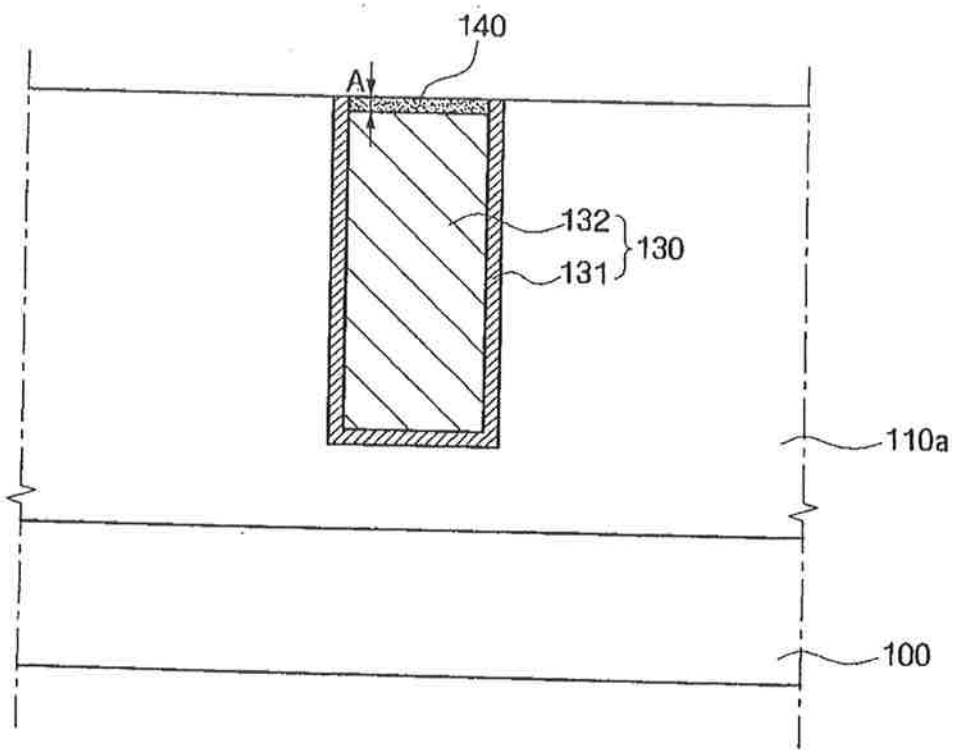


FIG. 6

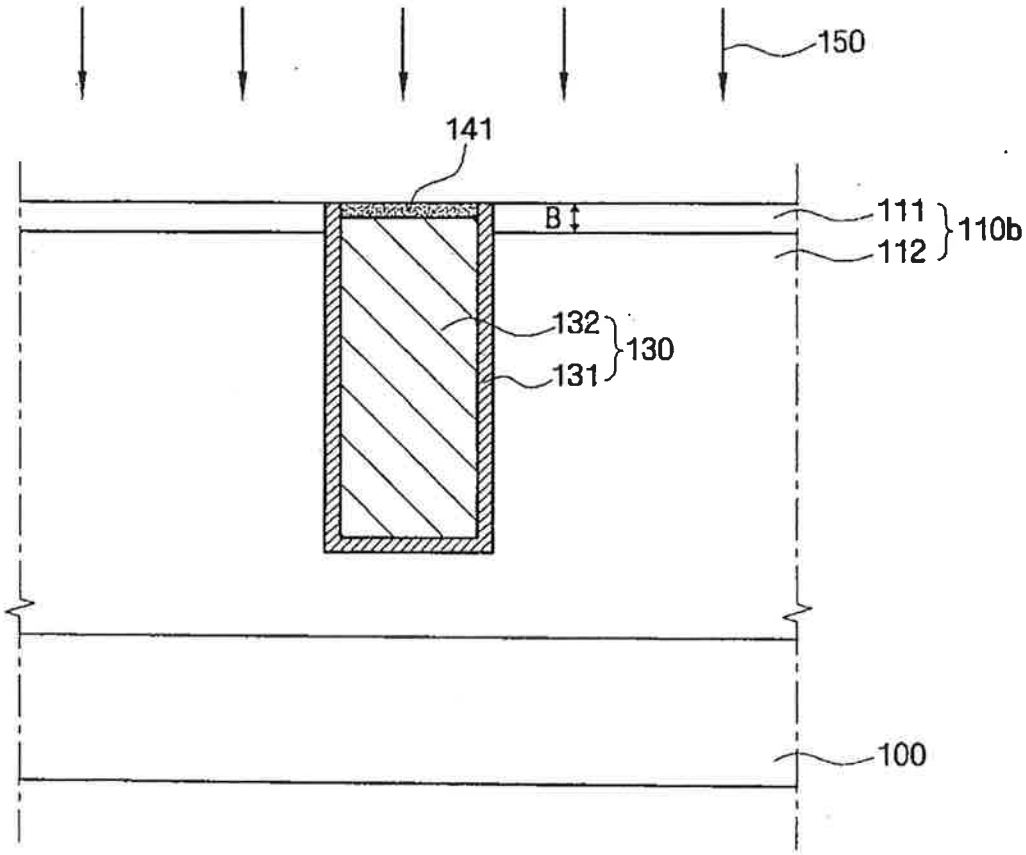


FIG. 7

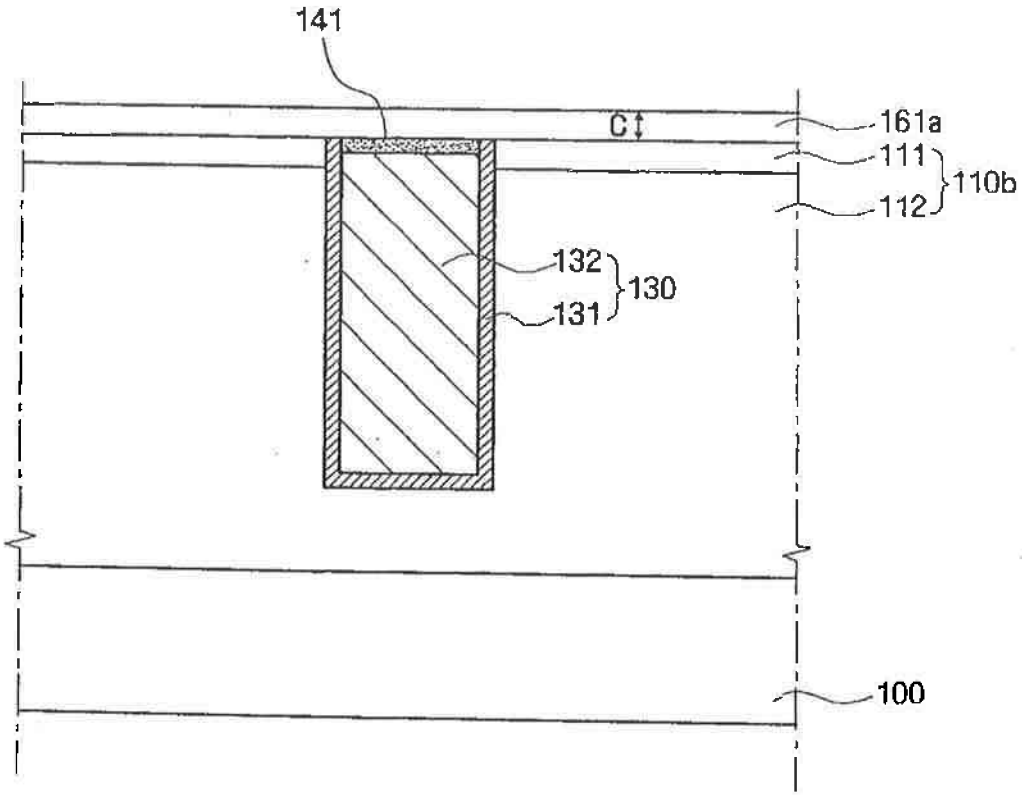


FIG. 8

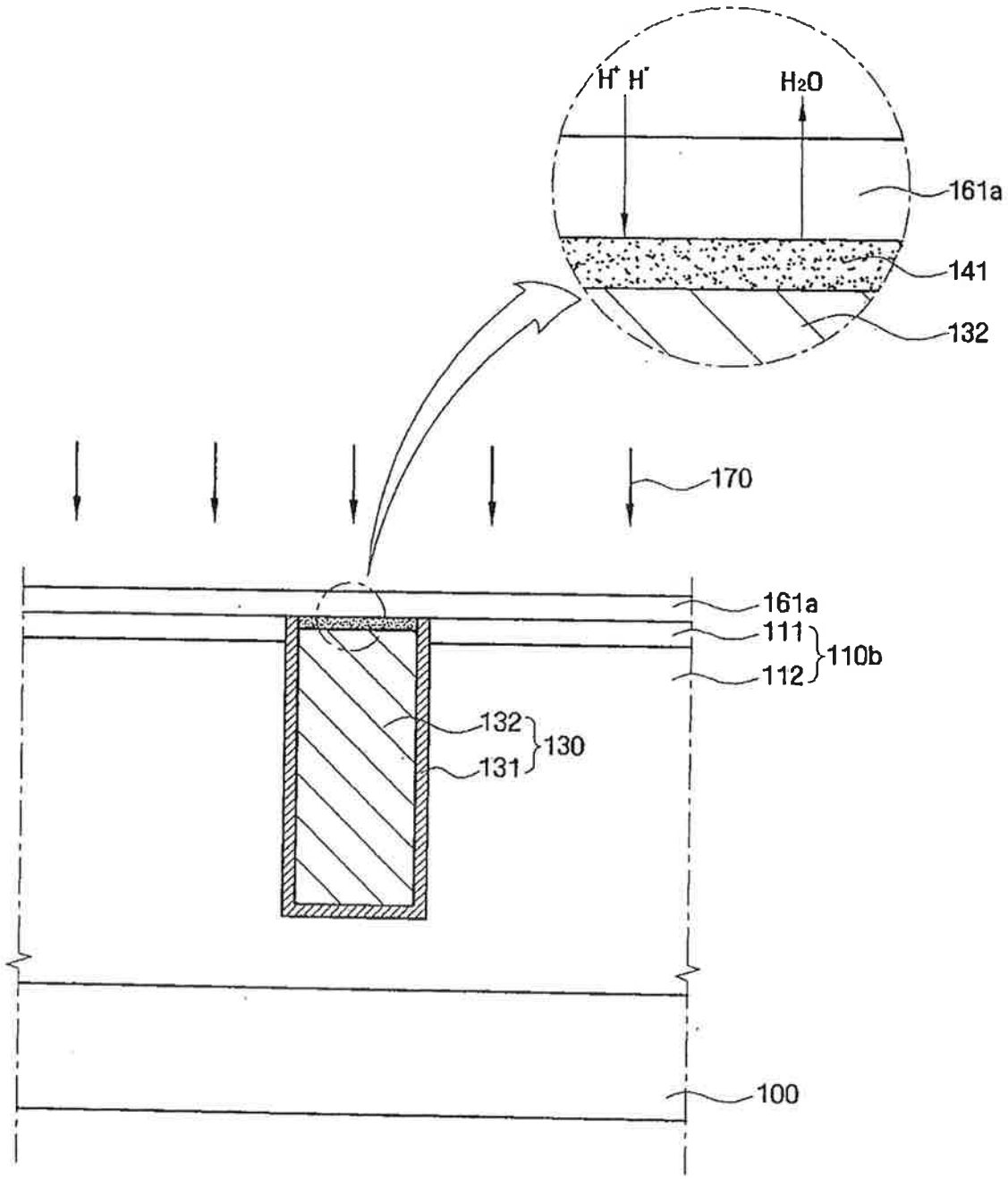


FIG. 9

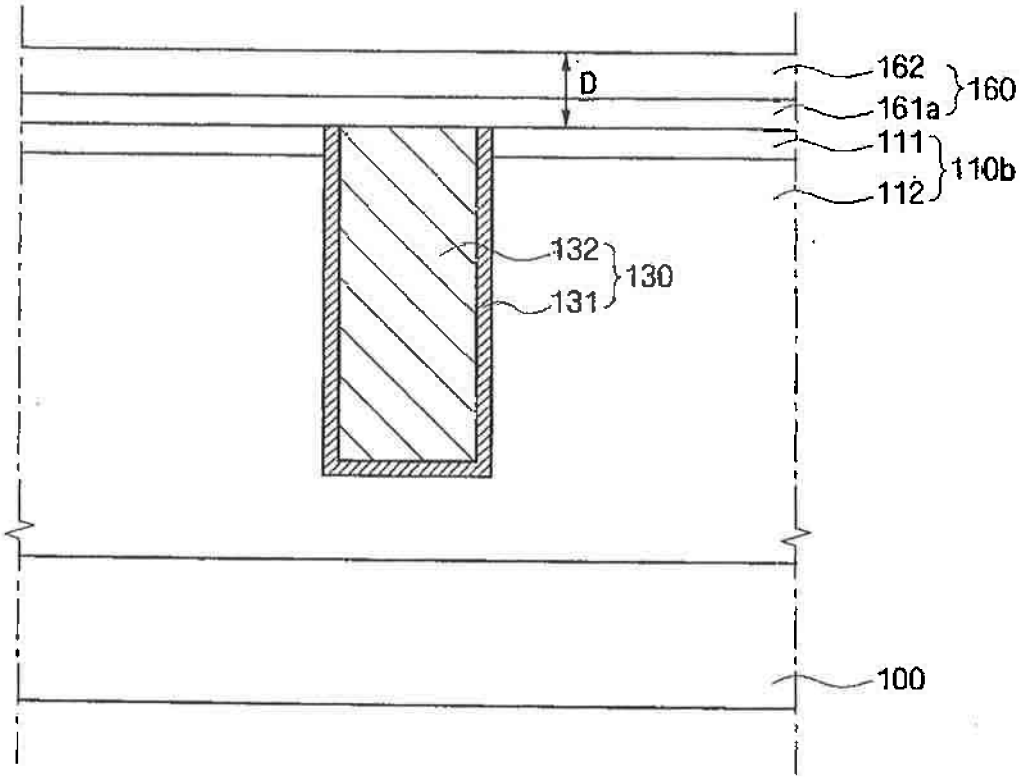


FIG. 10

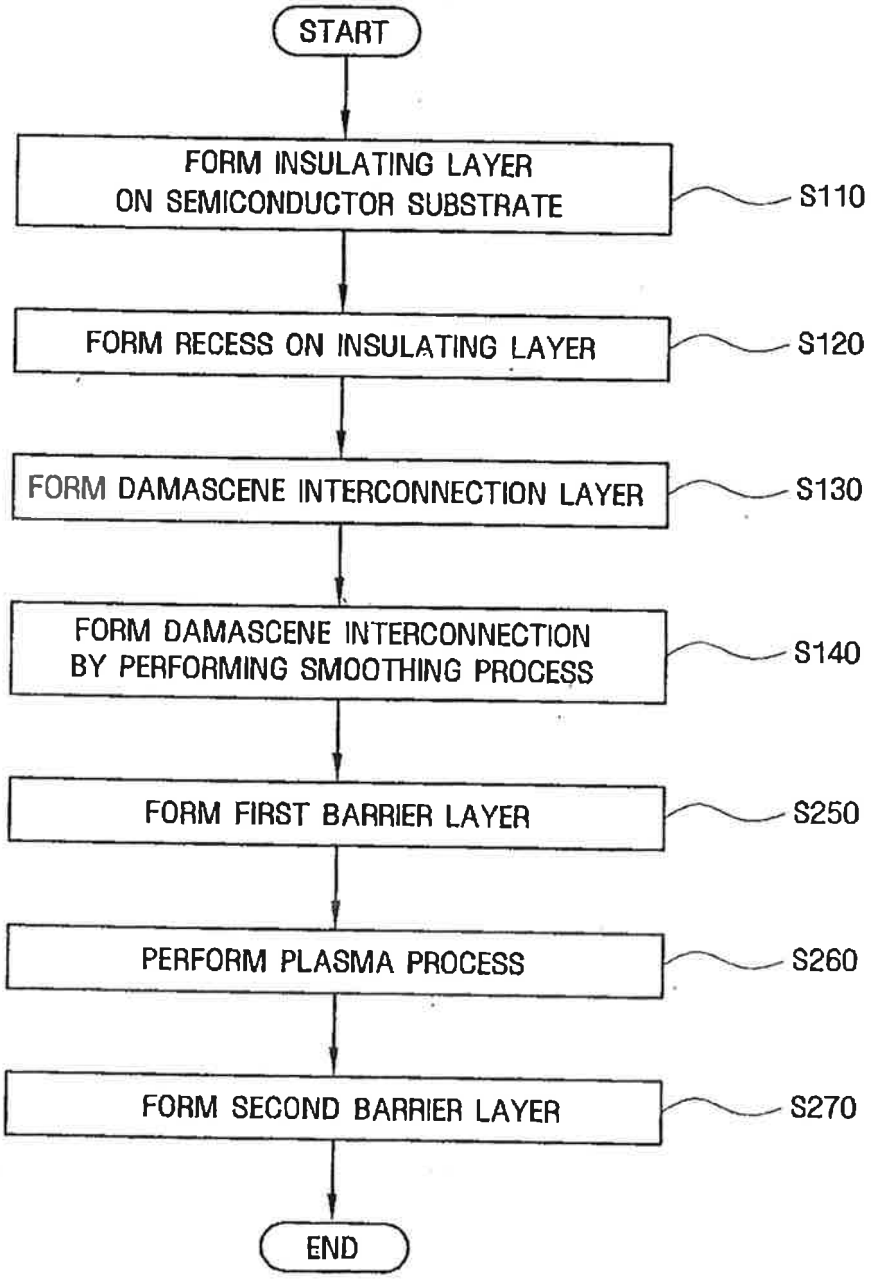

START
FORM INSULATING LAYER ON SEMICONDUCTOR SUBSTRATE
S110
FORM RECESS ON INSULATING LAYER
S120
FORM DAMASCENE INTERCONNECTION LAYER
S130
FORM DAMASCENE INTERCONNECTION BY PERFORMING SMOOTHING PROCESS
S140
FORM FIRST BARRIER LAYER
S250
PERFORM PLASMA PROCESS
S260
FORM SECOND BARRIER LAYER
S270
END

FIG. 11

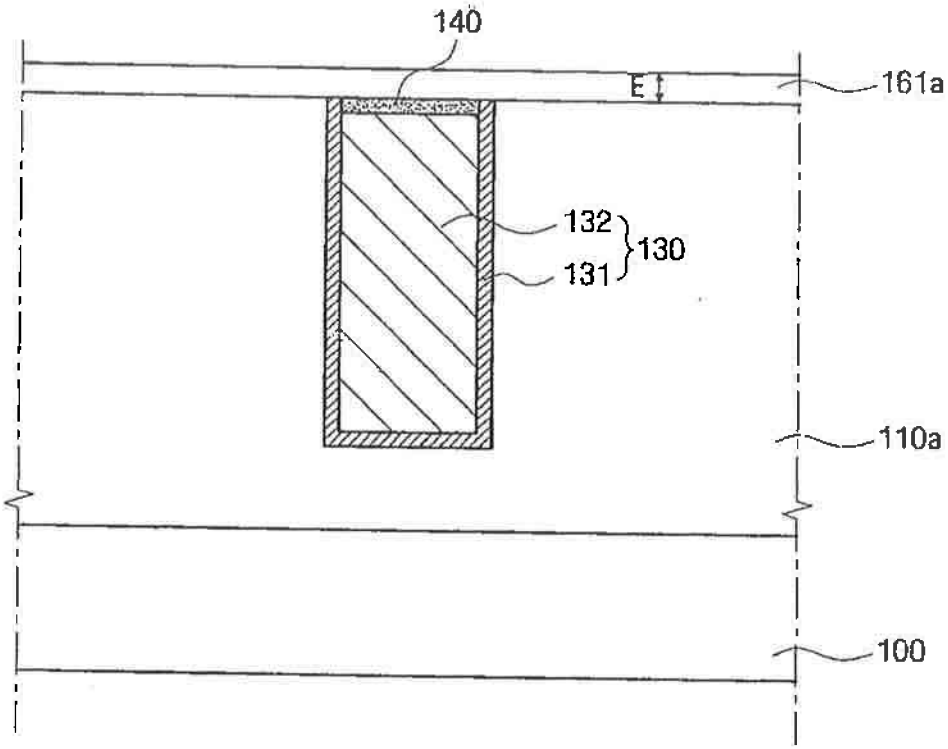


FIG. 12

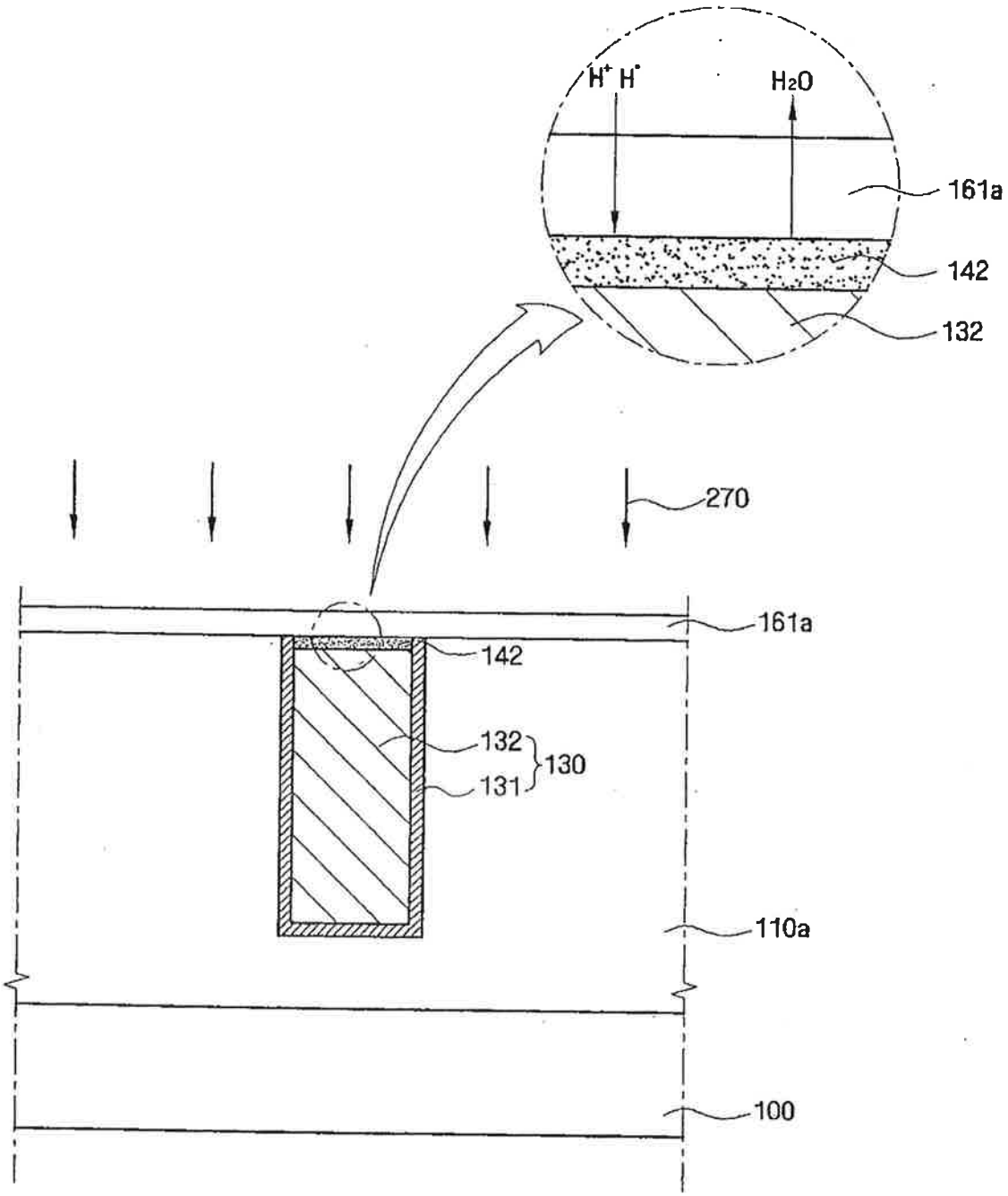


FIG. 13

