

Description

The invention pertains to the field of MOS, Metal/Oxide/Semiconductor and more particularly to a use of an electrically programmable MOS cell to implement a fuse.

The use of fuses in integrated circuits is very widespread, notably for the programming of read-only memories or to obtain a circuit configuration, after the breakdown of the fuse or fuses, that is different from the initial configuration. It is the case for example of integrated circuits for chip cards where the fuses, after breakdown, allow to block the access to certain circuit zones. In general, it is not possible to establish this configuration during the manufacture of the circuit, for access to these zones must be possible for testing the circuit and for its personalisation. It is only after this that the access to these zones must be prohibited. For this application, the security of the card is closely linked to an efficient breakdown of the fuses.

Other applications for fuses in integrated circuits are implemented, for example in high-capacity memories for redundancy, the defective columns (or lines) being replaced after breakdown of a corresponding fuse by supplementary columns (or lines).

There are various types of known fuses that can be used in integrated circuits notably in programmable memories where the recording is made by breakdown of a fuse or junction. The fuse is made in the form of a thin layer of metal alloy of nickel and chrome, or especially of polycrystalline silicon of better reliability destroyed by application of high power. The breakdown of the junction also needs well-controlled breakdown conditions with fairly high currents.

The main limitation of standard fuses is thus the need to implement high breakdown power, for example currents of 100 to 200 mA at 10 to 20 V. Now this is incompatible with development in the technology of integrated circuits where the trend is to reduce the consumption of circuits, and to reduce internal voltages and breakdown voltages of the diodes or junctions.

Thus it is more difficult with present-day technology to achieve the proper breakdown of a fuse in CMOS integrated circuits than in circuits of some years ago especially because the voltage applied during the breakdown must be far lower than before.

Other problems are also badly resolved, for example the parasite breakdown of fuses mounted in parallel with fuses to be broken down: indeed, during the breakdown of a fuse, the conduction of the breakdown control transistor may cause the "parasite" breakdown of an undesired fuse. The only way to resolve this problem consists in reducing the breakdown voltage, but this makes it more difficult to break down the desired fuse.

Another problem results from the breakdown of the fuse by electrostatic discharge. Indeed this breakdown takes place under conditions which currently approach characteristics required at the inputs/outputs of the circuits. Thus, the breakdown by electrostatic discharge may take place for 500V while the input/output voltages frequently reach 5000V. The use of fuses at the input/output pins and their breakdown during the application is thus impossible.

To overcome these drawbacks, integrated circuit designers have perfected electrically programmable (EPROM or EEPROM) MOS memory cells or "memory points" of which the logic state, circuit open (1) or on (0), is determined by the existence or not of charges accumulated at a floating grid

(unconnected). The programming of such a cell, that is to say the passage from the "circuit open" state to the "circuit on" state, is equivalent to shifting the threshold of conduction by these charges accumulated at the floating grid.

Such a cell with two logic states is equivalent to a fuse except as regards irreversibility. Indeed, the charges accumulated at the floating grid can be eliminated for example by heating the circuit, by radioactivity, by electromagnetic wave effect, or further through compensation of these charges by charges stored in the thin oxide of the cells, between the source and drain electrodes and the floating grid. Now for applications of the chip card type, all security relies on the fact that it must be impossible, after breakdown of the fuse, to bring it back to the logic state existing before the breakdown.

One can further refer to the state of the art constituted by the document IEEE - 1985 entitled "A new programmable cell utilizing insulator breakdown" pages 639 - 642 by N - SATO et al in which a BIC cell (Breakdown insulator cell) is described.

This cell comprises a thin insulating layer covering a contact zone on a diffusion layer N+, and an aluminium electrode connected to the insulating surface.

The programming of the cell is carried out by the application of pulses to the aluminium electrode in such a way as to break down the insulating layer, the electrode being then linked to the N+ region. This cell is intended for the implementation of PROM memories.

One can also refer to the state of the art constituted by the document Patent Abstract of Japan, vol 9, n° 170 of the 16th July 1985 in which FET transistors of a ROM memory plane have a floating

grid linked to the same potential as the control grid.

An object of the invention is the use of a fuse with a Metal/Oxide/Semiconductor structure which does not have the drawbacks of standard fuses in respect of the breakdown power values required and which does not have the drawbacks of MOS cells programmable from an initial state to another state by the storage of charges, as concerns security.

According to the invention there is proposed the use of an electrically programmable MOS cell to implement a fuse, the cell comprising two electrodes (A,S) formed by doping a substrate, a first grid (G2) formed by a polycrystalline silicon and partly covering one (A) of the two electrodes from which it is separated by a layer of thinned silicon in order to form a tunnel window (F), and a second grid (G1) separated from the first by a layer of oxide, the two grids (G1, G2) being interconnected in order to make it possible to apply an electric field of irreversible insulation breakdown of the oxide forming the window (F).

The invention will be understood more clearly and other characteristics will appear from the following description made with reference to the appended drawings :

- figures 1a and 1b show a sectional drawing of a known programmable MOS circuit with floating grid, and the equivalent symbolic electric diagram;
- figures 2a and 2b show a drawing of the MOS fuse with oxide breakdown usable according to the invention, and the corresponding symbolic electric diagram;
- figure 3 is the diagram of the assembly necessary for the breakdown of the fuse;
- figure 4 is a timing diagram of the corresponding control voltages.

Figure 1a shows a known electrically programmable and erasable MOS memory cell with tunnel effect: the silicon substrate is N+ doped to form firstly the source S, secondly the drain D, then is covered with a layer of silicon oxide, a grid FG of polycrystalline silicon called a "floating" grid because it is unconnected, and a second grid G at which there is provision for a contact point. The floating grid forms with the drain on a part of its length, a thin tunnel window F, typically with a thickness of 0.01 micrometer of oxide obtained at least partly by growth. The contact point of the grid G is connected to a line of words. As indicated hereabove, the programming of such a cell is obtained by tunnel effect, an intense electric field, typically 10 MV/cm, enabling the electric charges to go through the oxide window of the tunnel and to be stored at the floating grid FG. Following the direction of the electric field, the stored charges are either holes, or electrons. For a 0.01 micrometre oxide window, a voltage of 10 V has to be applied to the floating grid FG to obtain an electric field sufficient to enable the charges to go through by tunnel effect.

For this the voltage applied to the grid G by the "line of words" must be determined by taking account of the coefficient of capacitive coupling between the two grids G and FG. For example, if this coupling coefficient is equal to 0.5, the voltage applied to G must be equal to 20 V to obtain 10 V by capacitive coupling at the grid FG and trigger the tunnel effect, the drain being maintained at 0V. In the same way, it is sufficient to apply 20 V to the drain of the cell while maintaining the grid at 0V to trigger the transfer of charges by tunnel effect with an inverted electric field. Such a cell when it is "erased" (electrons stored

at the floating grid FG) has its threshold voltage VT_0 equal to about 5V; a "programmed" cell (holes stored at the floating grid) has its threshold voltage VT_1 equal to about 3V. If for the reading, a voltage of 2V is applied to the grid G, the erased cell does not conduct and the programmed cell conducts.

The oxide of the tunnel window between the grid FG and the drain is a very fragile element due to its small thickness. This structure of thin layer oxide between the drain and the grid to form the window is necessary so that the conduction by tunnel effect can take place. This effect takes place just before the electrostatic breakdown of the oxide occurs. For example, if the tunnel effect is triggered by an electric field comprised between 8 and 10 MV/cm, the breakdown of the oxide occurs for an electric field of about 12 MV/cm or even less if the electric field is applied suddenly. In EEPROM cells of this type, the voltage necessary during the programming is increased very slowly, 20 V/ms, to prevent the breakdown of the oxide. Figure 1b shows the equivalent electric diagram of this cell with source S, drain D, grid G and intermediate floating grid FG, at a very small distance (0.01 micrometre) from the drain on a portion of its length.

To make the fuse, the invention uses a structure that is quite similar, but instead of programming the cell as described hereabove, the oxide of the tunnel is "broken down", a low resistance is then set up between the drain and the grid FG. For this, the two grids G and FG are interconnected and, preferably, instead of raising the programming voltage slowly, this voltage is raised rapidly. The interconnection of the two grids enables the elimination of the capacitive coupling between the two grids by setting up a direct link between

them. Furthermore, one of the terminals of the resistor formed by the tunnel oxide can be grounded. Thus, under the same conditions of applied voltage as for the cell described hereabove used in a memory, an electric field of 20 MV/cm is obtained between G (and FG) and the drain D, which is quite sufficient to obtain the breakdown of the oxide in the window. Furthermore, the fast application of the voltage makes it possible to obtain a very efficient breakdown of the tunnel oxide and hence the lowest possible resistance between drain and grid. This condition of fast application of the breakdown voltage is not indispensable because, with voltages of this amplitude the tunnel oxide will in any case undergo breakdown; nevertheless, when the voltage is applied more slowly, the breakdown is less definite and a slightly higher resistance may remain between drain and grid.

Figure 2a gives a sectional view of the corresponding structure of the fuse similar to that of the memory cell, but in which the two grids are interconnected. They are marked G1 and G2 in this figure because there is no longer any "floating" grid. The breakdown voltage is applied between the terminal B (grids) and the terminal A (connection of drain D in figure 1a). The doped zone corresponding to the source S of figure 1a is not connected. Figure 2b is the equivalent symbolic electric diagram.

Figure 3 illustrates the assembly used to achieve the breakdown of the oxide which makes the fuse go from its initial "open" state to its "on" state when necessary, this transformation being irreversible: the fuse F1 represented as shown in figure 2b therefore has an unconnected terminal, its terminal A connected to a supply voltage V_{pp} through a transistor T1, of

which the grid is connected to a control terminal, COMVpp, and its terminal B connected to the ground through a transistor T2 of which the grid is connected to a control terminal COMVss. To break down this "fuse", the control signal of T2, COMVpp, is increased up to the supply voltage V_{pp} , whereas the control signal COMVss initially at the high state, is brought to 0. At the instant t1 in the timing diagram of figure 4, the transistor T2 is blocked and T1 starts to conduct. The voltage at the node B remains floating. No electric field is then generated through the tunnel oxide. At the instant t2, the voltage at the node A is $V_{pp} = 20V$ and the voltage at the node B is 0V. An intense electric field 20 MV/cm therefore exists in the tunnel window which rapidly breaks down. A leakage towards the ground of the current detector appears; this makes the potential at the node A go down. The breakdown phenomenon then stops.

During detection, the voltage applied to the grid of T1, COMVpp = 0V and the transistor T1 is blocked. The voltage applied to the grid of T2, COMVss = 5V (T2 must just be made conductive), which takes the grids (node B) of the fuse cell F1 to Vss (0V).

- when the oxide of the tunnel window is intact, there is no current in the fuse cell F1, and the current detector indicates this absence of current;
- when the oxide is broken down, there is a low resistance between A and B, which induces a current I towards the ground of the detector, a different state is then detected.

This phenomenon of breakdown is irreversible. No heating (annealing) of the circuit can change the structure of the broken down oxide. Furthermore, since the effect is not a storage of charges, no test on the discharge or storage of charges in the thin

oxide of the cell can affect the state of the fuse cell. This breakdown is fast, 1 ms, as compared with the programming time of a cell (figure 1a) of about 5 ms, or with the time needed for the breakdown of a standard fuse of about 100 ms. No power is needed, and the internal generator of voltage V_{pp} being used for the breakdown of the oxide, it is possible in the context of an application to integrated circuits for cards, to provide for the burn-out of one or more fuses of the circuit as soon as an anomaly is observed, without a fraudulent person being able to prevent it.

Such a structure can also be used to build EPROM memories with a single programming. Thus memory cards may be personalised by irreversible changes in the structure of the circuits by breakdown of oxide. Usually, as indicated hereabove, when the personalisation is obtained by special arrangements during manufacture, it necessitates costly and slow masking operations of little flexibility, and when the personalisation is done by electrical programming of EPROM or EEPROM cells, the resulting structures are vulnerable.

In practice to convert a cell as shown in figure 1a into a fuse as shown in figure 2a, it is enough during the operation for depositing silicon oxide on the floating grid to reserve a zone for the contact between the two grids, the contact being obtained when the polycrystalline silicon of the second grid is deposited in the reserved zone. Another possibility would be to provide for accessible contact points on the floating grid of all cells of this type, and to connect these points to the lines of words only of the cells used as fuses.

Claims

1. Use of an electrically programmable MOS cell to implement a fuse, the cell comprising two electrodes (A,S) formed by doping a substrate, a first grid (G2) formed by a polycrystalline silicon and partly covering one (A) of the two electrodes, from which it is separated by a layer of thinned silicon in order to form a tunnel window (F), and a second grid (G1) separated from the first by a layer of oxide, the two grids (G1, G2) being interconnected in order to make it possible to apply an electric field of irreversible insulation breakdown of the oxide forming the window (F).
2. Use in accordance with claim 1, characterised by the fact that the thickness of the window is of the order of 0.01 micrometres, the electrical insulation breakdown field applied where necessary between the grid and the electrode being above 12 MV/cm.
3. Use in accordance with either of the preceding claims, the cell being applied to memory cards so that after the personalisation of the cards access to certain zones of the circuits of these cards will be irreversibly blocked.
4. Use in accordance with any one of claims 1 to 3, a plurality of the cells being applied to a memory network in order to form its memory points, these memory points being thus programmable by insulation breakdown of oxide.



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