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(54) **Title:** METHODS OF ISOLATING ARRAY FEATURES DURING PITCH DOUBLING PROCESSES AND SEMICONDUCTOR DEVICE STRUCTURES HAVING ISOLATED ARRAY FEATURES

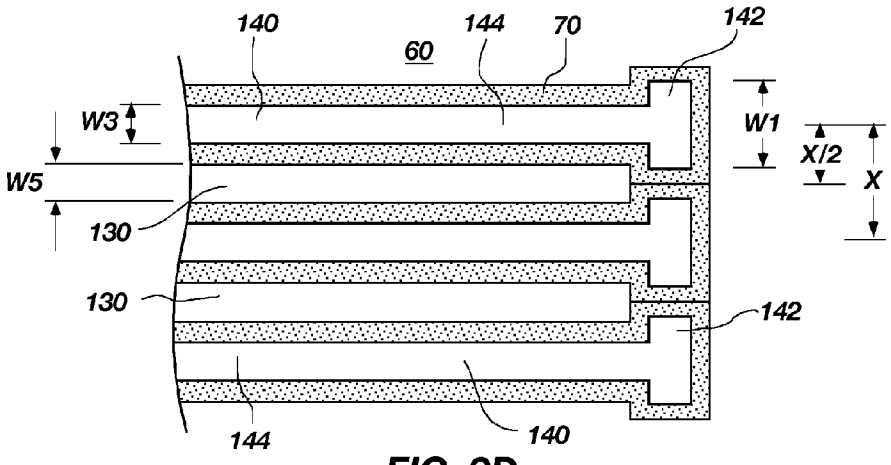


FIG. 2D

(57) **Abstract:** Methods of isolating spaces formed between features in an array during a pitch reduction process and semiconductor device structures having the same. In one embodiment, ends of the features are wider than middle regions of the features. During the pitch reduction process, spacer sidewalls formed between adjacent ends of the features come into substantial contact with on another, isolating the spaces between the features. In another embodiment, the features have a single width and an additional feature is located near ends of the features. Spacer sidewalls formed between adjacent features and the additional feature come into substantial contact with one another, isolating the spaces between the features.

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