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PATENT SPECIFICATION

DRAWINGS ATTACHED

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COMPLETE SPECIFICATION

Improvements relating to Semiconductor Devices

We, TEXAS INSTRUMENTS INCORPORATED, a Corporation organized according to the laws of the State of Delaware, United States of America, of 13500 North Central Expressway, Dallas, Texas, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to semiconductor devices, and more particularly to transistors, integrated circuits, or the like having metal contacts, and to methods for making such devices having metal contacts.

Electrical contacts to semiconductor devices must be composed of materials which have good chemical, electrical, thermal and mechanical properties when applied to semiconductor surfaces. While problems in making contacts exist for all semiconductors, the selection of contact material is especially difficult when the semiconductor is silicon, such as in planar transistors and integrated circuits where silicon is most commonly used. First, it is appropriate to discuss the restrictions within which a contact metal for a silicon planar device must be selected.

In planar semiconductor devices, usually a silicon oxide or glass coating overlies the silicon surface except in the actual contact areas, this coating functioning to passivate the junctions and provide an insulating base for expanded contacts and interconnections. Particularly in integrated circuits, strips of conductive material extend from one semiconductor region up over the oxide coating and across various regions and junctions of the device to contact another region. Accordingly, the contact material must exhibit good adherence to silicon and to silicon oxide or glass, but yet must not produce any undesirable reaction with, nor penetrate, the silicon or oxide.

The most successful techniques thus far devised for the manufacture of semiconductor devices and particularly silicon transistors and integrated circuits, rely heavily upon photoengraving to form diffusion masks, define contact areas, etc., and upon evaporation to deposit metals. Therefore, to be compatible with the most convenient manufacturing methods, the contact metal selected should permit the use of photomasking and etching, and also should permit evaporation as a technique for deposition. These techniques for applying the contact material are most effective when very thin films are used, and since the other dimensions of the conductor are limited in size by the desired electrical characteristics of the device, the contact material must have a high conductivity to prevent the introduction of series resistance.

There is a continuing trend in semiconductor technology to fabricate devices operable at higher frequencies and capable of switching at higher speeds. Of necessity, the physical dimensions of the device must be made very small to provide these characteristics. For example, the part of a high frequency transistor which functions as the emitter region may occupy one-tenth square mil or less on the face of a semiconductor wafer, and may be only a few hundredths of a mil in depth. Connection cannot be made directly to such a region with a bonded wire, so that the contact area must be expanded out over the oxide to make room for attaching an external lead requiring the contact metal to be unreactive with the oxide as above. In transistors of this type, the oxide layer overlying the base region is very thin

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because of the short time during which the device can be held at temperatures which promote oxide growth. Typically, this oxide layer would be less than 2000 Å, compared to almost 10,000 Å over the collector region. Therefore, degradation of the device due to penetration of the contact metal through the oxide to the junctions would be particularly severe in high frequency devices. Also, the contact metal must not tend to penetrate into the semiconductor surface since very slight penetration would obliterate the shallow region.

At the present time, connections are made from a semiconductor wafer to external circuitry by means of fine wires bonded to metallized contact areas on the wafer and to electrodes in the device package by thermocompression techniques. Gold wire is preferable in one embodiment because of its very high conductivity, its ductility further permitting easy handling and bonding even with the extreme small diameters necessitated by the semiconductor device geometries. Typically, the gold wires used would be only about one mil in diameter. Aluminium has been proposed for use as the lead wires and is useful in an all aluminium system, but it is more difficult to bond than gold because of the formation of a film of aluminium oxide in air. Also, aluminium forms an undesirable compound when in contact with gold, as will be explained below. Again, the use of the preferred manufacturing techniques for semiconductor devices imposes a constraint upon the metal used for the contacts, in this case the requirement that the metal be easily bonded with gold wire. Hence both gold and aluminium may be used to advantage, but gold is considered the preferred embodiment.

The contact metal should not form an alloy with the semiconductor material at temperatures used in bonding leads to, or packaging, the device. Formation of such an alloy would result in the undesirable penetration into the shallow semiconductor regions. As mentioned above, this limitation prevents the use of gold in direct contact with silicon because of its low eutectic temperature with silicon, 377°C, a temperature often exceeded in depositing contact metals, in bonding or in hermetically sealing the device. In like manner, the contact metal should not have a melting point below that to which the device would be exposed in subsequent processing and operation.

An additional requirement for a contact metal is that it provide an ohmic and low resistance contact to the semiconductor surface. If the device is made of silicon, particular problems occur because of the inherent properties of the material, the propensity of this semiconductor for forming an oxide, etc. Moreover, if the contact metal used is a donor or acceptor in the semiconductor, it must have a low solubility so that the tendency to form a junction can be thwarted by heavy doping of the contact area.

With these restrictions, most metals are totally unsuited for use alone as expanded contacts to silicon devices. For example, the best conductors, silver, copper and gold, do not adhere well to silicon oxide, and in addition gold forms a eutectic with silicon at low temperature, degrading device characteristics. Also silver oxidizes rapidly so a bond cannot be made easily, while copper diffuses very rapidly in silicon. Examining the other metals, it will be noted that tungsten and molybdenum do not permit bonding with gold wire, the former being additionally difficult to etch in a controlled manner using solvents compatible with photoresist polymers, silicon oxide, etc. Rhodium and iridium do not adhere to silicon oxide and are not readily etched. Zinc has a low melting point, does not adhere to silicon oxide, and has an undesirably high vapour pressure. Cobalt is difficult to evaporate. Nickel does not adhere well to silicon oxide and is difficult to bond with gold wire. Iron cannot be readily bonded. Platinum and palladium adhere poorly to silicon oxide, and are difficult to be bonded with gold wire. Tin has a very low melting point. Chromium cannot be readily etched nor bonded with gold wire, is too porous, and is unduly reactive with silicon oxide. Tantalum is even more difficult to etch and bond and is even more reactive with silicon oxide than chromium. Lead exhibits poor adherence to silicon oxide. Vanadium, zirconium and titanium are very poor conductors, react with silicon oxide, and are virtually impossible to bond with gold wire, while the latter two suffer the additional disadvantage of being difficult to etch. Indium has a very low melting point. Antimony, arsenic, and gallium are doping impurities with high solubilities and/or diffusion rates in silicon, while gallium melts at slightly above room temperature.

The only single metal which is at all suitable for contacts and interconnections in silicon planar transistors and integrated circuits is aluminium, which has been used widely for such purposes. Aluminium thin films of excellent quality are easily applied to semiconductor devices by evaporation and photoresist techniques, and contacts of this metal are readily bondable with gold or aluminium wires. Aluminium is the fourth best conductor, and its adherence to silicon and silicon oxide is possibly unsurpassed.

Nevertheless, despite its several advantages for use as a contact material in semiconductor devices, aluminium has several disadvantages. The first and most prominent is that when gold wires are bonded thereto an intermetallic compound of gold and aluminium

is formed. This compound, $AuAl_2$, exhibits a purple colour, and is commonly referred to in the industry as the "purple plague". When gold and aluminium are in contact, $AuAl_2$ forms rapidly at 300°C, which is a temperature nearly always exceeded in making connections to or encapsulating semiconductor devices. While $AuAl_2$ is a reasonably good conductor, it has extremely poor mechanical properties. It is brittle, and device reliability decreases as a result of its formation.

The second problem with aluminium is encountered when it is used as an expanded contact or interconnection, or when it is applied over the entire surface of a silicon planar device and then selectively removed except in desired contact areas. There is evidence that the application of aluminium films by means of evaporation often results in electrical degradation of the device in the form of shorts, high saturation currents, decreased gain, and undesirably low reverse breakdown characteristics. This degradation is particularly severe when the thermal oxide and/or glass coating over the junction is thin, which is usually the case in high frequency planar transistors. The origin of this degradation is obvious if the oxide coating contains pinholes; however, recent work indicates that aluminium has a tendency to cause electrical degradation in excess of that which can be attributed to pinholes in the oxide. It is believed that aluminium has a tendency to penetrate the protective oxide, probably due to a chemical reaction between aluminium and silicon oxide. This chemical reaction, expressed by the formula $3\ SiO_2+4Al \rightarrow 2Al_2O_3+3Si$, is very energetically favourable, the free energy of formation under standard conditions, $\Delta F°$, being -184 k cal/mole for this reaction. For aluminium the $\Delta F°$ for oxide formation is about -376, whereas for silicon it is -192, the difference providing the -184 figure. The excellent adherence of aluminium to silicon oxide is due to this reaction. Presumably, aluminium films applied to silicon oxide surfaces are held firmly due to an interfacial reaction of this type, but it is interesting to note that the reaction is also probably responsible for the electrical degradation that is observed.

Efforts have been expended toward finding an alloy of metals which will satisfy the requirements for silicon contacts, but the possibility of finding a suitable material by this approach is made difficult by the necessity that the contact metal is preferably applied by evaporation. The constituent metals selected must have vapour pressures very nearly equal or the alloy as such cannot be formed on a substrate by evaporation. Even if the vapour pressures are very close, the material applied by evaporation may well resemble a mixture rather than an alloy, and heat treatment at very near the melting point of the alloy is necessary to reform the original composition. Ordinarily such temperatures are incompatible with a semiconductor device. In any event, the metals in an alloy may exhibit a tendency to each preferentially in the photoengraving processes.

In order to avoid the problem of the formation of $AuAl_2$, aluminium has been proposed for use as the lead wires. While this avoids formation of the compound at the contact, the "plague" will form within the device package at the header post or tab electrode, which are required to be gold plated by most semiconductor device users, particularly the military.

Attempts to find a single metal or alloy as a substitute for aluminium have not been entirely successful for the reasons set forth above. Thus, it becomes necessary to employ a multilayered or sandwich type contact. For example, chromium and gold have been proposed as a contact, in which case a thin layer of chromium is applied first then a layer of gold is deposited over the chromium. Unfortunately, chromium exhibits relatively poor electrical contact to silicon, and is not itself a very good conductor. In addition, chromium does not prevent the penetration of gold into the silicon, and in fact this penetration is used to promote lower contact resistance, the CrAu films being sintered after deposition. Also, chromium is subject to severe undercutting during etching in the photoengraving process, since chromium is difficult to etch in a slow, controlled manner.

With the difficulties heretofore encountered in mind, it is an object of this invention to provide semiconductor devices having improved contacts and interconnections, particularly silicon planar transistors and integrated circuits of the type having silicon oxide coatings thereon.

In accordance with a preferred embodiment of our invention, a combination of metals almost uniquely commensurate with the above object is found to be molybdenum and gold. In accordance with another embodiment a desirable and useful combination is achieved by the use of molybdenum and another malleable metal, aluminium. There are particular applications in which aluminium may be used in place of gold, but for the ~~general~~ general analysis gold is considered more desirable. A thin film of molybdenum is first applied to the surface of the semiconductor device, typically over the entire face of a silicon wafer having a silicon oxide coating with openings etched in contact areas. Then the molybdenum is covered with a thin film of malleable metal, in this instance gold, and thereafter the gold and molybdenum are etched away in unwanted areas, leaving the desired pattern of contacts and interconnections on the silicon surface and on the oxide.

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Gold is used on top in the preferred embodiment because it is of excellent conductivity, being even higher than aluminium, and because of the ease with which it can be deposited by evaporation. Moreover, gold lends itself to photoresist etch procedures, and naturally is easy to bond with gold wire, producing no deleterious effects at the contact-to-wire interface. The underlying molybdenum layer is necessary to hold the gold to the surface because, as mentioned above, gold does not adhere well to silicon oxide. Further, gold makes poor electrical contact to silicon, as well as forming the gold-silicon eutectic at low temperature. Molybdenum is particularly well suited in this environment because it adheres well to silicon oxide, can be etched in a controlled manner with an etchant not incompatible with other materials present, and does not alloy with and is virtually impervious to gold. Moreover, the ΔF° for molybdenum oxide is less than that of silicon, so the reaction is not detrimental to a silicon oxide coating, although the adherence thereto is acceptable. Molybdenum makes good electrical contact to silicon if the contact region is heavily doped, preferably above about 10^{21} per cc for either N- of P-type, but yet does not form an alloy with the silicon surface so that shallow junctions are not degraded. In this regard, it might be noted that a virtually "alloyless" contact is formed, the molybdenum not alloying with the silicon and the gold not alloying with the molybdenum. It is for this reason that the silicon surface must be free of silicon oxide or other foreign matter where contacts are to be made, and the evaporation procedure used must not permit the formation of molybdenum oxide before gold is deposited. In spite of this, the molybdenum and gold contacts of this invention may be deposited with the silicon wafer being at reasonably low temperatures.

The present invention is a semiconductor device comprising a body of semiconductor material having an insulating coating over part of one surface thereof, a layer of molybdenum deposited on a part of said one surface which does not have said insulating coating and extending over at least a portion of said insulating coating, and a layer of a second conductive material deposited on said layer of molybdenum.

The present invention is also a semiconductor device comprising a body of semiconductor material having an insulating coating over one surface thereof, said body comprising a plurality of monocrystalline regions adjacent said one surface and spaced apart along said surface, each region including at least one P-N junction extending to the surface beneath said insulating coating, the coating defining openings over each said regions and extending across said face between the regions, and multilayered contacts to said regions and interconnections between said regios, said multilayered contacts comprising a layer of molybdenum on said surface within said openings and extending over the coating across the junctions to others of the openings, and a layer of conductive material overlying said layer of molybdenum.

The present invention is also a method of making a semiconductor device, comprising providing a semiconductor wafer having a region adjacent one surface thereof with a P-N junction between said region and other semiconductor material of the wafer extending to said surface beneath an insulating coating which is provided on said surface with a small opening over said region, and including the steps of depositing a layer of molybdenum upon said surface of the wafer over said insulating coating and onto said opening over said region, depositing a layer of conductive material upon said surface over the layer of molybdenum and selectively removing the layers of molybdenum and conductive material from areas surrounding said opening.

The present invention is also a method of making a semiconductor device, comprising providing a silicon wafer having a region adjacent one surface thereof with a P-N junction between said region and other semiconductor material of the wafer extending to said surface beneath a silicon oxide coating which is provided on said surface with an opening over said region, and including the steps of depositing a thin layer of molybdenum upon said surface of the wafer over said silicon oxide coating and onto the silicon surface in said opening, depositing a thin layer of gold upon said surface over the thin layer of molydenum, selectively applying an etch resistant coating to said surface over the layers of molybdenum and gold to cover the area above said opening and an expanded area extending from the area above said opening, and etching the layers of gold and molybdenum from said surface of the wafer in the regions not covered by said etch resistant coating.

The present invention is also a method of making a semiconductor device comprising the steps of providing a semiconductor wafer, forming a plurality of circuit components in the wafer adjacent one surface thereof with regions of such components having contact areas exposed through openings in an insulating coating on said surface, depositing a thin layer of molybdenum upon said surface, depositing a thin layer of conductive material over the layer of molybdenum, selectively removing portions of said layers from the surface of the wafer to provide contacts to said contact areas and interconnections overlying said insulating coating between certain ones of said contact areas.

Embodiments of the invention will now be described, by way of example, with reference to the accompanying drawings, wherein:

Fig. 1 is a plan view of a wafer of semiconductor material having a planar transistor formed therein, with holes cut in the oxide coating for application of contacts;

Fig. 2 is an elevational view in section of the semiconductor wafer of Fig. 1 taken along the line 2—2;

Fig. 3 is a schematic representation of an evaporation chamber suitable for carrying out the method of applying contacts of this invention;

Fig. 4 is an enlarged elevational view in section of a segment of the semiconductor wafer of Fig. 1, also along the lines 2—2, after contact material has been applied;

Fig. 5 is a greatly enlarged elevational view in section of a portion of the view of Fig. 4 after the contacts have been defined;

Fig. 6 is a plan view of the transistor wafer of Fig. 1 after the contacts and bonding pads have been applied;

Fig. 7 is an elevational view in section of the wafer of Fig. 6 taken along the line 7—7;

Fig. 8 is a pictorial view of the transistor of Fig. 6 mounted on a header;

Fig. 9 is a greatly enlarged elevational view in section of one of the contacts of this invention illustrating a severe undercutting situation; and

Fig. 10 is an elevational view in sectional of an integrated circuit using the contacts and interconnections of this invention.

With reference to Figs. 1 and 2, there is shown a semiconductor wafer 10 having a transistor formed therein including base and emitter regions 11 and 12, respectively, the remainder of the wafer providing the collector region. The transistor is formed by the planar technique, using successive diffusions with silicon oxide masking. This process leaves an oxide coating 13 on the top surface of the wafer, with the coating over the collector being thicker than over the base region, leaving the stepped configuration seen in Fig. 2. For high frequencies, the geometry of the active part of the transistor is extremely small, the elongated emitter region 12 being perhaps 0.1 to 0.2 mil (0.0002 inch) wide and less than a mil long. The base region is about one mil square. A pair of holes 14 and 15 are provided for the base contacts, and a hole 16 for the emitter contact, this latter opening being the same as used for the emitter diffusion. Due to the extremely small size of the actual base and emitter contact areas, one or two tenths of a mil in width, the contacts must be expanded out over the silicon oxide to facilitate bonding of leads for the base and emitter connections, as will be explained below. It may be noted from Fig. 4, which is approximately to scale, that the thickness of the oxide coating 13 over the base region 11 is much less than over the collector region. Also, the shallow depth of the diffused regions, particularly the emitter, may be seen. The large volume of metal compared to that of the oxide or diffused regions emphasizes the problems which would be encountered if any reaction or alloying with the oxide or silicon occurred. The bulk of the wafer 10 forms a collector region 17, and the collector contact may be applied to the lower face of the wafer. The size of the semiconductor wafer is selected for convenience in handling, with a typical size for the wafer 10 being 30 mils on each side and 4 mils thick (these dimensions are not to scale in the drawing). Typically, the wafer 10 is merely a small undivided part of a large slice of silicon, perhaps one inch in diameter and eight mils thick, during all of the process steps described below, and this slice is scribed and broken into individual wafers or dice only after the contacts are applied.

With reference to Fig. 3, a method of depositing the molybdenum and gold or aluminium contacts of this invention will be described. The following description will be directed to the use of gold as the top contact layer; however, necessary deviations to accommodate aluminium will be pointed out. The apparatus used for this deposition includes an evaporation chamber 20 which comprises a bell jar 21 mounted on a base plate 22. An opening 23 in the base plate is connected to a vacuum pump for evacuating the chamber. A stainless steel sheet 24 is mounted in a thermally isolated manner above the base plate 22 by means not shown, and serves as the work holder for a plurality of silicon slices 25 each of which includes at its upper face, in an undivided form, dozens or hundreds of the transistors of Figs. 1 and 2. Below the sheet 24 a bank of quartz infrared tubes 26 are positioned, these functioning to heat the sheet and the slices to any desired temperature in the general area of 200—400°C and to hold the slice temperature at the selected point with a fair degree of precision. A suitable temperature control, including a thermocouple and a feedback arrangement (not shown) is provided for this purpose. About four inches above the sheet 24 there is positioned a tungsten coil 27 for evaporating a charge 28 of gold, and also a molybdenum strip 29 which is itself evaporated. The technique used for evaporating molybdenum is somewhat unusual and warrants elaboration. The strip 29 is perhaps 10 mils thick, 3 inches long and one inch wide, while in the centre its width is constricted to about one-half inch. Current is passed through the length of the strip 29 until the central part heats up to just below

its melting point and begins to evaporate, but care is exercised to insure that the strip does not melt completely through at its centre. The strip 29, as well as the tungsten coil 27 and the IR tubes 26, are selectively energized by conductors (not shown) brought out through the base plate 22.

The contacts are deposited utilizing the apparatus of Fig. 3 by first placing the slices 25 on the work holder, then evacuating the chamber to about 6×10^{-6} mm of mercury. The slices, of course, have transistors or the like formed in the top surface as set forth above, and the holes for contacts have already been cut. A careful cleaning procedure for the slices, as set forth below, has been followed prior to this deposition of contacts. With the slices in place and a vacuum pulled, the IR tubes 26 are energized to bring the temperature of the sheet 24 and the slices 25 up to about 300 to 350°C. The molybdenum strip 29 is then energized by electric current and a molybdenum film 30 as seen in Fig. 4 is deposited upon the slices 25 entirely over the top surfaces thereof to a thickness of about 6 to 11 microinches. When the proper thickness is reached, the energization of the strip 29 is ceased. The power applied to the infrared tubes 26 is decreased slightly so that the sheet 24 and slices 25 cool to about 250 to 300°C, and the tungsten filament 27 is then energized to deposit a gold (or aluminium) film 31 to a thickness of perhaps 15 to 40 microinches upon the entire top face of each slice over the top of the molybdenum film 30. The deposition of malleable metal (gold) should be done as soon as possible after deposition of molybdenum because there appears to be a tendency for a film of molybdenum oxide, and/or a hydrocarbon film, to form over the molybdenum due to oxygen and oil residue in the vacuum system. Preferably the malleable metal (gold) evaporation is done within five minutes of the end of the molybdenum evaporation, or as soon as the slices have cooled from the temperature used for molybdenum evaporation to that used for gold evaporation. With the deposition of the films 30 and 31 complete, the slices are removed from the evaporation chamber 20 for selective removal of the molybdenum-gold coating in the undesired areas by using photographic techniques.

The slice cleaning procedure used prior to the evaporation will now be described. Unlike aluminium, molybdenum forms no liquid phase with the silicon substrate at reasonably elevated temperatures during evaporation. Thus, the silicon-molybdenum reaction is limited and for this reason the silicon surface should receive a careful pre-evaporation cleanup which leaves it very clean to insure good ohmic contact and mechanical adherence. An example of a recommended pre-evaporation cleanup will thus be given. The silicon slices, with transistors or the like formed therein and contact areas defined by etching, are placed in concentrated sulphuric acid at 150 to 200°C for about ten minutes, then rinsed in deionized water. The slices are then placed in boiling nitric acid for about five minutes, and again rinsed in deionized water. Thereafter, the slices are dipped in dilute hydrofluoric acid (or a 10% solution of ammonium bifluoride) for about six seconds, rinsed in cold deionized water for about twenty minutes, rinsed in acetone and dried, and then moved immediately into the evaporation chamber for pump-down and evaporation. In this cleanup technique, the function of the hot sulphuric acid is to remove all organic materials from the exposed surface of the silicon and silicon oxide. Such organic materials may be the residue from the photoresist polymer used in forming the transistor. The nitric acid removes the sulphate residue from the previous step. The hydroflouric acid insures that all oxide is removed from the silicon surface in the contact areas, and this likewise removes some of the oxide coating 13, but since the oxide coating 13 over most of the device is many times thicker than the residue over the base and emitter contact areas, this coating 13 remains essentially intact.

After removing the slices from the evaporation chamber, the excess portions of the molybdenum-gold coating 30—31 are eliminated by subjecting the silicon slices to a selective photoresist masking and etching treatment. A thin coating of a photoresist polymer, Eastman Kodak (Registered Trade Mark) KMER for example, is applied to the entire top surface of the wafer or slice. The photoresist is exposed to ultraviolet light through a mask which allows light to reach the areas where the molybdenum-gold film is to remain. The unexposed photoresist is then removed by developing in a photodeveloping solution. At this point, a layer 32 of photoresist overlies the portion of the molybdenum-gold coating which is to form the emitter contact and expanded lead as seen in Fig. 5. A similar mask would appear over the portion of the metal coating which is to form the base contacts and expanded lead.

The slice is now subjected to two etching solutions, the first one for the gold layer 31 and the second for the molybdenum layer 30. The gold layer is etched by a cyanide solution at about 70°C for about 15 to 45 seconds. A suitable cyanide etch solution is an aqueous solution of 60 grams per litre of Metex Aurostrip supplied by McDermid Incorporated of Waterbury, Connecticut. The slices are rinsed in water after the cyanide etch to prevent the evolution of toxic gas in subsequent processing. The gold etchant must operate in a relatively slow, controlled manner

so that the slices can be removed from the solution as nearly as possible to the exact time when the undesired gold has been removed but before undercutting of the gold occurs to any appreciable extent. The most common gold etchant, aqua regia, is not suitable since it is detrimental to the photoresist material. After the gold etching step, the excess molybdenum is removed by an etchant which likewise operates in a slow, controlled manner and which does not tend to oxidize molybdenum. A phosphoric acid solution is excellent for this purpose, and may comprise 70 parts phosphoric acid, 15 parts acetic acid, 3 parts nitric acid, and 5 parts deionized water. The phosphoric acid in this solution quickly removes any molybdenum oxide already in place or formed during the etching bath so that the entire etching time is occupied with removal of molybdenum, not molybdenum oxide. Thus, a time may be selected which coincides as nearly as possible with complete removal of the molybdenum coating, no leeway being needed for the variable of molybdenum oxide removal. At a temperature of 50°C, removal of the molybdenum coating 30 is effected in about 20 seconds with this phosphoric acid solution. The photoresist mask such as the layer 32, which has remained intact through these two etching steps, is now removed by rinsing in a solvent such as methylene chloride. An enlarged view of the emitter contact area would appear as in Fig. 5, where the removed portions of the metal coatings 30 and 31 are dotted. It is seen that very little undercutting occurs.

At some point in the process after deposition of the molybdenum and metal (gold) layers, it has been found advantageous in some cases to heat the slices to about 400 to 450°C for perhaps one-half hour to improve adherence of the layers to the slices.

Following the selective removal of the molybdenum-gold contact material, the slices are secured face down on glass slides with wax and the back or collector sides are etched with HF and nitric acid to reduce the slice thickness down to about 3 to 4 mils. After removing from the slides, the slices are scribed on the top face, and then broken into individual chips or wafers 10. Each wafer will have a contact pattern as seen in Fig. 6. A base contact land or bonding pad 36 is provided on top of the oxide, and two fingers or strips extend over the base-collector junction into the base contact holes 14 and 15. Likewise, an emitter contact land 37 or bonding pad is provided, and a single strip 38 extends over to make the emitter contact in the hole 16. The fingers or strips are very narrow, about one or two tenths of a mil or less, and so excellent definition or resolution is absolutely necessary. The pads 36 and 37 are large enough to permit bonding of 0.7 to 1 mil gold wires thereto.

The wafer 10 is mounted on a header 38 by a suitable solder material 39 as seen in Fig. 8, and gold wires 40 and 41 of perhaps 0.7 mil diameter are ball bonded to the base and emitter pads 36 and 37, respectively. The wires are then bonded to posts 42 and 43 which extend through the metallic header but are insulated therefrom. The collector region 17 of the transistor is thus ohmically connected to the header 38, which forms the collector electrode. A metallic can is thereafter sealed to the header to provide a hermetically sealed space for the transistor wafer. The operations of bonding leads to the pads and bonding the wafer to the header require the wafer to be subjected to temperatures of perhaps as high as 450°C. At such temperatures direct contact between gold and silicon would be disastrous to the device, such contact being avoided in this invention by the interposition of the layer of molybdenum. The impossibility of bonding wires to the actual base and emitter contact areas, and therefore the necessity for the expanded contacts and lands, is apparent in Fig. 8.

Returning now to the problem of etching away the unwanted portions of the metal coatings, the difficulties encountered when undercutting occurs may be appreciated by referring to Fig. 9. Here the emitter contact of Fig. 5 is illustrated except that undercutting is severe. The underlying layer 30 is etched away far underneath the gold layer ~~13~~ 31. This illustration is not unrealistic, as will be appreciated when the minute dimensions involved are taken into account. Undercutting of this nature would occur if a material were used for the layer 30 which could not be etched in a controlled manner, or if molybdenum were used but etching continued too long or the etchant did not tend to remove molybdenum oxide. The photoresist masking material 32' is shown overlying the gold layer 31 and the underlying layer 30, with the form of the original gold and underlying layers being shown in dotted lines. After the gold etching step and then the etching step for the layer 30 are performed, it is seen that the layer 30 is etched away to leave a mechanically weak contact structure which, in addition to electrical degradation, is undesirable since the contact resembles a pedestal and may easily be broken away from the silicon. After the photoresist has been removed, the thin cantilevered edges 33 of the gold film would easily droop down and contact the silicon. Then when the device is heated to above the gold-silicon eutectic temperature in a later stage of manufacture the device would be destroyed by the rapid spreading of the gold-silicon alloy. It should be noted at this point that the undercutting problem, while present to some extent, does

not have such dire consequences when only a single material is used in making the contact. If only aluminium is used as the contact material, only one etching step is used so that the "cantilevering" of contact material is not evident, but even if it were there would be no detriment to the device if this material came into contact with the silicon surface.

To provide good, low resistance, ohmic contacts to silicon with molybdenum, it is necessary that the surface regions of the silicon where contact is made be of high impurity concentration, whether N-type or P-type. When boron or phosphorous is used as the impurity the surface concentration for good contact should be greater than 2×10^{19} atoms per cc, and preferably above 10^{21}. Electrical contact can be made to silicon surfaces that contain lesser concentrations, but the contact resistance increases as the dopant concentration decreases. A sharp break in the plot of contact resistance vs. impurity concentration occurs at about 2×10^{19}. In typical transistors such as that described above, the N-type emitter is ordinarily of very high concentration, especially at the surface, since this is the second diffusion. Even though generally of lower concentration than the emitter, the base region is also ordinarily doped heavily enough, at the surface at least, to provide low resistance contact. If not, a shallow P-type diffusion step is introduced prior to evaporation of contact materials. This diffusion would be through holes of about the same size and in the same place as the holes 14 and 15 cut for the base contacts, and preferably the exact same openings are used. In integrated circuits the extra diffusions to produce high surface concentrations in the contact areas are more likely to be necessary. This is because the collector contact is made on top of the wafer to a region which may be an epitaxial layer of low concentration or else may be the first diffusion in a triple diffused device, this first diffusion generally being of fairly low concentration so that the two subsequent diffusions may be made. Also, the base region of the transistor of an integrated circuit is ordinarily made simultaneously with the formation of a diffused resistor. Since the resistivity of the material which forms this diffused resistor region should be fairly high, this requires the base concentration to be fairly low. Accordingly, in a typical integrated circuit with NPN transistors and P-type diffused resistors, the impurity concentration for contacts to the collectors, bases and resistors must be supplemented.

Referring to Fig. 10, an integrated circuit is shown in section which comprises a P-type silicon wafer 40 having a transistor formed on the left-hand end by a diffused N-type collector region 41, a P-type base region 42, and an N-type emitter region 43. On the right-hand side a resistor is provided by first an isolation region 44, then the resistor itself which is a P-type diffused region 45. Before the second N-type diffusion, which forms the emitter region 43, a hole is cut where the collector contact is to be made and a high concentration N+ region 46 is created simultaneously with the emitter region 43. Then high concentration P+ regions 47, 48 and 49 are produced by a subsequent selective boron diffusion using oxide masking. Thereafter holes are cut in the oxide coating where the transistor contacts and the resistor contacts are to be made, the surface is cleaned, and the evaporation procedure as set forth above is used to apply a molybdenum coating and a gold coating to the top surface of the device, then the metal coatings are selectively removed to produce the desired pattern of contacts and interconnections. It is seen that the collector is connected to one end of the resistor by an interconnection 50 which extends over the oxide. A typical integrated circuit would include in the same semiconductor wafer many transistors and resistors of the type seen in Fig. 10, rather than one of each. Of course, the heavily-doped regions under the contacts could be used in the transistor of Fig. 6.

The necessity for the extra P+ diffusion to provide low contact resistance may be obviated in some cases if a flash of very thin layer of aluminium is applied prior to depositing the layer of molybdenum on the surface of the device. Since aluminium is a P-type dopant itself, no additional doping is necessary to provide the high surface concentration in the P-type regions. Ordinarily the emitter regions would be very heavily doped N-type, so the addition of a small amount of aluminium would not convert the surface of these regions or degrade the contact resistance. This arrangement takes advantage of the excellent adherence of aluminium to silicon. The interposed layer of molybdenum prevents the combining of aluminium and gold and thus avoids the undesirable intermetallic compound. The rigorous surface preparation is not as critical when aluminium is applied before applying molybdenum. The presence of aluminium in this three-layered contact arrangement, however, introduces some of the problems of degradation due to aluminium passing through pinholes, etc.

It should be noted that the contact arrangement of this invention, comprising evaporated molybdenum and evaporated gold, is essentially an "alloyless" system. The molybdenum does not alloy with the silicon and the gold does not alloy with the molybdenum. In contrast with aluminium where the deposited metal is ordinarily heated to a temperature above the aluminium-silicon eutectic, 577°C, the contact materials of this invention are deposited at reasonably low temperatures and

need no heating to produce alloying. Since heating steps are avoided, degradation of the semiconductor devices is minimized.

When aluminium is used as the malleable metal layer on top of the molybdenum layer, some of the above materials and values will need to be varied. For example, the etchant used to remove unwanted portions of molybdenum and aluminium may be composed of 70 mls. of phosphoric acid, 15 mls. of acetic acid, 3 mls. of nitric acid and 5 mls. of deionized water. The time and temperature of etching will vary with thickness of the layers, but typical ranges are 20—60 seconds at etch temperatures of 50—70°C.

Generally an advantage of the present invention is that materials are used which do not tend to degrade the semiconductor device by their presence, which lend themselves to manufacturing techniques compatible with other processes used on the device, and which permit working with very small geometries. In the specific case of silicon planar devices, an advantage of the present invention is that a contact and interconnection arrangement is provided which adheres well to silicon and to silicon oxide surfaces without reacting unfavourably with either, which can be used with available photoresist masking and etching procedures, which forms an ohmic and low resistance electrical connection to silicon, which can be applied readily by metal evaporation techniques, which has a high conductivity, and which can be bonded with gold wires.

WHAT WE CLAIM IS:—

1. A semi-conductor device comprising a body of semiconductor material having an insulating coating over part of one surface thereof, a layer of molybdenum deposited on a part of said one surface which does not have said insulating coating and extending over at least a portion of said insulating coating, and a layer of a conductive material deposited on said layer of molybdenum.

2. A semiconductor device according to claim 1, wherein the body of semiconductor material is in the form of a wafer having a region adjacent said surface with a P-N junction between said region and other semiconductor material of the wafer extending to said surface beneath said insulating coating, the coating defining a small opening over said region, said layer of molybdenum and said layer of conductive material adhering to each other without forming an alloy with each other to engage the surface of said region in said opening and extend from said opening out over said insulating coating and over the edge of said junction to a position spaced from said region.

3. A semiconductor device according to claim 1 or 2, wherein the conductive material is gold.

4. A semiconductor device according to claim 1, including a layer of aluminium between said layer of molybdenum and said surface.

5. A semiconductor device according to claim 1 or 4, wherein said conductive material is aluminium.

6. A semiconductor device according to any preceding claim, wherein the insulating coating is an oxide.

7. A semiconductor device according to claim 6, wherein the wafer is silicon, the insulating coating is silicon oxide and the layer of molybdenum and the layer of conductive material are in the form of thin films, the layer of conductive material overlying all portions of said molybdenum film.

8. A semiconductor device according to claim 7, wherein the conductive layer is gold.

9. A semiconductor device according to claim 7 or 8, wherein said region is shallow relative to the thickness of the wafer and is very heavily doped near said surface under said opening, said device including conductive means electrically connected to said layer of conductive material at said position spaced from said region.

10. A semiconductor device according to claim 8 and 9, wherein the gold film is spaced from the surface of the silicon wafer and from the silicon oxide coating by means of the film of molybdenum, the film of molybdenum being substantially unalloyed with the silicon surface, and wherein said conductive means comprises a gold wire compression bonded to the gold film.

11. A semiconductor device comprising a body of semiconductor material having an insulating coating over one surface thereof, said body comprising a plurality of monocrystalline regions adjacent said one surface and spaced apart along said surface, each region including at least one P-N junction extending to the surface beneath said insulating coating, the coating defining openings over each said regions and extending across said face between the regions, and multilayered contacts to said regions and interconnections between said regions, said multilayered contacts comprising a layer of molybdenum on said surface within said openings and extending over the coating across the junctions to others of the openings and a layer of conductive material overlying said layer of molybdenum.

12. A semiconductor device according to claim 11, wherein the conductive material is gold.

13. A semiconductor device according to claim 11, wherein the conductive material is aluminium.

14. A semiconductor device substantially as hereinbefore described with reference to Figs.

need no heating to produce alloying. Since heating steps are avoided, degradation of the semiconductor devices is minimized.

When aluminium is used as the malleable metal layer on top of the molybdenum layer, some of the above materials and values will need to be varied. For example, the etchant used to remove unwanted portions of molybdenum and aluminium may be composed of 70 mls. of phosphoric acid, 15 mls. of acetic acid, 3 mls. of nitric acid and 5 mls. of deionized water. The time and temperature of etching will vary with thickness of the layers, but typical ranges are 20—60 seconds at etch temperatures of 50—70°C.

Generally an advantage of the present invention is that materials are used which do not tend to degrade the semiconductor device by their presence, which lend themselves to manufacturing techniques compatible with other processes used on the device, and which permit working with very small geometries. In the specific case of silicon planar devices, an advantage of the present invention is that a contact and interconnection arrangement is provided which adheres well to silicon and to silicon oxide surfaces without reacting unfavourably with either, which can be used with available photoresist masking and etching procedures, which forms an ohmic and low resistance electrical connection to silicon, which can be applied readily by metal evaporation techniques, which has a high conductivity, and which can be bonded with gold wires.

WHAT WE CLAIM IS:—

1. A semi-conductor device comprising a body of semiconductor material having an insulating coating over part of one surface thereof, a layer of molybdenum deposited on a part of said one surface which does not have said insulating coating and extending over at least a portion of said insulating coating, and a layer of a conductive material deposited on said layer of molybdenum.

2. A semiconductor device according to claim 1, wherein the body of semiconductor material is in the form of a wafer having a region adjacent said surface with a P-N junction between said region and other semiconductor material of the wafer extending to said surface beneath said insulating coating, the coating defining a small opening over said region, said layer of molybdenum and said layer of conductive material adhering to each other without forming an alloy with each other to engage the surface of said region in said opening and extend from said opening out over said insulating coating and over the edge of said junction to a position spaced from said region.

3. A semiconductor device according to claim 1 or 2, wherein the conductive material is gold.

4. A semiconductor device according to claim 1, including a layer of aluminium between said layer of molybdenum and said surface.

5. A semiconductor device according to claim 1 or 4, wherein said conductive material is aluminium.

6. A semiconductor device according to any preceding claim, wherein the insulating coating is an oxide.

7. A semiconductor device according to claim 6, wherein the wafer is silicon, the insulating coating is silicon oxide and the layer of molybdenum and the layer of conductive material are in the form of thin films, the layer of conductive material overlying all portions of said molybdenum film.

8. A semiconductor device according to claim 7, wherein the conductive layer is gold.

9. A semiconductor device according to claim 7 or 8, wherein said region is shallow relative to the thickness of the wafer and is very heavily doped near said surface under said opening, said device including conductive means electrically connected to said layer of conductive material at said position spaced from said region.

10. A semiconductor device according to claim 8 and 9, wherein the gold film is spaced from the surface of the silicon wafer and from the silicon oxide coating by means of the film of molybdenum, the film of molybdenum being substantially unalloyed with the silicon surface, and wherein said conductive means comprises a gold wire compression bonded to the gold film.

11. A semiconductor device comprising a body of semiconductor material having an insulating coating over one surface thereof, said body comprising a plurality of monocrystalline regions adjacent said one surface and spaced apart along said surface, each region including at least one P-N junction extending to the surface beneath said insulating coating, the coating defining openings over each said regions and extending across said face between the regions, and multilayered contacts to said regions and interconnections between said regions, said multilayered contacts comprising a layer of molybdenum on said surface within said openings and extending over the coating across the junctions to others of the openings and a layer of conductive material overlying said layer of molybdenum.

12. A semiconductor device according to claim 11, wherein the conductive material is gold.

13. A semiconductor device according to claim 11, wherein the conductive material is aluminium.

14. A semiconductor device substantially as hereinbefore described with reference to Figs.

1, 2 and 4 to 8 of the accompanying drawings.

15. A semiconductor device substantially as hereinbefore described with reference to Fig. 10 of the accompanying drawings.

16. A method of making a semiconductor device, comprising providing a semiconductor wafer having a region adjacent one surface thereof with a P-N junction between said region and other semiconductor material of the wafer extending to said surface beneath an insulating coating which is provided on said surface with a small opening over said region, and including the steps of depositing a layer of molybdenum upon said surface of the wafer over said insulating coating and onto said opening over said region, depositing a layer of conductive material upon said surface over the layer of molybdenum and selectively removing the layers of molybdenum and conductive material from areas surrounding said opening.

17. A method of making a semiconductor device, comprising providing a silicon wafer having a region adjacent one surface thereof with a P-N junction between said region and other semiconductor material of the wafer extending to said surface beneath a silicon oxide coating which is provided on said surface with an opening over said region, and including the steps of depositing a thin layer of molybdenum upon said surface of the wafer over said silicon oxide coating and onto the silicon surface in said opening, depositing a thin layer of gold upon said surface over the thin layer of molybdenum, selectively applying an etch resistant coating to said surface over the layers of molybdenum and gold to cover the area above said opening and an expanded area extending from the area above said opening, and etching the layers of gold and molybdenum from said surface of the wafer in the regions not covered by said etching resistant coating.

18. A method of making a semiconductor device comprising the steps of providing a semiconductor wafer, forming a plurality of circuit components in the wafer adjacent one surface thereof with regions of such components having contact areas exposed through openings in an insulating coating on said surface, depositing a thin layer of molybdenum upon said surface, depositing a thin layer of conductive material over the layer of molybdenum, selectively removing portions of said layers from the surface of the wafer to provide contacts to said contact areas and interconnections overlying said insulating coating between certain ones of said contact areas.

19. A method of making a semiconductor device substantially as hereinbefore described with reference to Figs. 1 to 8 and Fig. 10 of the accompanying drawings.

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