

SOLID STATE OPTOELECTRONIC DEVICE WITH PLATED SUPPORT SUBSTRATE

TECHNICAL FIELD

[0001] The present technology is directed to solid state lighting ("SSL") devices constructed on large diameter wafers (e.g., greater than 4 inches) and with a plated metal support substrate.

BACKGROUND

[0002] SSL devices generally use semiconductor light emitting diodes ("LEDs"), organic light emitting diodes ("OLEDs"), and/or polymer light emitting diodes ("PLED") as sources of illumination rather than electrical filaments, a plasma, or a gas. Mobile phones, laptop computers, digital cameras, MP3 players, and other portable electronic devices can utilize SSL devices for background illumination. SSL devices can also be used for signage, indoor lighting, outdoor lighting, and other types of general illumination.

[0003] Figure 1 shows a conventional vertical SSL device 10 including a light emitting structure 17 having a p-type gallium nitride (GaN) 12, GaN/indium gallium nitride (InGaN) multiple quantum wells ("MQWs") 14, and n-type GaN 16 in series. The SSL device 10 also includes a support substrate 18 and a p-type contact 20 between the support substrate 18 and the p-type GaN material 12. Conventional support substrates 18 are typically sapphire or a semiconductor material having a wafer form factor. The SSL device 10 also includes an n-type contact 22 on top of the SSL device 10 that can be wirebonded to an external contact 24 of an external host device 26. As voltage is applied between the n-type contact 22 and the p-type contact 20, electrical current passes through the light emitting structure 17 and produces light. The SSL device 10 can be made on a wafer that is singulated into individual SSL devices.

[0004] Conventional devices use thermo-compression bonding, such as copper-copper (Cu-Cu) bonding, to attach the light emitting structure 17 to the support substrate 18. This process requires high temperatures and pressures that can bow or deform the wafer to the extent that it cracks or warps. Currently LED industry is mostly working with 2–4 inch diameter substrates, which limits the throughput and increases costs because fewer SSL devices can be produced on such small wafers. Even at these diameters warp and bow of the wafers is a

problem for fabrication of LEDs. This problem becomes severe for large diameter (>4 inch) wafers.

BRIEF DESCRIPTION OF THE DRAWINGS

[0005] Figure 1 is an illustration of a vertical SSL device according to the prior art.

[0006] Figure 2 is a side view of a wafer comprising a plurality of SSL devices according to an embodiment of the present technology.

[0007] Figure 3A is a side view of a growth substrate and a light emitting structure according to an embodiment of the present technology.

[0008] Figure 3B is a side view of a growth substrate, light emitting structure, barrier material, and reflective material according to an embodiment of the present technology.

[0009] Figure 4 is a side view of a wafer including a plated substrate according to an embodiment of the present technology.

[0010] Figure 5 is a side view of a wafer after the growth substrate has been removed from the light emitting structure according to an embodiment of the present technology.

[0011] Figure 6 is a side view of a wafer having n-type contacts and singulation lines according to an embodiment of the present technology.

[0012] Figure 7 is a side view of a wafer comprising a plurality of SSL devices having trenches that define mesas according to an embodiment of the present technology.

[0013] Figure 8 is a side view of a growth substrate and light emitting structure according to an embodiment of the present technology.

[0014] Figure 9 is a side view of a wafer comprising a growth substrate and light emitting structure including trenches according to an embodiment of the present technology.

[0015] Figure 10 is an enlarged view of a trench structure according to an embodiment of the present technology.

[0016] Figure 11 is a side view of a wafer having a plated substrate according to an embodiment of the present technology.

[0017] Figure 12 is a side view of a wafer after the growth substrate has been removed according to an embodiment of the present technology.

[0018] Figure 13 is a side view of a wafer having exterior contacts and singulation lines between individual SSL devices according to an embodiment of the present technology.

[0019] Figure 14 is a side view of a wafer having a patterned resist according to an embodiment of the present technology.

[0020] Figure 15 is a side view of the wafer of Figure 14 having discrete material portions formed on the wafer according to an embodiment of the present technology.

[0021] Figure 16 is a side view of the wafer of Figure 14 wherein the patterned resist has been removed according to embodiments of the present technology.

[0022] Figure 17 is a top view of the wafer of Figure 14 according to embodiments of the present technology.

DETAILED DESCRIPTION

[0023] Various embodiments of SSL devices, assemblies, and methods of manufacturing are described below. As used hereinafter, the term "SSL device" generally refers to devices with LEDs, laser diodes, OLEDs, PLEDs, and/or other suitable light emitting structures other than electrical filaments, a plasma, or a gas. A person skilled in the relevant art will also understand that the technology may have additional embodiments, and that the technology may be practiced without several of the details of the embodiments described below with reference to Figures 2–13.

[0024] Figure 2 illustrates a wafer 100 comprising several light emitting dies 110 formed at the wafer-level according to selected embodiments of the present technology. The wafer 100 can be singulated along dividing lines 102 to create the individual dies 110. In one embodiment, the wafer 100 includes a plated substrate 120, an optional barrier material 130, an optional reflective material 131, an embedded contact 140, a light emitting structure 150, and an exterior contact 160 on the light emitting structure 150. In other embodiments, the embedded contact 140 can be highly reflective and/or provide a barrier to prevent diffusion to/from the lighting structure 150 such that the barrier material 130 and/or reflective material 131 can be omitted. The plated substrate 120 is at the side of the embedded contact 140 and the plated substrate has a thickness sufficient to inhibit bowing of the light emitting structure 150. For example, when the light emitting structure 150 has a diameter of at least 100mm (e.g., 100mm, 150mm, 200mm, 300mm, or more), the plated substrate 120 alone without another carrier or support substrate can

inhibit bowing at the center of the wafer 100 to less than about $10\mu\text{m}$ – 100mm , or less than about one of $500\mu\text{m}$, $100\mu\text{m}$, $50\mu\text{m}$, $20\mu\text{m}$, $10\mu\text{m}$ or $5\mu\text{m}$ (e.g. 0.001% to 1%).

[0025] The plated substrate 120 can be electrically and thermally conductive. For example, the plated substrate 120 can be an elemental metal, an alloy of different metals, or a plurality of non-alloyed metals. In one embodiment, the plated substrate 120 includes copper, a copper alloy, nickel, aluminum, and/or other metals. The properties of different metal or alloy materials, e.g. thickness and composition, could be chosen such that resulting stress from the deposited materials is substantially eliminated and does not result in the wafer warp or bow.

[0026] The light emitting structure 150 can be an LED, an OLED, a PLED or other solid state lighting structure including a first semiconductor material 152, a second semiconductor material 154, and an active region 156 between the first semiconductor material 152 and the second semiconductor material 154. For example, the first semiconductor material 152 can be a p-GaN material, the second semiconductor material 154 can be an n-GaN material, and the active region 156 can be a quantum well structure having one or more quantum wells. In several embodiments, the wafer 100 is circular with a diameter of at least four inches, and in many applications the wafer 100 can have a diameter of six inches or more (e.g. between approximately 150–300 mm). Figures 3A–14 illustrate several processes, techniques, and methods for producing the dies 110.

[0027] Figure 3A illustrates the wafer 100 at a stage of a process according to an embodiment of the present technology after the lighting structure 150 has been formed on a growth substrate 170 apart from the plated substrate 120 shown in Figure 2. In several embodiments, at least part of the light emitting structure 150 is grown epitaxially on the growth substrate 170. In one embodiment, the growth substrate 170 includes silicon (Si) with a Si(1,1,1) crystal orientation at a surface of the growth substrate 170. In other embodiments, the growth substrate 170 can also include aluminum gallium nitride (AlGaN), GaN, silicon carbide (SiC), sapphire (Al_2O_3), an engineered substrate, a combination of the foregoing materials, and/or other suitable substrate materials.

[0028] In selected embodiments, the first and second semiconductor materials 152 and 154 include a p-type GaN material and an n-type GaN material, respectively. In another embodiment, the first and second semiconductor materials 152 and 154 include an n-type GaN material and a p-type GaN material, respectively. In further embodiments, the first and second

semiconductor materials 152 and 154 can individually include at least one of gallium arsenide (GaAs), aluminum gallium arsenide (AlGaAs), gallium arsenide phosphide (GaAsP), gallium(III) phosphide (GaP), zinc selenide (ZnSe), boron nitride (BN), AlGaN, and/or other suitable semiconductor materials.

[0029] The active region 156 can include a single quantum well ("SQW"), multiple quantum wells ("MQWs"), and/or a bulk semiconductor material. As used hereinafter, a "bulk semiconductor material" generally refers to a single grain semiconductor material (e.g., InGaN) with a thickness greater than about 10 nanometers and up to about 500 nanometers. In certain embodiments, the active region 156 can include an InGaN SQW, InGaN/GaN MQWs, and/or an InGaN bulk material. In other embodiments, the active region 156 can include aluminum gallium indium phosphide (AlGaInP), aluminum gallium indium nitride (AlGaInN), and/or other suitable materials or configurations. In any of the foregoing embodiments, the first semiconductor material 152, the active region 156, the second semiconductor material 154, and any buffer materials (not shown) can be formed on the growth substrate 170 via metal organic chemical vapor deposition ("MOCVD"), molecular beam epitaxy ("MBE"), liquid phase epitaxy ("LPE"), hydride vapor phase epitaxy ("HVPE"), and/or other suitable epitaxial growth techniques.

[0030] The orientation of the light emitting structure 150 in Figures 3A and 3B is inverse to what is shown in Figure 2 because the second semiconductor material 154, active region 156 and first semiconductor material 152 are grown sequentially over the growth substrate 170, and then the embedded contact 140 is formed over the first semiconductor material 152. A metal seed material 200 is formed on the embedded contact material 140. The seed material 200 can be copper or another suitable plating material that is deposited onto the embedded contact material using sputtering, vapor deposition, or other techniques so that it is be relatively thin. The plated metal substrate 120 (Figure 2) can then be formed at the other side of the light emitting structure 150 proximate the first semiconductor material 152.

[0031] Figure 3B illustrates an alternative embodiment according to the present technology. In addition to the materials described above with reference to Figure 3A, Figure 3B includes the barrier material 130 and the reflective material 131. In several embodiments, particularly those in which the seed material 200 comprises copper, the barrier material 130 prevents copper from diffusing into other materials of the stack. The barrier material 130 can be tungsten-titanium (WTi), tantalum nitride, or other suitable materials. The reflective material

131 can be nickel-silver (Ni-Ag), silver (Ag), or other suitable materials. The choice of whether to include the barrier material 130 and/or the reflective material 131 depends on the application for which the dies 110 are designed. For purposes of brevity, the remaining figures do not show the barrier material 130 or the reflective material 131.

[0032] Figure 4 illustrates a subsequent stage of an embodiment of the present technology, after a relatively large quantity of supporting bulk metal has been formed monolithically with the seed material. In several embodiments, the bulk metal can be plated on the seed material to form a plated substrate 210 using electroplating or electroless plating. The plated substrate 210 can be sufficient to support the light emitting structure 150 in a manner that inhibits or prevents warping, bowing and cracking. For example, the thickness of the plated substrate 210 can be 50–300 μ m, such as 150–300 μ m, 100–150 μ m or 75–150 μ m, and the plated substrate 210 can have a diameter of at least 4 inches (e.g., 6 inches or more). The precise thickness of the plated substrate 210 can depend in part upon the material and dimensions of the light emitting structure 150 and/or the metal of the plated substrate 210. The material of the plated substrate 210 can also efficiently conduct heat away from the light emitting structure 150 and can be an electrical contact for the light emitting structure 150. The plated substrate 210 provides a relatively large contact area that is easy to align with the corresponding electrical contact on a host structure.

[0033] Several embodiments of light emitting dies 110 with the plated substrate 210 described above provide several advantages over conventional designs. For example, the plated substrate 210 can prevent bowing of the light emitting structure 150 that can be caused by lateral interior strain between disparate materials of the light emitting structure 150. Such bowing in conventional devices can have many adverse affects, such as lack of uniformity among wafers, difficulty in mounting the singulated dies, delamination between layers, and breakage. Conventional permanent bond processes such as thermo-compression bonding (e.g., Cu-Cu) or temporary liquid phase ("TLP") bonding with inter-metallic compound formation, nickel-tin (NiSn) bonds, tin-copper (SnCu) bonds and tin-silver (SnAg) bonds, are time-consuming and therefore relatively expensive processes. In addition, the thermo-compression bonding process does not work as well on irregular surfaces, whereas plated materials can be readily formed on such surfaces.

[0034] Figures 3A, 3B, and 4 illustrate the wafer 100 in a first orientation in which the growth substrate 170 is shown at the bottom and the plated substrate 210 is shown at the top (as represented by arrow A). Figure 5 illustrates a subsequent stage of an embodiment of a method

of the present technology in which the wafer 100 has been inverted (e.g., arrow A points downward in Figure 5). The wafer 100 can be mounted to a temporary carrier 240 with a temporary bond. The temporary carrier 240 can be an inexpensive recyclable material, such as silicon or tape. The growth substrate 170 is then removed from the light emitting structure 150 by grinding, etching, or another suitable technique (shown in dashed lines).

[0035] Figure 6 shows the wafer 100 after the light emitting structure 150 has been exposed by removing the temporary carrier 240 and after forming several exterior contacts 250 on the wafer 100. The exterior contacts 250 can be formed using conventional metal deposition and patterning techniques. The wafer 100 can also be exposed to a surface-roughening operation. In selected embodiments, each die 110 has one exterior contact 250; in other embodiments, each die 110 has a plurality of exterior contacts 250. The wafer 100 can be annealed at this point, and different configurations can be annealed at different temperatures, such as at a low temperature (less than about 200°C) or a high temperature (more than about 200°C). The temporary carrier 240 can survive the relatively low temperatures, but may not survive temperatures above about 200°C. Accordingly, in the low-temperature embodiments the temporary carrier 240 remains on the die 110 through the annealing processes. In high-temperature processes, however, the temporary carrier 240 is removed and the wafer is mounted to a different structure before submitting the wafer to such high temperatures. The dies 110 can be singulated along lines 102 and packaged after forming the exterior contacts 250.

[0036] The arrangement of the light emitting structure 150 and the exterior contacts 250 in Figure 6 is a vertical LED configuration. In several embodiments, the plated substrate 210 is electrically conductive, can be used as an extension of the embedded contact 140, and it can provide a heat sink at the base of the die 110. As such, the die 110 can be mounted to an electrically conductive surface having an electrical bias, and the exterior contact 250 can be wirebonded to a lead at the opposite bias to complete the circuit. The plated substrate 210 also effectively conducts heat away from the die 110.

[0037] Figure 7 shows another embodiment of the wafer 300 including several dies 310 according to the present technology. Many components of this embodiment are similar to aspects of the embodiments described above. The individual dies 310 of the wafer 300 include a plated substrate 320, an embedded contact 340, a light emitting structure 350, and exterior contacts 360. The light emitting structure 350, which can be generally similar to the light emitting structure 10 described above with reference to Figure 1, can include a first

semiconductor material, a second semiconductor material, and an active region. In selected embodiments, the light emitting structure 350 includes trenches 352 separating the light emitting structure 350 into mesas 355. The trenches 352 can be aligned with singulation lines between individual dies 310 and lined with a dielectric liner 354. The plated substrate 320 can be formed to have projections 322 in the trenches 352, and the dielectric liner 354 can insulate the projections 322 from the light emitting structure 350. In several embodiments, the projections 322 are integral with the plated substrate 320.

[0038] Figure 8 illustrates the wafer 300 after the light emitting structure 350 and the embedded contact 340 have been formed on a growth substrate 370. Optionally, a barrier and/or reflective material (not shown) can be formed on the growth substrate 370. Aspects of this process are similar to the process described above with reference to Figures 3A–6.

[0039] Figure 9 shows an embodiment of a subsequent stage in which the embedded contact 340 and the light emitting structure 350 are etched to form the trenches 352 and the mesas 355. The areas above the mesas 355 can be covered with a mask, and the wafer 300 can be etched, for example via a wet etch, through the exposed portions of the embedded contact material and the light emitting structure 350 to form V-shaped trenches 352. In selected embodiments, the trench 352 can be etched, then dielectric liners 354 can be deposited and patterned. Then the embedded contacts 340 can be deposited and patterned. In several embodiments, the trenches 352 extend completely through the light emitting structure 350 and into the growth substrate 370. In other embodiments, the V-shaped trenches 352 do not reach completely through the light emitting structure 350, leaving a small connecting portion of the light emitting structure 350 at the base of the trench 352. In embodiments in which the individual dies 310 (see Fig. 7) are to be singulated, the singulation procedure can cut through this small connecting portion. The dimensions of the mesas 355 correspond to the final size of the light emitting dies that will be ultimately produced from the wafer 300. The tolerance between the dimensions of the mesas 355 and the final intended size of the light emitting dies can be somewhat large because the wafer 300 is singulated along the trenches. The etching processes described herein can also be performed using dry etch processes.

[0040] Figure 10 is an enlarged view of a single trench 352 according to an embodiment of the present technology. During a wet etch process, the crystal structure of the light emitting structure 350 is preferentially etched at an angle to form angled walls 350a. When the trenches 352 are to be filled with a conductive material, such as a plated metal, the dielectric liners 354

are formed before the trenches 352 are filled. The dielectric liners 354 can be formed by depositing a thin conformal material of dielectric material over all of the exposed surfaces. In selected embodiments, the dielectric material on top of the mesas 355 (shown in dashed lines) can be removed using a mechanical, chemical-mechanical or etching process. In other embodiments, the dielectric material can be deposited after the trenches 352 are etched but before the mask is removed from the wafer 300 such that a portion of the thin dielectric liner 354 remains in the trenches 352 after removing the mask.

[0041] Figure 11 illustrates yet another stage of the process for manufacturing the wafer 300 according to an embodiment of the present technology. After forming the trenches 352 and the dielectric liners 354, the material for the embedded contacts 340 can be deposited and the plated substrate 320 can be plated over the light emitting structure 350 and in the trenches 352. In selected embodiments, the contacts 340 can be formed on top of the mesas 355 and not in the trenches 352, as shown in Figure 11. Alternatively, the contacts 340 can be formed on the mesas 355 and in the trenches 352, as shown in Figure 7. As described above, in several embodiments a seed material (not shown) can first be deposited over the wafer 300 to facilitate the plating process. The plated substrate 320 can be metal, be thick enough to support the wafer 300, and prevent or at least inhibit bowing. For example, the thickness of the plated substrate 320 can be 50–300 μm , such as 150–300 μm , 100–150 μm or 75–150 μm . This process eliminates the need for thermo-compression or inter-metallic compound bonding, and it allows the wafer 300 to have a larger diameter. In several embodiments, the wafer 300 can be at least four inches in diameter, and in many cases 6–8 inches in diameter without undo bowing.

[0042] The wafer 300 is oriented with the plated substrate 320 facing the top of Figure 11, as shown by arrow A. Figure 12 illustrates another stage of the method after a temporary carrier 380 has been attached to the plated substrate 320, the growth substrate 370 has been removed, and the wafer has been inverted (e.g., see Arrow A). Figure 13 shows yet another portion of the method according to embodiments of the present technology after exterior contacts 390 have been formed on individual dies 310. As discussed above, the dies 310 can be annealed at a high or low temperature. If the annealing process is performed at a high temperature that would harm the bond line between the temporary carrier 380 and the substrate 320, the temporary carrier 380 can be removed prior to forming the exterior contacts 390. Otherwise, the temporary carrier 380 can remain in place as the exterior contacts 390 are formed.

[0043] Figures 14–17 illustrate yet another embodiment of the present technology in which a patterned plating is formed on a substrate at an intermediate stage of production of light emitting dies. Figure 3A and the associated description above relate to an intermediate step in which a seed layer 200 has been formed on an embedded contact 140. In place of (or in addition to) forming the plated substrate 210 on the seed layer, the following structures and processes can be used. Figure 14 shows a wafer 400 comprising a growth substrate 470, a light emitting structure 450, an optional barrier material 430, and a metal seed layer 420, similar to embodiments described above with reference to Figures 1–6. The wafer 400 also includes a patterned resist 440 formed at intervals approximately equal to the size and configuration of the individual dies that will eventually be formed by these processes and singulated into individual SSL devices. In selected embodiments, the patterned resist 440 can align with the planned singulation paths between the dies. In other embodiments, however, the patterned resist 440 can be aligned independently from the singulation paths.

[0044] Figure 15 illustrates a further stage in the process according to embodiments of the present technology in which discrete plated material portions 442 are plated using any suitable plating or metal deposition technique. In selected embodiments, the individual discrete material portions 442 are prevented from coalescing with adjacent material portions 442 by the width of the patterned resist 440. In selected embodiments the width of the patterned resist 440 on the wafer 400 is at least approximately twice the thickness of the discrete plated material portions 442. Figure 16 illustrates a further portion of the process in which the patterned resist 440 is removed, leaving the discrete material portions 442 on the wafer 400 and bonded with the seed material. The resulting structure is a series of discrete plated material portions 442 with streets 444 running between them where the patterned resist 440 once was.

[0045] Figure 17 is a top view of the discrete material portions 442 and the streets 444 running between them. The streets 444 can be orthogonal as shown, or they can have another suitable orientation. The streets 444 relieve stresses in the wafer 400, and therefore mitigates bowing and deflection of the wafer 400. Using these techniques, the wafer 400 can be a much larger size of six or eight inches or more than with conventional techniques which are generally limited to two or four inches.

[0046] The processes described herein are generally applicable to an entire wafer and all of the SSL devices on the wafer. It is to be understood, however, that in several embodiments,

one or more of the processes can be localized to a predetermined group of SSL devices, and that not all of the processes need be uniformly applied to the entire wafer.

[0047] From the foregoing, it will be appreciated that specific embodiments of the technology have been described herein for purposes of illustration, but that various modifications may be made without deviating from the technology. In addition, many of the elements of one embodiment may be combined with other embodiments in addition to or in lieu of the elements of the other embodiments. Accordingly, the technology is not limited except as by the appended claims.

CLAIMS

We claim:

1. A method of manufacturing a light emitting die, comprising:
forming a light emitting structure on a growth substrate;
forming an embedded contact electrically coupled to the first semiconductor material at a first side; and
plating a metal at the first side, wherein the plated metal forms a plated substrate having a thickness sufficient to inhibit bowing of the light emitting structure.
2. The method of claim 1 wherein:
the first semiconductor material comprises a p-type gallium nitride ("p-GaN") material, the second semiconductor material comprises a n-type gallium nitride ("n-GaN") material, and the active region comprises an indium gallium nitride ("InGaN") material;
the embedded contact comprises a p-contact electrically coupled to the p-GaN material;
and
the method further comprises attaching a carrier to the plated substrate, removing the growth substrate from the light emitting structure, and forming exterior contacts electrically coupled to the n-GaN material.
3. The method of claim 2 wherein:
the embedded contact is a reflective material;
the plated substrate comprise copper; and
the thickness of the plated substrate is approximately 50–150 microns.
4. The method of claim 1, further comprising:
depositing a barrier material on the embedded contact;
forming a seed material on the barrier material; and
plating the metal on the seed material.

5. The method of claim 1 wherein plating the metal at the first side of the light emitting structure comprises depositing a barrier material on the embedded contact, forming a seed material on the barrier material, and plating the metal on the seed material

6. The method of claim 1 wherein the thickness of the plated substrate is approximately 50–300 microns.

7. The method of claim 1 wherein the thickness of the plated substrate is approximately 75–150 microns.

8. The method of claim 1, further comprising removing a carrier and dicing through the plated substrate, a barrier material, the embedded contact, and the light emitting structure to form individual SSL devices.

9. The method of claim 1 wherein the growth substrate is at least approximately six inches in diameter.

10. The method of claim 1 wherein the light emitting structure comprises a first semiconductor material, a second semiconductor material, and an active region between the first and second semiconductor materials.

11. A method of manufacturing solid state lighting devices, comprising:
forming a light emitting structure on a generally circular growth substrate, wherein the growth substrate and the light emitting structure are at least approximately six inches in diameter;
etching a plurality of trenches in the light emitting structure that separate the light emitting structure into individual mesas;
forming a plated substrate on the individual mesas and in the trenches such that a first side of the plated substrate faces toward the mesas and a second side opposite the first side faces away from the mesas;
attaching a carrier to the second side of the plated substrate; and
removing the growth substrate from the light emitting structure.

12. The method of claim 11, further comprising:
forming an embedded contact at the first side of the light emitting structure before forming the plated substrate; and
forming a barrier on the embedded contact, wherein etching the trenches comprises forming V-shaped trenches through the light emitting structure, the embedded contact, and the barrier.
13. The method of claim 11 wherein etching the plurality of trenches comprises etching through the light emitting structure to expose a portion of the growth substrate.
14. The method of claim 11 wherein etching the plurality of trenches in the light emitting structure comprises using a wet etch that penetrates to the growth substrate.
15. The method of claim 11, further comprising forming dielectric liners in the plurality of trenches that electrically isolate the light emitting structure from the plated substrate.
16. A wafer having a plurality of individual solid state lighting devices, comprising:
a light emitting structure comprising a first semiconductor material on a first side, a second semiconductor material on a second side, and an active region between the first and second semiconductor materials;
an embedded contact at the first side;
a plated substrate formed on the embedded contact, wherein the plated substrate has a thickness sufficient to inhibit bowing of the light emitting structure; and
a plurality of exterior contacts formed on the second side of the light emitting structure, wherein the wafer is at least approximately 150 millimeters in diameter.
17. The wafer of claim 16 wherein the wafer is between approximately 150–300 millimeters in diameter.
18. The wafer of claim 16 wherein the wafer has trenches in the light emitting structure and the plated substrate comprises a plurality of projections protruding from the plated substrate into the trenches.

19. The wafer of claim 16, further comprising at least one of a barrier material and a reflective material between the plated substrate and the embedded contact.
20. The wafer of claim 16 wherein the plated substrate has a thickness of about 50–300 μm .
21. The wafer of claim 16 wherein the plated substrate has a thickness of about 100–150 μm .