3DIC Interconnect Apparatus and Method

BACKGROUND

[0001] The semiconductor industry has experienced rapid growth due to continuous improvements in the integration density of a variety of electronic components (*e.g.,* transistors, diodes, resistors, capacitors, etc.). For the most part, this improvement in integration density has come from repeated reductions in minimum feature size (*e.g.,* shrinking the semiconductor process node towards the sub-20nm node), which allows more components to be integrated into a given area. As the demand for miniaturization, higher speed and greater bandwidth, as well as lower power consumption and latency has grown recently, there has grown a need for smaller and more creative packaging techniques of semiconductor dies.

[0002] As semiconductor technologies further advance, stacked semiconductor devices, e.g., 3D integrated circuits (3DIC), have emerged as an effective alternative to further reduce the physical size of a semiconductor device. In a stacked semiconductor device, active circuits such as logic, memory, processor circuits and the like are fabricated on different semiconductor wafers. Two or more semiconductor wafers may be installed on top of one another to further reduce the form factor of the semiconductor device.

[0003] Two semiconductor wafers may be bonded together through suitable bonding techniques. The commonly used bonding techniques include direct bonding, chemically activated bonding, plasma activated bonding, anodic bonding, eutectic bonding, glass frit bonding, adhesive bonding, thermo-compressive bonding, reactive bonding and/or the like. An electrical connection may be provided between the stacked semiconductor wafers. The stacked

semiconductor devices may provide a higher density with smaller form factors and allow for increased performance and lower power consumption.

BRIEF DESCRIPTION OF THE DRAWINGS

[0004] For a more complete understanding of the present disclosure, and the advantages thereof, reference is now made to the following descriptions taken in conjunction with the accompanying drawings, in which:

[0005] Figures 1-6 are cross-sectional views of various processing steps during fabrication of an interconnect in accordance with an embodiment;

[0006] Figure 7 is a cross-sectional view of an intermediate processing step during fabrication of an interconnect in accordance with another embodiment; and

[0007] Figure 8 is a flow diagram illustrating a method of forming an interconnect in accordance with an embodiment.

[0008] Corresponding numerals and symbols in the different figures generally refer to corresponding parts unless otherwise indicated. The figures are drawn to clearly illustrate the relevant aspects of the various embodiments and are not necessarily drawn to scale.

DETAILED DESCRIPTION OF ILLUSTRATIVE EMBODIMENTS

[0009] The making and using of embodiments of the present disclosure are discussed in detail below. It should be appreciated, however, that the present disclosure provides many applicable inventive concepts that can be embodied in a wide variety of specific contexts. The specific embodiments discussed are merely illustrative of specific ways to make and use the invention, and do not limit the scope of the invention.

[0010] The present disclosure will be described with respect to embodiments in a specific context, namely, a method for forming interconnect structures for a stacked semiconductor device. Other embodiments, however, may be applied to a variety of semiconductor devices. Hereinafter, various embodiments will be explained in detail with reference to the accompanying drawings.

[0011] Figures 1-6 illustrate various intermediate steps of forming an interconnect structure between two bonded wafers or dies in accordance with an embodiment. Referring first to Figure 1, a first wafer 100 and a second wafer 200 is shown prior to a bonding process in accordance with various embodiments. In an embodiment, the second wafer 200 has similar features as the first wafer 100, and for the purpose of the following discussion, the features of the second wafer 200 having reference numerals of the form "2xx" are similar to features of the first wafer 100 having reference numerals of the form "1xx," the "xx" being the same numerals for the first wafer 100 and the second wafer 200. The various elements of the first wafer 100 and the second wafer 200 will be referred to as the "first <element> 1xx" and the "second <element> 2xx," respectively.

[0012] In an embodiment, the first wafer 100 comprises a first substrate 102 having a first electrical circuit (illustrated collectively by first electrical circuitry 104) formed thereon. The first substrate 102 may comprise, for example, bulk silicon, doped or undoped, or an active layer of a semiconductor-on-insulator (SOI) substrate. Generally, an SOI substrate comprises a layer of a semiconductor material, such as silicon, formed on an insulator layer. The insulator layer may be, for example, a buried oxide (BOX) layer or a silicon oxide layer. The insulator layer is provided on a substrate, typically a silicon or glass substrate. Other substrates, such as a multi-layered or gradient substrate may also be used.

[0013] The first electrical circuitry 104 formed on the first substrate 102 may be any type of circuitry suitable for a particular application. In an embodiment, the circuitry includes electrical devices formed on the substrate with one or more dielectric layers overlying the electrical devices. Metal layers may be formed between dielectric layers to route electrical signals between the electrical devices. Electrical devices may also be formed in one or more dielectric layers.

[0014] For example, the first electrical circuitry 104 may include various N-type metal-oxide semiconductor (NMOS) and/or P-type metal-oxide semiconductor (PMOS) devices, such as transistors, capacitors, resistors, diodes, photo-diodes, fuses, and the like, interconnected to perform one or more functions. The functions may include memory structures, processing structures, sensors, amplifiers, power distribution, input/output circuitry, or the like. One of ordinary skill in the art will appreciate that the above examples are provided for illustrative purposes only to further explain applications of the present invention and are not meant to limit the present invention in any manner. Other circuitry may be used as appropriate for a given application.

[0015] Also shown in Figure 1 is a first inter-layer dielectric (ILD)/inter-metallization dielectric (IMD) layer 106. The first ILD layer 106 may be formed, for example, of a low-K dielectric material, such as phosphosilicate glass (PSG), borophosphosilicate glass (BPSG), FSG, SiO_xC_y, Spin-On-Glass, Spin-On-Polymers, silicon carbon material, compounds thereof, composites thereof, combinations thereof, or the like, by any suitable method known in the art, such as spinning, chemical vapor deposition (CVD), and plasma-enhanced CVD (PECVD). It should also be noted that the first ILD layer 106 may comprise a plurality of dielectric layers.

[0016] First contacts 108 are formed through the first ILD layer 106 to provide an electrical contact to the first electrical circuitry 104. The first contacts 108 may be formed, for example, by using photolithography techniques to deposit and pattern a photoresist material on the first ILD layer 106 to expose portions of the first ILD layer 106 that are to become the first contacts 108. An etch process, such as an anisotropic dry etch process, may be used to create openings in the first ILD layer 106. The openings may be lined with a diffusion barrier layer and/or an adhesion layer (not shown), and filled with a conductive material. The diffusion barrier layer comprises one or more layers of TaN, Ta, TiN, Ti, CoW, or the like, and the conductive material comprises copper, tungsten, aluminum, silver, and combinations thereof, or the like, thereby forming the first contacts 108 as illustrated in Figure 1.

[0017] One or more additional ILD layers 110 and the first interconnect lines 112a-112d (collectively referred to as first interconnect lines 112) form metallization layers over the first ILD layer 106. Generally, the one or more additional ILD layers 110 and the associated metallization layers are used to interconnect the electrical circuitry to each other and to provide an external electrical connection. The additional ILD layers 110 may be formed of a low-K dielectric material, such as fluorosilicate glass (FSG) formed by PECVD techniques or high-

density plasma chemical vapor deposition (HDPCVD) or the like, and may include intermediate etch stop layers. External contacts (not shown) may be formed in an uppermost layer.

[0018] It should also be noted that one or more etch stop layers (not shown) may be positioned between adjacent ones of the ILD layers, *e.g.*, the first ILD layer 106 and the additional ILD layers 110. Generally, the etch stop layers provide a mechanism to stop an etching process when forming vias and/or contacts. The etch stop layers are formed of a dielectric material having a different etch selectivity from adjacent layers, *e.g.*, the underlying first substrate 102 and the overlying ILD layers 106/110. In an embodiment, etch stop layers may be formed of SiN, SiCN, SiCO, CN, combinations thereof, or the like, deposited by CVD or PECVD techniques.

[0019] In an embodiment, the first wafer 100 is a backside illumination sensor (BIS) and the second wafer 200 is a logic circuit, such as an ASIC device. In this embodiment, the first electrical circuitry 104 includes photo active regions, such as photo-diodes formed by implanting impurity ions into the epitaxial layer. Furthermore, the photo active regions may be a PN junction photo-diode, a PNP photo-transistor, an NPN photo-transistor or the like. The BIS sensor may be formed in an epitaxial layer over a silicon substrate.

[0020] The second wafer 200 may comprise a logic circuit, an analog-to-digital converter, a data processing circuit, a memory circuit, a bias circuit, a reference circuit, and the like.

[0021] In an embodiment, the first wafer 100 and the second wafer 200 are arranged with the device sides of the first substrate 102 and the second substrate 202 facing each other as illustrated in Figure 1. As discussed in greater detail below, an opening will be formed extending from a backside (opposite the device side) of the first wafer 100 to the selected portions of the second interconnect lines 212 of the second wafer 200, such that portions of

selected first interconnect lines 112 of the first wafer 100 will also be exposed. The opening will be subsequently filled with a conductive material, thereby forming an electrical contact on the backside of the first wafer to the interconnect lines of the first wafer 100 and the second wafer 200.

[0022] Figure 2 illustrates the first wafer 100 and the second wafer 200 after bonding in accordance with an embodiment. As shown in Figure 1, the first wafer 100 will be stacked and bonded on top of the second wafer 200. The first wafer 100 and the second wafer 200 may be bonded using, for example, a direct bonding process such as metal-to-metal bonding (*e.g.*, copper-to-copper bonding), dielectric-to-dielectric bonding (*e.g.*, oxide-to-oxide bonding), metal-to-dielectric bonding (*e.g.*, oxide-to-copper bonding), any combinations thereof and/or the like.

[0023] It should be noted that the bonding may be at wafer level, wherein the first wafer 100 and the second wafer 200 are bonded together, and are then singulated into separated dies. Alternatively, the bonding may be performed at the die-to-die level, or the die-to-wafer level.

[0024] After the first wafer 100 and the second wafer 200 are bonded, a thinning process may be applied to the backside of the first wafer 100. In an embodiment in which the first substrate 102 is a BIS sensor, the thinning process serves to allow more light to pass through from the backside of the first substrate to the photo-active regions without being absorbed by the substrate. In an embodiment in which the BIS sensor is fabricated in an epitaxial layer, the backside of the first wafer 100 may be thinned until the epitaxial layer is exposed. The thinning process may be implemented by using suitable techniques such as grinding, polishing, a SMARTCUT® procedure, an ELTRAN® procedure, and/or chemical etching.

[0025] Also shown in Figure 2 is a first opening 226. As discussed in greater detail below, an electrical connection will be formed extending from a backside of the first wafer 100 to select

ones of the second interconnect lines 212 of the second wafer 200. The first opening 226 represents the opening in which the backside contact will be formed. The first opening 226 may be formed using photolithography techniques. Generally, photolithography techniques involve depositing a photoresist material, which is subsequently irradiated (exposed) and developed to remove a portion of the photoresist material. The remaining photoresist material protects the underlying material from subsequent processing steps, such as etching.

[0026] Also shown in Figure 2 is an optional anti-reflection coating (ARC) layer 228. The ARC layer 228 reduces the reflection of the exposure light used during the photolithography process to pattern a patterned mask (not shown), which reflection may cause inaccuracies in the patterning. The ARC layer 228 may be formed of a nitride material (*e.g.*, silicon nitride), an organic material (*e.g.*, silicon carbide), an oxide material, high-k dielectric, and the like. The ARC layer 228 may be formed using suitable techniques such as CVD and/or the like.

[0027] Other layers may be used in the patterning process. For example, one or more optional hard mask layers may be used to pattern the first substrate 102. Generally, one or more hard mask layers may be useful in embodiments in which the etching process requires masking in addition to the masking provided by the photoresist material. During the subsequent etching process to pattern the first substrate 102, the patterned photoresist mask will also be etched, although the etch rate of the photoresist material may not be as high as the etch rate of the first substrate 102. If the etch process is such that the patterned photoresist mask would be consumed before the etching process is completed, then an additional hard mask may be utilized. The material of the hard mask layer or layers is selected such that the hard mask layer(s) exhibit a lower etch rate than the underlying materials, such as the materials of the first substrate 102.

[0028] Referring now to Figure 3, a multi-layered dielectric film 330 is formed over the backside of the first substrate 102 and along sidewalls of the first opening 226 in accordance with an embodiment. As will be discussed in greater detail below, the multi-layered dielectric film 330 provides greater passivation and isolation between through via structures and device circuits/pixel arrays. The multi-layered dielectric film 330 provides greater protection than a single film during, for example, a subsequent etch process to form electrical contacts to selected ones of the first interconnect structures 112 and the second interconnect structures 212. For example, an etch process such as a plasma etch may result in damage to the first substrate 102 as well as the dielectric layers (*e.g.*, the ILD layers 106, 110, and 210). Additionally, the multi-layered dielectric film 330 may provide greater protection against metal ions diffusing into the first substrate 102 and the dielectric layers.

[0029] Figure 3 illustrates an embodiment in which the multi-layered dielectric film 330 comprises a first dielectric film 330a and a second dielectric film 330b. An example of dielectric materials that may be used is a nitride material for the first dielectric film 330a and an oxide for the second dielectric film 330b. The nitride layer, such as a silicon nitride (Si_3N_4) layer, may be formed using CVD techniques using silane and ammonia as precursor gases, and deposition temperatures ranging from 550° to 900° Celsius (C). The oxide layer, such as a silicon dioxide layer, may be formed by thermal oxidation or by CVD techniques using tetra-ethyl-ortho-silicate (TEOS) and oxygen as precursor. In an embodiment, the first dielectric film 330a has a thickness from about 200 Å to about 8,000 Å, and the second dielectric film 330b has a thickness from about 200 Å to about 8,000 Å. The thicknesses of the first dielectric film 330a and the second dielectric film 330b may be adjusted to provide sufficient protection, such as protection from the etch processes and/or isolation/passivation. Other materials, including other oxides,

other nitrides, SiON, SiC, low k dielectric materials (e.g., Black Diamond), and/or high k oxides (e.g., HfO_2, Ta_2O_5).

[0030] Figure 4 illustrates a patterned mask 440 formed over the backside of the first substrate 102 in accordance with an embodiment. The patterned mask 440 may be, for example, a photoresist material that has been deposited, masked, exposed, and developed as part of a photolithography process. The patterned mask 440 is patterned to define a via opening extending through the one or more ILD layers 110 of the first substrate 102 and at least some of the one or more ILD layers 210 of the second substrate 202, thereby exposing portions of select ones of the first interconnect lines 112 and the second interconnect lines 212, as explained in greater detail below.

[0031] Figure 5 illustrates the semiconductor device shown in Figure 4 after one or more additional etching processes are performed in accordance with an embodiment. A suitable etching process, such as a dry etch, an anisotropic wet etch, or any other suitable anisotropic etch or patterning process, may be performed on the semiconductor device to form a second opening 514.

[0032] As illustrated in Figure 5, the second opening 514 extends the first opening 226 to the first interconnect lines 112a and 112b and to the second interconnect line 212a. In an embodiment, the first interconnect lines 112a and 112b are formed of suitable metal materials such as copper, which exhibits a different etching rate (selectivity) than the first ILD layers 110. As such, the first interconnect lines 112a and 112b function as a hard mask layer for the etching process of the first ILD layers 110. A selective etching process may be employed to etch the first ILD layers 110 rapidly while etching only a portion of the first interconnect lines 112a and 112b. As shown in Figure 5, the exposed portion of the first interconnect lines 112a and 112b

may be partially etched away, thereby forming a recess 516, as the etch process continues toward the second interconnect line 212a. The depth of the recess 516 may vary depending on a variety of applications and design needs.

[0033] The second etch process continues until the second interconnect line 212a is exposed, thereby forming a combined opening extending from a backside of the first wafer 100 to the second interconnect line 212a of the second wafer 200 as illustrated in Figure 5.

[0034] It should be noted that the second etch process may extend through a variety of various layers used to form the first ILD layers 110 and the second ILD layers 210, which may include various types of materials and etch stop layers. Accordingly, the second etch process may utilize multiple etchants to etch through the various layers, wherein the etchants are selected based upon the materials being etched.

[0035] Figure 6 illustrates a conductive material formed within the first opening 226 (see Figure 5) and the second opening 514 (see Figure 5) in accordance with various embodiments. In an embodiment, the conductive material may be formed by depositing one or more diffusion and/or barrier layers 622 and depositing a seed layer. For example, a diffusion barrier layer comprising one or more layers of Ta, TaN, TiN, Ti, CoW, or the like is formed along the sidewalls of the first opening 310 and the second opening 514. The seed layer (not shown) may be formed of copper, nickel, gold, any combination thereof and/or the like. The diffusion barrier layer and the seed layer may be formed by suitable deposition techniques such as PVD, CVD and/or the like. Once the seed layer has been deposited in the openings, a conductive material, such as tungsten, titanium, aluminum, copper, any combinations thereof and/or the like, is filled into the first opening 310 and the second opening 514, using, for example, an electro-chemical plating process, thereby forming a conductive plug 620.

[0036] Figure 6 also illustrates removal of excess materials, e.g., excess conductive materials, from the backside of the first substrate 102. In embodiments, one or more of the layers of the multi-layer dielectric film 330 may be left along a backside of the first substrate 102 to provide additional protection from the environment. In the example illustrated in Figure 6, the first dielectric film 330a and the second dielectric film 330b of the multi-layer dielectric film 330 remain. In this example, the excess materials may be removed using an etch process, a planarization process (e.g., a CMP process), or the like, using the second dielectric film 330b as a stop layer.

[0037] Figure 7 illustrates another example in which the second dielectric film 330b along the backside of the first substrate 102 is removed. In this example, the first dielectric film 330a may act as a stop layer for an etch or planarization process, or the like, to remove the excess second dielectric film 330b.

[0038] Figures 6 and 7 further illustrate a dielectric capping layer 660 formed along a backside of the first wafer 100. The dielectric capping layer 660 may comprise one or more layers of dielectric materials, such as silicon nitride, silicon oxynitride, silicon oxycarbide, silicon carbide, combinations thereof, and multi-layers thereof. The dielectric capping layer 660 may have a thickness from about 200 Å to about 6,000 Å, and be formed by, for example, using suitable deposition techniques such as sputtering, CVD and the like.

[0039] Figure 8 is a flowchart illustrating a method of forming stacked chip configuration in accordance with an embodiment. The method begins in step 810, wherein substrates to be bonded are provided. The substrates may be processed wafers (such as those illustrated in Figure 1), dies, a wafer and a die, or the like. In step 812, the substrates are bonded and a patterned mask is formed thereon, the patterned mask defining an opening for a contact plug to be

subsequently formed, such as that discussed above with reference to Figure 2. Optionally, an ARC layer and/or one or more hard mask layers are formed.

[0040] Thereafter, in step 814, a first etch process is performed to etch through a first substrate of the first wafer, such as discussed above with reference to Figure 3, thereby forming a first opening. In step 816, a multi-layer dielectric film is formed within the first opening and along a backside of the first substrate, and in step 818, a patterned mask, as discussed above with reference to Figure 4, is formed to define a second opening to contact select ones of the interconnects formed on the first substrate and/or the second substrate. In step 820, another etch process is used to create the second opening, which exposes portions of the interconnects on the first substrate and/or the second substrate, as discussed above with reference to Figure 5. The opening is filled with a conductive material in step 822, such as that discussed above with reference to Figures 6 and 7. A dielectric cap layer may be formed over the conductive material, such as that discussed above with reference to Figures 6 and 7.

[0041] In an embodiment, an apparatus is provided. The apparatus includes a first chip and a second chip. The first chip has a first substrate, a plurality of first dielectric layers and a plurality of first metal lines formed in the first dielectric layers over the first substrate. The second chip has a surface bonded to a first surface of the first semiconductor chip, wherein the second chip has a second substrate, a plurality of second dielectric layers and a plurality of second metal lines formed in the second dielectric layers over the second substrate. A first opening having a first width is in the first substrate, and a second opening extends from a bottom of the first opening through the plurality of first dielectric layers and into the plurality of second dielectric layers, wherein the second opening has a second width less than the first width. A conductive plug is in the first opening and the second opening. A plurality of liners is interposed between the

conductive plug and the first substrate such that the plurality of liners extending along a bottom of the first opening. At least one of the plurality of liners does not extend between the conductive plug and the plurality of first dielectric layers of the first chip.

[0042] In another embodiment, a method is provided. The method includes providing a first chip, wherein the first chip has a substrate and a plurality of dielectric layers, the plurality of dielectric layers having metallization layers formed therein. A first surface of the plurality of dielectric layers of the first chip is bonded to a surface of a second chip. A first opening extending into a backside of the substrate is formed, and a plurality of liners are formed along sidewalls and a bottom of the first opening. A second opening extending from a bottom of the first opening through the plurality of dielectric layers to a metallization layer in the second chip is formed, and a conductive material is formed in the first opening and the second opening.

[0043] In yet another embodiment, another method is provided. The method includes providing a bonded structure having a first substrate bonded to a second substrate, the first substrate having one or more overlying first dielectric layers and a first conductive interconnect in the one or more first dielectric layers, the second substrate having one or more overlying second dielectric layers and a second conductive interconnect in the one or more second dielectric layers, the first substrate being bonded to the second substrate such that the first dielectric layers face the second dielectric layers. A first opening is formed extending through the first substrate, and a plurality of dielectric layers are formed along sidewalls and a bottom of the first opening. After the forming the plurality of dielectric layers, a second opening is formed extending from the first opening to a first pad formed in at least one of the first dielectric layers and a second pad formed in at least one of the second dielectric layers. A conductive plug is formed in the first opening and the second opening.

[0044] Although embodiments of the present invention and its advantages have been described in detail, it should be understood that various changes, substitutions and alterations can be made herein without departing from the spirit and scope of the invention as defined by the appended claims.

[0045] Moreover, the scope of the present application is not intended to be limited to the particular embodiments of the process, machine, manufacture, composition of matter, means, methods and steps described in the specification. As one of ordinary skill in the art will readily appreciate from the disclosure of the present invention, processes, machines, manufacture, compositions of matter, means, methods, or steps, presently existing or later to be developed, that perform substantially the same function or achieve substantially the same result as the corresponding embodiments described herein may be utilized according to the present invention. Accordingly, the appended claims are intended to include within their scope such processes, machines, manufacture, compositions of matter, means, methods, or steps.

WHAT IS CLAIMED IS:

1. A method comprising:

providing a first chip, the first chip having a substrate and a plurality of dielectric layers disposed on a front side of the substrate, the plurality of dielectric layers having metallization layers formed therein;

bonding a first surface of the plurality of dielectric layers of the first chip to a surface of a second chip, the first surface of the plurality of dielectric layers and the front side of the substrate facing the surface of the second chip;

forming an anti-reflection coating layer over a backside of the substrate;

forming a first trench extending through the anti-reflection coating layer and into the backside of the substrate;

forming a plurality of liners along sidewalls and a bottom of the first trench, wherein forming the plurality of liners comprises:

depositing a first liner of the plurality of liners in physical contact with a semiconductor material of the substrate and the anti-reflection coating layer; and

depositing a second liner of the plurality of liners on the first liner of the plurality of liners;

forming a second trench extending from the bottom of the first trench through the plurality of dielectric layers to a metallization layer in the second chip;

forming a barrier layer along sidewalls and a bottom of the second trench;

forming a conductive material in the first trench and the second trench, a topmost surface of the second liner of the plurality of liners being level with a topmost surface of the first liner of the plurality of liners.

forming a cap layer over the conductive material and the backside of the substrate, the cap layer and the barrier layer comprising different materials, the conductive material being interposed between the cap layer and the second chip.

2. The method of claim 1, wherein a subset of the plurality of liners extend over a backside of the first chip, and wherein the cap layer extends over the subset of the plurality of liners.

3. The method of claim 1, wherein the second trench extends to and between conductive pads in the plurality of dielectric layers on the substrate and to a conductive pad formed in a dielectric layer of the second chip.

4. A method comprising:

forming a bonded structure having a first substrate bonded to a second substrate, the first substrate having one or more first dielectric layers disposed thereon and a first conductive interconnect is disposed in the one or more first dielectric layers, the second substrate having one or more second dielectric layers disposed thereon and a second conductive interconnect is disposed in the one or more second dielectric layers, the first substrate being bonded to the second substrate such that the first dielectric layers face the second dielectric layers;

forming a first opening extending through the first substrate;

forming a plurality of third dielectric layers along sidewalls and a bottom of the first opening, wherein forming the plurality of third dielectric layers comprises:

forming a first one of the plurality of third dielectric layers along the sidewalls and the bottom of the first opening, the first one of the plurality of third dielectric layers being in physical contact with a semiconductor material of the first substrate; and

forming a second one of the plurality of third dielectric layers over the first one of the plurality of third dielectric layers, the second one of the plurality of third dielectric layers being in physical contact with the first one of the plurality of third dielectric layers;

after the forming the plurality of third dielectric layers, etching a second opening extending from the first opening to a first pad formed in at least one of the first dielectric layers and a second pad formed in at least one of the second dielectric layers, the second opening having a width less than a width of the first opening, wherein etching the second opening comprises partially etching the first pad;

forming a conductive plug in the first opening and the second opening, a topmost surface of the conductive plug being level with a topmost surface of the first one of the plurality of third dielectric layers and a topmost surface of the second one of the plurality of third dielectric layers; and

after the forming the conductive plug, forming a cap layer over a backside of the first substrate, the cap layer being in physical contact with the topmost surface of the conductive plug, the topmost surface of the first one of the plurality of third dielectric layers, and the topmost surface of the second one of the plurality of third dielectric layers.

5. The method of claim 4, further comprising, prior to the forming the conductive plug, forming a liner along sidewalls of the first opening and the second opening.

6. The method of claim 4, wherein less than all of the plurality of third dielectric layers extend over the backside of the first substrate.

7. The method of claim 4, wherein the first one of the plurality of third dielectric layers comprises a nitride layer, and wherein the second one of the plurality of third dielectric layers comprises an oxide layer.

8. A method comprising:

bonding a first semiconductor chip to a second semiconductor chip, wherein the first semiconductor chip comprises a first substrate, a plurality of first dielectric layers and a plurality of first metal lines formed in the first dielectric layers over the first substrate, wherein the second semiconductor chip comprises a second substrate, a plurality of second dielectric layers and a plurality of second metal lines formed in the second dielectric layers over the second substrate;

forming a first opening in the first substrate, the first opening having a first width;

forming a second opening extending from a bottom of the first opening through the plurality of first dielectric layers and into the plurality of second dielectric layers, the second opening comprising:

a first portion having a second width less than the first width, wherein the first portion extends from the first substrate to one of the plurality of first metal lines; and

a second portion having a third width less than the second width, wherein the second portion extends from the first portion to one of the plurality of second metal lines, and wherein a single patterning mask is used to etch both the first portion and the second portion of the second opening;

forming a plurality of liners along a bottom and sidewalls of the first opening, wherein forming the plurality of liners comprises:

depositing a first liner layer along the bottom and the sidewalls of the first opening, the first liner layer being in physical contact with a semiconductor material of the first substrate;

depositing a second liner layer over the first liner layer, the second liner layer being in physical contact with the first liner layer; and

removing a portion of the second liner layer to expose a topmost surface of the first liner layer;

forming a conductive plug in the first opening and the second opening, at least one of the plurality of liners not extending between a sidewall of the conductive plug and sidewalls of the plurality of first dielectric layers; and

after forming the conductive plug, forming a cap layer over the conductive plug, the cap layer comprising a dielectric material, the cap layer contacting a topmost surface of the conductive plug and a topmost surface of at least one of the plurality of liners.

9. The method of claim 8, wherein the cap layer extends over the plurality of liners.

10. The method of claim 8, wherein a subset of the plurality of liners extends over a backside of the first substrate.

11. The method of claim 8, wherein the conductive plug extends between two of the plurality of first metal lines in the first semiconductor chip.

12. The method of claim 8, further comprising forming at least one diffusion barrier layer between the conductive plug and one or more of the plurality of first dielectric layers.

13. The method of claim 8, wherein the plurality of liners includes an oxide layer and a nitride layer.

14. The method of claim 8, wherein the conductive plug electrically couples one of the plurality of first metal lines in the first semiconductor chip to the one of the plurality of second metal lines in the second semiconductor chip.

15. The method of claim 14, wherein the one of the plurality of first metal lines in the first semiconductor chip has a recess.

16. The method of claim 1, wherein forming the second trench comprises etching a metallization feature in the plurality of dielectric layers.

17. The method of claim 1, wherein a sidewall of the first liner of the plurality of liners and a sidewall of the second liner of the plurality of liners are coplanar.

18. The method of claim 17, wherein the sidewall of the first liner of the plurality of liners and the sidewall of the second liner of the plurality of liners physically contact the barrier layer.

19. The method of claim 5, wherein the liner comprises a diffusion barrier layer.

20. The method of claim 8, wherein the topmost surface of the conductive plug is level with the topmost surface of the at least one of the plurality of liners.