CLAIMS

1. A memory comprising:

a first write driver inverter including a first ground node;

a switch transistor coupled between the first ground node and ground, wherein the switch transistor is configured to switch off during a write assist period to float the ground for the first write driver inverter;

a boost capacitor; and

a first write driver transistor having a first terminal coupled to a bit line and a second terminal connected to a terminal of the boost capacitor, wherein the first write driver inverter is configured to invert a data signal to drive a gate of the first write driver transistor.

2. The memory of claim 1, further comprising:

a second write driver inverter including the first write driver transistor, wherein the first write driver transistor is an NMOS transistor, the first terminal is a drain terminal, and the second terminal is a source terminal.

3. The memory of claim 2, further comprising:

a bit line pair including the bit line and a complement of the bit line;

a third write driver inverter including a second ground node, wherein the switch transistor is also coupled between the second ground node and ground; and

a second NMOS transistor having a drain coupled to the complement of the bit line and a source connected to the terminal of the boost capacitor, wherein the third write driver is configured to invert a complement of the data signal to drive a gate of the second NMOS transistor.

4. The memory of claim 1, further comprising:

a first boost enable inverter for inverting a boost enable signal to drive a gate of the switch transistor.

5. The memory of claim 3, wherein the switch transistor comprises a first switch transistor coupled between the first ground node and ground and a second switch transistor coupled between the second ground node and ground.

6. The memory of claim 3, further comprising a column multiplexer configured to select for the bit line pair.

7. The memory of claim 6, further comprising a column multiplexer control signal generator including a control signal inverter for generating a column multiplexer control signal and having a third ground node, wherein the column multiplexer control signal generator further includes a column multiplexer switch transistor coupled between the third ground node and ground, and wherein the column multiplexer switch transistor is configured to switch off during the write assist period to float a ground for the control signal inverter.

8. The memory of claim 7, wherein the control signal inverter comprises a first control signal inverter including the third ground node and a second control signal inverter including a fourth ground node, and wherein the column multiplexer switch transistor comprises a first column multiplexer switch transistor coupled between the third ground node and ground and comprises a second column multiplexer switch transistor coupled between the fourth ground node and ground.

9. The memory of claim 1, wherein the memory comprises a static random access memory (SRAM).

10. The memory of claim 1, wherein the boost capacitor comprises a PMOS transistor.

11. The memory of claim 10, wherein the terminal of the boost capacitor is a gate for the PMOS transistor.

12. A method, comprising:

during a write operation for a memory, inverting a data input signal in a write driver inverter to ground a gate of a first write driver transistor having a drain terminal coupled to a bit line; and

during a write assist period for the write operation, boosting a source terminal of the first write driver transistor to a negative boost voltage while floating a ground for the write driver inverter to float the gate of the first write driver transistor.

13. The method of claim 12, further comprising:

during the write operation, inverting a complement of the data input signal to ground a gate of a second write driver transistor having a drain coupled to a complement of the bit line; and

during the write assist period for the write operation, boosting a source of the second write driver transistor to the negative boost voltage while floating the gate of the second write driver transistor.

14. The method of claim 12, further comprising:

switching off a switch transistor coupled between a ground node for the write driver inverter and ground during the write assist period to float a ground for the write driver inverter and to float the gate of the first write driver transistor.

15. The method of claim 12, further comprising:

during the write operation, inverting a first input control signal for a column multiplexer in a first control signal inverter and inverting a second input control signal for the column multiplexer in a second control signal inverter to control the column multiplexer to couple the drain terminal of the first write driver transistor to the bit line; and

during the write assist period for the write operation, floating a ground for the first control signal inverter and floating a ground for the second control signal inverter.

16. The method of claim 15, further comprising switching off a column multiplexer switch transistor to float the ground for the first control signal inverter and to float the ground for the second control signal inverter.

17. The method of claim 12, further comprising grounding an anode of a boost capacitor having a cathode connected to the source terminal of the first write driver transistor to boost the source terminal of the first write driver transistor to the negative boost voltage.

18. A memory, comprising:

a first write driver inverter;

means for floating a ground for the first write driver inverter during a write assist period;

a boost capacitor;

a boost enable inverter configured to invert a boost enable signal to ground an anode of the boost capacitor during the write assist period to provide a negative voltage boost to a cathode of the boost capacitor; and

a first write driver transistor having a first terminal coupled to a bit line and a second terminal connected to the cathode of the boost capacitor, wherein the write driver inverter is configured to invert a data signal to drive a gate of the first write driver transistor.

19. The memory of claim 18, further comprising a second write driver inverter including the first write driver transistor, wherein the first write driver transistor is an NMOS transistor, the first terminal is a drain terminal, and the second terminal is a source terminal.

20. The memory of claim 19, further comprising a column multiplexer configured to couple the first terminal to the bit line responsive to a control signal.