

Description

The present invention relates to a semiconductor integrated circuit arrangement comprising a semiconductor integrated circuit device containing an input MOS transistor responsive to an input signal, an input terminal, coupled to said input MOS transistor, for receiving said input signal; and an electrostatic discharge protection circuit limiter means coupled to said input MOS transistor and responsive to a given threshold control potential, for limiting at said variable threshold the electrostatic potential applied to the gate of said input MOS transistor, said threshold being variable according to said given threshold control potential.

Such a device is known from IBM Technical Disclosure Bulletin Vol. 22, No. 10, March 1980, pages 4452-4453 in the report entitled, "Voltage Programmable Protect Circuit"

Another electrostatic protection circuit is known from EP-A-0 042 305, using an MOS transistor connected to ground. The transistor is a depletion mode device, so that it conducts when no power is applied. When power is applied, it is switched off and no protection is provided.

Generally speaking, for an insulated-gate field effect transistor (MOS transistor) being formed with a metallic gate, insulation film and semiconductor elements, any countermeasure to avoid a faulty application of overvoltage to the gate electrode should be adopted. This is because such a faulty overvoltage application will rupture the electrical insulation of the gate insulation film and result in permanently damaging the MOS semiconductor device with a slight supply of power.

The gate oxide ruptures when the dielectric strength of the gate oxide, made of e.g. silicon dioxide, is more than approximately 10^7 V/cm. Thus, if a voltage of 30-50 V is applied across a 300-500 Å thick gate oxide, a rupture occurs. It is conventionally known that such permanent damage can be prevented by providing an input protection circuit which simply suppresses the peak potential of an input voltage below the voltage at which a rupture occurs.

However, when the above conventional input protection circuit is applied to an ultraviolet erasable non-volatile semiconductor memory (EPROM) or an electric erasable non-volatile semiconductor memory (EEPROM) and, if an input terminal of an EPROM or an EEPROM is designed to be commonly used for a low-voltage signal input and high-voltage signal input (whose potential will not cause said permanent damage), a certain problem arises. That is, when a high-voltage signal is supplied to the input terminal, the input protection circuit with a given fixed input limiting threshold could respond to the potential of a high-voltage input signal so

that the necessary high-voltage component exceeding the input limiting threshold is suppressed or blocked. Such inconvenience cannot be avoided according to said conventional input protection circuit.

It is accordingly an object of the present invention to provide an improved electrostatic discharge protection circuit for protecting from overvoltage damage a MOS-input device which is to be responsive to a high-voltage input signal.

According to the invention, the semiconductor integrated circuit device initially defined is characterized in that said limiter means includes a bipolar transistor whose emitter-collector path is inserted between the gate of said input MOS transistor and a fixed reference potential and the base of said bipolar transistor is connected to receive said given threshold control potential.

This invention can be more fully understood from the following detailed description when taken in conjunction with the accompanying drawing, in which:

Fig. 1 shows a schematic explanatory circuit configuration of a known protection circuit in which a gate-controlled MOS diode with a fixed gate potential is employed; and

Fig. 2 shows a circuit configuration of an embodiment of the present invention, in which a bipolar transistor with a fixed or variable base potential is employed.

Fig. 1 shows an electrostatic discharge protection circuit for protecting from overvoltage damage a MOS-input device which is to be responsive to a high-voltage input signal. A signal input terminal 11 receives an input signal. Terminal 11 is coupled via a resistor element 16 to an input node 14 of a MOS-input semiconductor integrated circuit 13 which contains an input MOS transistor 12 having a gate coupled to node 14. Node 14 is coupled to a circuit-ground (substrate) via a gate-controlled MOS diode 15 having a predetermined gate-controlled breakdown voltage (V_{SB}). The gate of the diode 15 receives a power source potential V_c (e.g. 5 volts).

According to the circuit of Fig. 1 the potential difference between the gate and drain of MOS diode 15 becomes V_c , because the gate receives potential V_c while the drain potential is substantially zero when no signal is input to terminal 11. In this case the gate-controlled breakdown voltage of diode 15 is equivalently increased by V_c from the intrinsic gate-controlled breakdown voltage V_{SB} of MOS diode 15 with zero-gate potential. That is, the limiting threshold for an input signal potential can be made variable according to the gate potential of MOS diode 15, and the responsive potential of the input signal can be set at a high value in proportion to the gate potential. On the other hand, even when

the semiconductor integrated circuit device itself is carried (at this time an electrostatic discharge is highly liable to occur), the gate of input MOS transistor 12 is protected perfectly. This is because, when carried, no power is supplied to the integrated circuit device so that $V_c = 0$ and the limiting threshold for the input signal potential is set at a low value which is substantially equal to the intrinsic gate-controlled breakdown voltage of MOS diode 15 with zero-gate potential.

Resistor element 16 between input terminal 11 and input node 14 serves to suppress an excessive input current fed into diode 15 and also to reduce the rate of change of an input signal voltage with a rapid potential change, thereby achieving the protection not only for input MOS transistor 12 but also for gate-controlled MOS diode 15. The resistance value of resistor element 16 is preferably 1-2 kohm.

Fig. 2 shows a circuit configuration of an embodiment of the present invention. In the embodiment of Fig. 2 a PNP bipolar transistor 15A is used in place of the gate-controlled MOS diode. The base of transistor 15A is responsive to a fixed or variable base potential V_b . When the potential at input node 14 exceeds the given base potential V_b of the base-emitter threshold voltage of transistor 15A, transistor 15A is rendered conductive so that node 14 is shunted to the circuit ground, thereby achieving the input circuit protection.

As will be understood from the above description, the limiting threshold for the circuit protection is varied by a threshold control potential (V_b) continuously or optionally applied to the base of protection transistor 15A. From this, MOS-input semiconductor circuit 13 is protected from damage due to an excessive high surge voltage input, while no signal blocking is effected for a high-voltage signal input so that semiconductor circuit 13 can respond to such a high-voltage signal input.

While the invention has been described in connection with what is presently considered to be the most practical and preferred embodiment, it is understood that the invention is not to be limited to the disclosed embodiment. For instance, MOS-input circuit 13 may include a digital circuit other than EPROM/EEPROM, or it may include a MOS-input analog circuit.

Claims

1. A semiconductor integrated circuit arrangement comprising: an integrated circuit device (13) containing an input MOS transistor (12) responsive to an input signal;
an input terminal (11), coupled to said input MOS transistor (12), for receiving said input signal; and

an electrostatic discharge protection circuit comprising: limiter means (15A) coupled to said input MOS transistor (12) and responsive to a given threshold control potential (V_b), for limiting at a variable threshold the electrostatic potential applied to the gate of said input MOS transistor (12), said threshold being variable according to said given threshold control potential (V_b),

characterized in that said limiter means (15A) includes a bipolar transistor (15A) whose emitter-collector path is inserted between the gate of said input MOS transistor (12) and a fixed reference potential and the base of said bipolar transistor (15A) is connected to receive said given threshold control potential (V_b).

2. A device according to claim 1, characterized in that said given threshold control potential (V_b) corresponds to a power source potential of said semiconductor device (13).
3. A device according to claim 1, characterized in that said given threshold control potential (V_b) is higher than a power source potential of said semiconductor device (13).
4. A device according to claim 1, 2 or 3, characterized in that said limiter means (15A, 16) includes a resistor element (16) coupled between said input terminal (11) and said bipolar transistor (15A).

Patentansprüche

1. Integrierte Halbleiterschaltungsanordnung mit:
einer integrierten Schaltungsvorrichtung (13) mit einem auf ein Eingangssignal ansprechenden Eingabe-MOS-Transistor (12);
einem Eingabeanschluß (11), verbunden mit dem Eingabe-MOS-Transistor (12) zum Empfangen des Eingangssignals; und
einer Schutzschaltung für eine elektrostatische Entladung mit:
einer Begrenzungseinrichtung (15A), verbunden mit dem Eingabe-MOS-Transistor (12) und ansprechend auf ein vorgegebenes Schwellsteuerpotential (V_b) zum Begrenzen des elektrostatischen Potentials, das an das Gate des Eingabe-MOS-Transistors (12) angelegt ist, auf eine vorbestimmte Schwelle, wobei die Schwelle gemäß dem vorgegebenen Schwellsteuerpotential (V_b) variabel ist,
dadurch gekennzeichnet, daß
die Begrenzungseinrichtung (15A) einen bipolaren Transistor (15A) beinhaltet, dessen Emitter-Kollektorpfad eingesetzt ist zwischen das Gate des Eingabe-MOS-Transistors (12)



the semiconductor integrated circuit device itself is carried (at this time an electrostatic discharge is highly liable to occur), the gate of input MOS transistor 12 is protected perfectly. This is because, when carried, no power is supplied to the integrated circuit device so that $V_c = 0$ and the limiting threshold for the input signal potential is set at a low value which is substantially equal to the intrinsic gate-controlled breakdown voltage of MOS diode 15 with zero-gate potential.

Resistor element 16 between input terminal 11 and input node 14 serves to suppress an excessive input current fed into diode 15 and also to reduce the rate of change of an input signal voltage with a rapid potential change, thereby achieving the protection not only for input MOS transistor 12 but also for gate-controlled MOS diode 15. The resistance value of resistor element 16 is preferably 1-2 kohm.

Fig. 2 shows a circuit configuration of an embodiment of the present invention. In the embodiment of Fig. 2 a PNP bipolar transistor 15A is used in place of the gate-controlled MOS diode. The base of transistor 15A is responsive to a fixed or variable base potential V_b . When the potential at input node 14 exceeds the given base potential V_b of the base-emitter threshold voltage of transistor 15A, transistor 15A is rendered conductive so that node 14 is shunted to the circuit ground, thereby achieving the input circuit protection.

As will be understood from the above description, the limiting threshold for the circuit protection is varied by a threshold control potential (V_b) continuously or optionally applied to the base of protection transistor 15A. From this, MOS-input semiconductor circuit 13 is protected from damage due to an excessive high surge voltage input, while no signal blocking is effected for a high-voltage signal input so that semiconductor circuit 13 can respond to such a high-voltage signal input.

While the invention has been described in connection with what is presently considered to be the most practical and preferred embodiment, it is understood that the invention is not to be limited to the disclosed embodiment. For instance, MOS-input circuit 13 may include a digital circuit other than EPROM/EEPROM, or it may include a MOS-input analog circuit.

Claims

1. A semiconductor integrated circuit arrangement comprising: an integrated circuit device (13) containing an input MOS transistor (12) responsive to an input signal;
an input terminal (11), coupled to said input MOS transistor (12), for receiving said input signal; and

an electrostatic discharge protection circuit comprising: limiter means (15A) coupled to said input MOS transistor (12) and responsive to a given threshold control potential (V_b), for limiting at a variable threshold the electrostatic potential applied to the gate of said input MOS transistor (12), said threshold being variable according to said given threshold control potential (V_b),

characterized in that said limiter means (15A) includes a bipolar transistor (15A) whose emitter-collector path is inserted between the gate of said input MOS transistor (12) and a fixed reference potential and the base of said bipolar transistor (15A) is connected to receive said given threshold control potential (V_b).

2. A device according to claim 1, characterized in that said given threshold control potential (V_b) corresponds to a power source potential of said semiconductor device (13).
3. A device according to claim 1, characterized in that said given threshold control potential (V_b) is higher than a power source potential of said semiconductor device (13).
4. A device according to claim 1, 2 or 3, characterized in that said limiter means (15A, 16) includes a resistor element (16) coupled between said input terminal (11) and said bipolar transistor (15A).

Patentansprüche

1. Integrierte Halbleiterschaltungsanordnung mit: einer integrierten Schaltungsvorrichtung (13) mit einem auf ein Eingangssignal ansprechenden Eingabe-MOS-Transistor (12); einem Eingabeanschluß (11), verbunden mit dem Eingabe-MOS-Transistor (12) zum Empfangen des Eingangssignals; und einer Schutzschaltung für eine elektrostatische Entladung mit: einer Begrenzungseinrichtung (15A), verbunden mit dem Eingabe-MOS-Transistor (12) und ansprechend auf ein vorgegebenes Schwellsteuerpotential (V_b) zum Begrenzen des elektrostatischen Potentials, das an das Gate des Eingabe-MOS-Transistors (12) angelegt ist, auf eine vorbestimmte Schwelle, wobei die Schwelle gemäß dem vorgegebenen Schwellsteuerpotential (V_b) variabel ist, dadurch gekennzeichnet, daß die Begrenzungseinrichtung (15A) einen bipolaren Transistor (15A) beinhaltet, dessen Emitter-Kollektorpfad eingesetzt ist zwischen das Gate des Eingabe-MOS-Transistors (12)



und ein festes Referenzpotential und die Basis des bipolaren Transistors (15A) verbunden ist, das vorgegebene Schwellsteuerpotential (Vb) zu empfangen.

2. Vorrichtung nach Anspruch 1, dadurch gekennzeichnet, daß das vorgegebene Schwellsteuerpotential (Vb) einem Spannungsquellenpotential der Halbleitervorrichtung (13) entspricht.
3. Vorrichtung nach Anspruch 1, dadurch gekennzeichnet, daß das vorgegebene Schwellsteuerpotential (Vb) höher ist als ein Spannungsquellenpotential der Halbleitervorrichtung (13).
4. Vorrichtung nach Anspruch 1, 2 oder 3, dadurch gekennzeichnet, daß die Begrenzungseinrichtung (15A, 16) ein Widerstandselement (16) beinhaltet, das zwischen dem Eingabeanschluß (11) und dem Bipolartransistor (15A) geschaltet ist.

donné (Vb) est supérieur à un potentiel de source d'alimentation dudit dispositif à semi-conducteur (13).

- 5 4. Dispositif selon l'une quelconque des revendications 1 à 3, caractérisé en ce que ledit moyen limiteur (15A, 16) comprend un élément résistant (16) couplé entre ladite borne d'entrée (11) et ledit transistor bipolaire (15A).

Revendications

1. Agencement de circuit intégré à semi-conducteur comprenant : un dispositif de circuit intégré (13) contenant un transistor à métal-oxyde-semi-conducteur MOS d'entrée (12) réagissant à un signal d'entrée ;
 une borne d'entrée (11), couplée audit transistor MOS d'entrée (12), pour recevoir ledit signal d'entrée ; et
 un circuit de protection contre les décharges électrostatiques comprenant : un moyen limiteur (15A) couplé audit transistor MOS d'entrée (12) et réagissant à un potentiel de réglage de seuil donné (Vb), pour limiter, à un seuil variable, le potentiel électrostatique appliqué à la grille dudit transistor MOS d'entrée (12), ledit seuil étant variable en fonction dudit potentiel de réglage de seuil donné (Vb),
 caractérisé en ce que ledit moyen limiteur (15A) comprend un transistor bipolaire (15A) dont la voie émetteur-collecteur est insérée entre la grille dudit transistor MOS d'entrée (12) et une borne de potentiel de référence fixe et la base dudit transistor bipolaire (15A) est connectée pour recevoir ledit potentiel de réglage de seuil donné (Vb).
2. Dispositif selon la revendication 1, caractérisé en ce que ledit potentiel de réglage de seuil donné (Vb) correspond à un potentiel de source d'alimentation dudit dispositif à semi-conducteur (13).
3. Dispositif selon la revendication 1, caractérisé en ce que ledit potentiel de réglage de seuil