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PRESSURE-FIT ELECTRICAL SOCKET
FOR DIRECT INTERCONNECTION TO A SEMICONDUCTOR CHIP

5 The present invention relates to electrical
sockets for signal level semiconductor chips, and, more
particularly, to electrical sockets that directly
interconnect to a semiconductor chip by a means of a
pressure fit.

10 Signal level semiconductor chips are thin,
wafer-like semiconductor devices that are used to
process information signals, for example, in electronic
calculators and microprocessors. Such chips typically
have a multiplicity of contact terminations on a side
that must be electrically interconnected to external
15 circuitry to permit electrical testing of the chips.
While electrical probes can be used to perform elec-
trical testing of semiconductor chips, thorough testing
of the chips requires more substantial electrical
contact to the contact terminations of the chip than
20 can be provided by the use of electrical probes. This
is because high frequency testing of the chips results
in the electrical probes having unacceptably high
values of inductance. Additionally preliminary opera-
tion of the chips at high voltage and high temperature
25 for a considerable period of time to eliminate detec-
tive chips, known as chip "burn-in", would appropriate
the use of expensive electrical probe apparatus for an
unduly long period of time. The high voltages and high
heat required for chip burn-in also pose a danger of
30 damaging the electrical probe apparatus.

Accordingly, thorough electrical testing of
semiconductor chips has been performed in the prior art

through permanent mounting of the chips, as by soldering or wire bonding, to discrete packages, which are then, in turn, pressure-fitted into electrical sockets. More economical electrical testing of semiconductor chips would be facilitated, however, if the chips could be directly interconnected into electrical sockets by mechanical pressure alone.

A further drawback of prior art permanent-mount discrete packages and associated electrical sockets is that the package-and-socket combination occupies a relatively large area of a completed semiconductor device package, such that there exists a relatively large spacing between multiple chips in the package. This results in significant signal delay between chips in the package, and also considerable signal losses and signal cross-talk in the package. Accordingly, it would also be desirable to provide smaller electrical sockets for signal level semiconductor chips, in which the chips may be spaced in close proximity to each other.

Accordingly an object of the invention is to provide direct, pressure-fit electrical sockets for signal level semiconductor chips that permit thorough electrical testing and burn-in of the chips.

A further object of the invention is to provide electrical sockets for signal level semiconductor chips that are small in size to permit the chips to be spaced in close proximity to each other.

It is a further object of the invention to provide electrical sockets for signal level semiconductor chips that exhibit high reliability.

The foregoing and further objects of the invention are realized, in preferred form, in a pressure-fit electrical socket for direct interconnection to a semiconductor chip of the type including multiple contact terminations on one side of a chip. The electrical socket comprises a flexible lead carrier with patterned leads thereon. Such patterned leads include multiple lead terminations configured in the reverse image of the contact terminations of the semiconductor chip. A centering frame is situated atop the flexible lead carrier, and has an aperture exposing the contact terminations of the flexible lead carrier, and being adapted to receive and align the semiconductor chip. The socket further comprises a rigid substrate on which the combination of the flexible substrate with the chip centering guide thereon is mounted. An elastically-deformable layer of silicon rubber is situated between the flexible lead carrier and the rigid substrate, beneath the lead terminations on the lead carrier. This arrangement permits the lead terminations to individually vary in spacing from the rigid substrate when the semiconductor chip is pressed against the lead terminations, thereby accommodating slight variations in the heights of the contact terminations on the semiconductor chip. Lastly, a means to apply pressure, such as a mechanical coil spring, may be included for forcing the semiconductor chip against the flexible lead carrier, to realize a pressure-fit electrical contact.

Embodiments of the invention will now be described, by way of example and with reference to the accompanying drawings, in which:-

Figure 1 is an exploded view in three dimensions of a pressure-fit electrical socket in accordance with the invention;

Figure 2 is a detail view of the electrical socket of Figure 1 shown in assembled form;

Figure 3 is a cross-sectional view of an assembled version of the socket of Figure 1, additionally illustrating a semiconductor chip and pressure means for consummating the electrical interconnection of the chip and the socket;

Figure 4 is a detail of the construction of Figure 3 illustrating the conductor chip being pressed into the socket; and

Figure 5 is a view similar to Figure 3, illustrating an electrical socket incorporating an electrical ground plane.

Figure 1 illustrates in exploded form a preferred electrical socket 10 in accordance with the invention. Socket 10 includes a flexible lead carrier layer 12 adapted to be mounted on a rigid substrate layer 14 by adhesive means (not shown) such as epoxy, for example. Flexible lead carrier 12 includes patterned electrical leads 12A, which include multiple lead terminations 12B. A lead pattern 12C is included on a rigid substrate 14, and is adapted to be interconnected to patterned leads 12A by solder (not shown), for example.

Between flexible lead carrier 12 and rigid substrate 14 is situated an elastically-deformable, or

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rubber-like, layer 16. Elastically-deformable layer 16 permits individual variations in the spacing of lead terminations 12B from rigid substrate 14 so as to accommodate slight variations in the heights of the contact terminations on a semiconductor chip (not shown) that is to be interconnected to socket 10.

Also included in electrical socket 10 is semiconductor chip centering frame 18, which is normally mounted atop flexible carrier 12, for example, by adhesive means (not shown) such as epoxy, or mechanical means (not shown) such as screws. Centering frame 18, which comprises an insulating material, includes an aperture 18A in which a semiconductor chip is received to be interconnected to socket 10, in accordance with the present invention.

Figure 2 is a detail view of electrical socket 10 of Figure 1 in assembled form and is partially in cross section. Depicted in Figure 2 are lead terminations 12B which comprise bumps of metal preferably formed of gold atop copper.

Figure 3 depicts, in assembled form, electrical socket 10 and a semiconductor chip 20 situated in aperture 18A of centering frame 18. Also depicted in Figure 3, in schematic form, is a pressure means 22, which suitably comprises a coil spring, and which preferably includes a heat-conductive material 22A, such as aluminum, for removal of heat from semiconductor chip 20.

Pressure means 22 forces semiconductor chip 20 downwardly in aperture 18A of electrical socket 10, so that, as more clearly illustrated in the detail view of Figure 4, elastically-deformable layer 16 may be deformed to permit lead terminations 12B of flexible

(A)

lead carrier 12 to individually vary in spacing from rigid substrate 14. This "lead-height variation" feature of electrical socket 10 enables the socket to accommodate slight variations in the heights of contact terminations 20A on semiconductor chip 20.

Figure 5 illustrates a modified electrical socket 10' that is especially well suited for high frequency operation of semiconductor device 20'. Electrical socket 10' is similar to electrical socket 10 shown in Figure 1, and, thus, has reference numerals similar to those used for socket 10. Socket 10' differs from socket 10 in that socket 10' includes a ground or shield plane 50 of copper, for example, situated directly atop rigid substrate 14'. As is known in the art, ground plane 50 is useful for high frequency operation of semiconductor chip 20. Other variations of rigid substrate 14 may incorporate one or more ground planes at different levels than ground plane 50 in Figure 5. For example, a silicon circuit board with multiple conducting levels may incorporate a ground plane in a center level, rather than atop the circuit board.

Various parts of the electrical sockets described herein are suitably composed of the following preferred materials, having the following preferred dimensions:

<u>Part</u>	<u>Preferred Material(s)</u>	<u>Preferred Dimension(s)</u>
Flexible lead carrier 12	Kapton polyimide film	0.5 to 3 mils thick
Patterned leads	Copper coated with thick copper	0.2-0.7 mil thick copper plus 0.1-0.3

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			mil gold
	Lead terminations 12B	Gold on copper	Square of 2x2 mils to 4x4 mils; copper thickness of 0.2-0.7 mils; gold thickness of 0.3 to 0.5 mil; center-to-center spacing between terminations of 6 mils or more
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10			
	Elastically-deformable layer 16	Room Temperature Vulcanizing (RTV) silicone rubber	2 to 5 mils
15			
	Chip centering frame 18	Mylar film or Kapton polyimide film	5-10 mils
20			
	Pressure means 22	Coil Spring	100-5000 psi, with 1100 psi most preferred

Kapton and Mylar are Registered Trade Marks.

A preferred method of constructing electrical socket 10 (Fig. 1) is to form a uniform layer of copper on flexible lead carrier 12, which may be accomplished using standard techniques. Gold bumps to complete lead terminations 12B are then formed at appropriate locations, preferably using standard photoresist additive plating technique. Patterned leads 12A are next formed from the foregoing uniform layer on lead carrier 12, preferably by standard photoresist etching technique. Leads 12A are then coated with gold by electroplating, for example, for corrosion protection. Substrate leads 12C are next formed on rigid substrate 14, which may be accomplished using standard

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techniques. An elastically-deformable layer, such as Room Temperature Vulcanizing (RTV) silicone rubber, is then placed on rigid substrate 14 to form layer 16. Flexible lead carrier 12 is affixed to rigid substrate 14, preferably by adhesive means, such as epoxy. Chip centering frame 18 is then placed atop flexible lead carrier 12, and properly positioned by aligning aperture 18A over lead terminations 12B in such a way that contact terminations 20A on semiconductor chip 20 are respectively aligned with the reverse-image lead terminations 12B when chip 20 is placed in aperture 18A. This alignment step can be facilitated by using a transparent-glass, substitute chip provided with contact terminations, which permits visual inspection of contact alignment through the transparent glass. A semiconductor chip 20 is then inserted in aperture 18A of chip centering frame 18 to a pressure of 1100 p.s.i. to force such terminations into intimate engagement with contact terminations 20A on the chip.

As an alternative embodiment of the invention, gold bumps (not shown) are formed on chip contact terminations 20A (see Figure 4), rather than on lead terminations 12B. The advantage of the non-gold bumped electrical socket is that the socket cannot be rendered defective as a result of damage to a gold bump, which may occur during socketing of the chip, for example.

The electrical socket of the foregoing, alternative embodiment is particularly beneficial when used with a multiplicity of like electrical sockets in a complete semiconductor device package, because the resulting package cannot be rendered defective by virtue of one or more defective gold bumps in the electrical sockets. On the other hand, electrical sockets



of the previously-described type are particularly beneficial for electrical testing of individual semiconductor chips that have not been provided with gold bumps.

The foregoing describes a pressure-fit
5 electrical socket that directly interconnects to a semiconductor chip. Multiple electrical sockets of the type described herein may beneficially be spaced closely together in a semiconductor device package, so as to reduce in the package, signal delay, signal
10 losses, and signal cross-talk. Moreover, semiconductor chips may be electrically tested in the sockets of the present invention without the need for permanent mounting of the chips in discrete packages before insertion into an electrical socket.

15 While only certain preferred features of the invention have been shown by way of illustration, many modifications and changes will occur to those skilled in the art.

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CLAIMS



1. A pressure-fit electrical socket for direct interconnection to a semiconductor chip of the type having multiple contact terminations on a side of the chip, the socket comprising:

(a) a flexible lead carrier with patterned electrical leads thereon, said leads including multiple lead terminations configured in the reverse image of the contact terminations on the semiconductor chip;

(b) a chip centering frame situated atop said flexible lead carrier and having an aperture exposing said lead terminations of said flexible lead carrier and being adapted to receive the semiconductor chip;

(c) a rigid substrate on which said flexible substrate with said centering guide thereon are mounted; and

(d) an elastically-deformable layer of silicon rubber situated between said flexible lead carrier and said rigid substrate, beneath said lead terminations on said lead carrier, so as to permit said lead terminations to individually vary in spacing from said rigid substrate when the semiconductor chip is pressed against said lead terminations.

2. An electrical socket according to Claim 1, further comprising means to apply pressure against the semiconductor chip to complete electrical interconnection of the chip and the socket.

3. An electrical socket according to Claim 1 or Claim 2, wherein said lead terminations each comprises gold on a layer of copper.

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4. An electrical socket according to any one of Claims 1 - 3, wherein said flexible lead carrier comprises a layer of insulating material of between 0.5 and 3 mils thickness.

5. An electrical socket according to Claim 4, wherein said flexible lead carrier comprises a layer of polyimide material.

6. An electrical socket according to any one of Claims 1 - 5, further comprising an electrical ground plane situated between said flexible lead carrier and said rigid substrate.

7. An electrical socket according to Claim 3 wherein: said layer of copper has a thickness in the range of 0.2 to 0.7 mils; and

said gold on said layer of copper has a thickness in the range of 0.3 to 0.5 mils.

8. An electrical socket according to any one of Claims 1 - 7 wherein said layer of silicon rubber extends underneath of said chip centering frame.

9. An electrical socket according to Claim 8 wherein said layer of silicon rubber tapers from a peak in said aperture of said chip centering frame to an edge terminating underneath of said chip centering frame.

10. A pressure-fit electrical socket substantially as hereinbefore described with reference to, and as illustrated in, the accompanying drawings.
