

Description

Technical field

This invention relates generally to reference circuits and, more particularly, to current reference circuits which minimize output errors resulting from variations in power supply voltage and device size matching errors.

Background art

Reference circuits which utilize either a base-to-emitter voltage, V_{BE} , or a delta V_{BE} to establish a reference voltage and current by both reference voltage means and reference current means are well known. Such a circuit is described in detail in U.S. Patent No. 4,342,926. Transistor devices which are size ratioed and coupled to the reference current in a conventional current mirror structure reflect the reference current to an output device which provides a bias voltage. Although known reference circuits may be made substantially process independent, power supply voltage independence typically exists only for power supply voltages of five volts or less. This is because most of the power supply voltage generally appears across a single transistor. Due to the conventional phenomenon known as channel length modulation, the transistor which reflects the majority of power supply voltage displays a finite output impedance. As a result, a current mismatch exists between the reference voltage means and reference current means. Whenever a resistor type reference current means is utilized, the current mismatch translates into an offset voltage existing across the resistor. Further, as the supply voltage is increased, the offset voltage increases which creates a dependence on the supply voltage. Although this voltage error is generally insignificant for power supply voltages of five volts or less, the output error becomes increasingly worse at high voltage levels for N-channel conductivity devices due to the conventional impact ionization phenomenon. P-channel conductivity devices also create an offset error but the offset error is not as pronounced as it is for N-channel conductivity devices at higher voltages.

Brief summary of the invention

It is an object of the present invention to provide an improved current source circuit.

Another object of the present invention is to provide a current source having reduced output error.

Yet another object of the present invention is to provide a current source having a high output impedance.

Yet a further object of the present invention is to provide a current source having reduced errors for operation at various power supply voltages.

In carrying out the above and other objects and advantages of the present invention, there is provided, in one form, a bias current reference circuit having a reference voltage established by a diode-connected device. A reference current

generator is coupled to the diode-connected device to provide a reference current which is proportional to the reference voltage. A unity gain amplifier having a predetermined impedance is coupled to both the diode-connected device and reference current generator and provides a bias voltage. Bias current means are coupled to the bias voltage and provide an output bias current. Buffer means, for substantially increasing the output impedance of the unity gain amplifier and decreasing the power supply variation dependency, are coupled to both the unity gain amplifier and the bias current means.

Brief description of the drawings

Fig. 1 illustrates in schematic form a current source circuit constructed in accordance with the preferred embodiment of the present invention; and

Fig. 2 illustrates in graphical form a reduction in output bias current error provided by the present invention.

Description of the preferred embodiment

Shown in the single drawing is a current source circuit 10 constructed in accordance with the preferred embodiment of the present invention. Current source 10 comprises generally reference voltage portion 11, reference current portion 12, unity gain amplifier portion 13, bias current portion 14 and buffer portion 15. It should readily be understood that the present invention may be practiced using any of numerous types of reference voltage means and reference current means. Two commonly known current sources utilize a base-to-emitter voltage, V_{BE} and a delta V_{BE} to provide a reference current. The present invention may be readily adapted for use with other types of reference voltage and current means such as a power supply and resistor. For purposes of illustration only, a current source circuit utilizing a delta V_{BE} will be described. Further, while specific N-channel and P-channel MOS devices are generally shown, it should be clear that current source 10 could be implemented by completely reversing the processing techniques (e.g. N-channel to P-channel) or by using other types of transistors.

Reference voltage portion 11 comprises a diode-connected bipolar transistor 17 having both the base and collector electrodes coupled together for receiving a power supply voltage V_{DD} . Reference current portion 12 comprises a bipolar transistor 18 having the collector electrode thereof coupled to power supply voltage V_{DD} , a base electrode coupled to the base and collector electrodes of bipolar transistor 17 and an emitter electrode. The emitter electrode of transistor 18 is coupled to a first terminal of a resistor 19.

Unity gain amplifier portion 13 comprises P-channel transistors 21 and 22 and N-channel transistors 23 and 24. Buffer portion 15 comprises N-channel transistors 25 and 26. P-channel transistor 21 has a source electrode coupled to an

emitter electrode of transistor 17 and a gate electrode coupled to its drain electrode, to a gate electrode of transistor 22 and to a drain electrode of transistor 25. P-channel transistor 22 has a source electrode coupled to a second terminal of resistor 19 and a drain electrode coupled to a gate electrode of transistors 25, to a gate electrode of transistor 26 and to a drain electrode of transistor 24. Source electrode of transistor 25 is coupled to both a drain electrode and a gate electrode of transistor 23 and to a gate electrode of transistor 24. Transistors 23 and 24 each have a source electrode coupled to a second supply voltage V_{SS} which is more negative than supply voltage V_{DD} . Therefore, transistors 21 and 23 are effectively coupled as diodes.

Bias current portion 14 comprises a P-channel transistor 27 and an N-channel transistor 28. Transistor 27 has a source electrode coupled to supply voltage V_{DD} and both a gate electrode and a drain electrode coupled together to provide an output bias reference voltage. A drain electrode of transistor 26 of buffer portion 15 is coupled to the drain electrode of transistor 27 and a source electrode of transistor 26 is coupled to a drain electrode of transistor 28. A gate electrode of transistor 28 is coupled to the gate electrodes of transistors 23 and 24 and the drain electrode of transistor 23. A source electrode of transistor 28 is coupled to supply voltage V_{SS} .

In a preferred form, each source electrode of N-channel transistors 23, 24, 25, 26 and 28 is coupled to the respective substrate thereof. Although the present invention may be practiced without connecting the source electrode and substrate of each of these transistors, the threshold voltage of each transistor connected in this manner is effectively lowered. Therefore, a lower voltage is required to make N-channel transistors 23, 24, 25, 26 and 28 conductive which allows for a greater voltage operation.

In operation, transistor 17 provides a fixed reference voltage which is equal to the V_{BE} of transistor 17. Transistor 18 also has a base-to-emitter voltage associated therewith. To utilize a delta V_{BE} current source, the current densities of transistors 17 and 18 must be different so that transistors 17 and 18 have a different V_{BE} voltage. Applying Kirchhoff's voltage law to the loop formed by transistors 17, 18, 21 and 22 and resistor 19, if transistors 21 and 22 are matched devices having equal current densities, it can be readily shown that the voltage across resistor 19 is equal to the difference between the base-to-emitter voltages of transistors 17 and 18, delta V_{BE} . Resistor 19 therefore provides an accurate reference current through transistors 22 and 24. A proportional reference current is mirrored or reflected through series-connected transistors 21, 25 and 23.

Transistors 23, 24 and 25 function as a current source. Since transistors 17, 21 and 23 are connected functionally as diodes, the majority of the voltage potential between V_{DD} and V_{SS} is across the drain and source electrodes of transistor 25.

Transistors 23 and 24 have a substantially constant voltage potential existing across the current electrodes thereof. The voltage potential across the drain and source electrodes of transistor 24 is the sum of the gate to source voltage of transistor 24 and the gate to source voltage of transistor 25. The voltage potential across the drain and source electrodes of transistor 23 is the gate to source voltage of transistor 23. Thus transistor 25 buffers transistor 23 from most of the voltage potential between V_{DD} and V_{SS} by having most of the voltage potential across its drain and source electrodes.

To establish the output bias reference voltage at the gate electrode of transistor 27, transistor 28 is coupled to transistor 23 so that a bias current, I , flows through transistor 28. Bias current I is proportional to or is the same current which flows through transistor 23. Further, substantially the same voltage which appears across the gate and source electrodes of transistor 23 also appears across the gate and source electrodes of transistor 28. Transistor 26 is a cascode device and performs an analogous function to transistor 25 by having most of the voltage potential between V_{DD} and V_{SS} across its drain and source electrodes instead of this voltage appearing across transistor 28. By applying Kirchhoff's voltage law to the loop formed by transistors 23, 25, 26 and 28, it can be readily seen that the voltage which exists across the gate and source electrodes of transistors 25 and 26 are substantially equal in magnitude. Since the drain to source voltage of each of transistors 23, 24 and 28 is small in comparison with the voltage differential of V_{DD} and V_{SS} , the natural impedance of each transistor is large and is therefore not decreased by impact ionization. Additionally, by having a small drain to source voltage across each of transistors 23, 24 and 28, the effect of matching errors associated with these transistors is minimized. Further, transistors 25 and 26 absorb any variation in the difference between V_{DD} and V_{SS} without affecting the current through each transistor. Therefore, the effective impedance of current source 20 is greatly increased.

To fully appreciate the advantages of the higher effective impedance provided by buffer portion 15, consider the operation of current source 10 without transistors 25 and 26, without transistor 23 being diode-connected and with transistor 24 being diode-connected. In such a circuit configuration, the voltage across transistor 23 is typically much higher than the voltage across transistor 24 which is diode-connected. Due to the fact that transistors 23 and 24 have a finite output impedance caused by channel length modulation, the current mismatch between transistors 23 and 24 translates into an offset voltage across resistor 19 which provides an error in the output bias current. As the voltage across the drain electrode of transistor 23 increases, the amount of offset voltage across resistor 19 increases proportionately. The output bias voltage error becomes more pronounced at high voltage levels

on N-channel transistors due to impact ionization. Impact ionization is a phenomenon in which charge carriers are lost to the substrate at increasingly higher drain to source voltage potentials thereby decreasing the impedance of the transistors. The effect of a reduced transistor impedance is an increase in the offset voltage across resistor 19 which thereby increases the output bias current, I.

Shown in Fig. 2 is a graph which illustrates in curve (A) the offset voltage across resistor 19 for a range of V_{DD} supply voltages if transistors 25 and 26 are removed from current source 10 and if transistor 24 is diode-connected and transistor 23 is not diode-connected. Also shown in curve (B) of Fig. 2 is a graph illustrating the offset voltage across resistor 19 for the same range of V_{DD} supply voltages for the present invention illustrated in Fig. 1. As can be readily seen, a substantial reduction in offset voltage and therefore supply voltage dependency and output bias current error is achieved by the present invention.

It should be readily apparent that in order to prevent the possibility of an inactive state, a conventional start-up circuit (not shown) is required to allow start-up current to flow through reference voltage portion 11 when the output bias is below a predetermined threshold.

Claims

1. A current source circuit having reduced error, comprising:

reference voltage means (11) having a diode-connected device (17), for providing a reference voltage proportional to a bias current;

reference current means (12) coupled to the reference voltage means, for providing a reference current proportional to the reference voltage;

unity gain amplifier means (13) having a predetermined output impedance coupled to both said reference voltage and said reference current means, for providing a bias voltage proportional to said reference current;

bias current means (14) coupled to said unity gain amplifier means, for providing an output bias current proportional to said bias voltage; and

buffer means (15) coupled to both said unity gain amplifier means and said bias current means, for substantially increasing the output impedance of said unity gain amplifier thereby decreasing power supply variation dependency.

2. The current source circuit of claim 1 wherein said reference current means (12) comprise:

a first transistor (18) having a first current electrode coupled to a first power supply voltage terminal (V_{DD}) for receiving a first supply voltage, a control electrode coupled to said reference voltage means (11; 17), and a second current electrode; and

resistance means (19) having a first terminal coupled to the second current electrode of said first transistor (18) and a second terminal coupled to said unity gain amplifier means (13).

3. The current source circuit of claim 2 wherein the diode-connected device of said reference voltage means (11) is a second transistor (17) having both a first current electrode and a control electrode coupled to the first supply voltage (V_{DD}) and a second current electrode coupled to said unity gain amplifier means (13).

4. The current source circuit of claim 3 wherein said first (18) and second (17) transistors are bipolar transistors.

5. The current source circuit of claim 3 wherein said unity gain amplifier means (13) comprise:

a third transistor (21) of a first conductivity type having a first current electrode coupled to the second current electrode of said second transistor (17), a second current electrode coupled to both a control electrode thereof and to said buffer means (15);

a fourth transistor (22) of said first conductivity type having a first current electrode coupled to the second terminal of said resistance means (19), a control electrode coupled to both the control electrode and second current electrode of said third transistor (21) and to said unity gain amplifier means (13), and a second current electrode;

a fifth transistor (24) of a second conductivity type having a first current electrode coupled to the second current electrode of said fourth transistor (22) and to said buffer means (15), a second current electrode coupled to a second supply voltage terminal for receiving a second supply voltage (V_{SS}), and a control electrode; and

a sixth transistor (23) of said second conductivity type having a first current electrode coupled to a control electrode thereof, to the control electrode of said fifth transistor (24), to said buffer means (15) and to said bias current means (14), and a second current electrode coupled to the second supply voltage terminal (V_{SS}).

6. The current source circuit of claim 5 wherein said buffer means (15) comprise:

a seventh transistor (25) of said second conductivity type having a first current electrode coupled to the second current electrode of said third transistor (21), a second current electrode coupled to the first current electrode of said sixth transistor (23), and a control electrode; and

an eighth transistor (26) of said second conductivity type having first and second current electrodes coupled to said bias current means (14), and a control electrode coupled to the control electrode of said seventh transistor (25), to the second current electrode of said fourth transistor (22) and to the first current electrode of said fifth transistor (24).

7. The current source circuit of claim 6 wherein said bias current means (14) comprise:

a ninth transistor (27) of said first conductivity type having a first current electrode coupled to said first supply voltage terminal (V_{DD}), and a control electrode coupled to both a second current electrode thereof and the first current electrode of said eighth transistor (26), for providing an output voltage proportional to said output bias current; and



on N-channel transistors due to impact ionization. Impact ionization is a phenomenon in which charge carriers are lost to the substrate at increasingly higher drain to source voltage potentials thereby decreasing the impedance of the transistors. The effect of a reduced transistor impedance is an increase in the offset voltage across res. 19 which thereby increases the output bias current, I.

Shown in Fig. 2 is a graph which illustrates in curve (A) the offset voltage across resistor 19 for a range of V_{DD} supply voltages if transistors 25 and 26 are removed from current source 10 and if transistor 24 is diode-connected and transistor 23 is not diode-connected. Also shown in curve (B) of Fig. 2 is a graph illustrating the offset voltage across resistor 19 for the same range of V_{DD} supply voltages for the present invention illustrated in Fig. 1. As can be readily seen, a substantial reduction in offset voltage and therefore supply voltage dependency and output bias current error is achieved by the present invention.

It should be readily apparent that in order to prevent the possibility of an inactive state, a conventional start-up circuit (not shown) is required to allow start-up current to flow through reference voltage portion 11 when the output bias is below a predetermined threshold.

Claims

1. A current source circuit having reduced error, comprising:

reference voltage means (11) having a diode-connected device (17), for providing a reference voltage proportional to a bias current;

reference current means (12) coupled to the reference voltage means, for providing a reference current proportional to the reference voltage;

unity gain amplifier means (13) having a predetermined output impedance coupled to both said reference voltage and said reference current means, for providing a bias voltage proportional to said reference current;

bias current means (14) coupled to said unity gain amplifier means, for providing an output bias current proportional to said bias voltage; and

buffer means (15) coupled to both said unity gain amplifier means and said bias current means, for substantially increasing the output impedance of said unity gain amplifier thereby decreasing power supply variation dependency.

2. The current source circuit of claim 1 wherein said reference current means (12) comprise:

a first transistor (18) having a first current electrode coupled to a first power supply voltage terminal (V_{DD}) for receiving a first supply voltage, a control electrode coupled to said reference voltage means (11; 17), and a second current electrode; and

resistance means (19) having a first terminal coupled to the second current electrode of said first transistor (18) and a second terminal coupled to said unity gain amplifier means (13).

3. The current source circuit of claim 2 wherein the diode-connected device of said reference voltage means (11) is a second transistor (17) having both a first current electrode and a control electrode coupled to the first supply voltage (V_{DD}) and a second current electrode coupled to said unity gain amplifier means (13).

4. The current source circuit of claim 3 wherein said first (18) and second (17) transistors are bipolar transistors.

5. The current source circuit of claim 3 wherein said unity gain amplifier means (13) comprise:

a third transistor (21) of a first conductivity type having a first current electrode coupled to the second current electrode of said second transistor (17), a second current electrode coupled to both a control electrode thereof and to said buffer means (15);

a fourth transistor (22) of said first conductivity type having a first current electrode coupled to the second terminal of said resistance means (19), a control electrode coupled to both the control electrode and second current electrode of said third transistor (21) and to said unity gain amplifier means (13), and a second current electrode;

a fifth transistor (24) of a second conductivity type having a first current electrode coupled to the second current electrode of said fourth transistor (22) and to said buffer means (15), a second current electrode coupled to a second supply voltage terminal for receiving a second supply voltage (V_{SS}), and a control electrode; and

a sixth transistor (23) of said second conductivity type having a first current electrode coupled to a control electrode thereof, to the control electrode of said fifth transistor (24), to said buffer means (15) and to said bias current means (14), and a second current electrode coupled to the second supply voltage terminal (V_{SS}).

6. The current source circuit of claim 5 wherein said buffer means (15) comprise:

a seventh transistor (25) of said second conductivity type having a first current electrode coupled to the second current electrode of said third transistor (21), a second current electrode coupled to the first current electrode of said sixth transistor (23), and a control electrode; and

an eighth transistor (26) of said second conductivity type having first and second current electrodes coupled to said bias current means (14), and a control electrode coupled to the control electrode of said seventh transistor (25), to the second current electrode of said fourth transistor (22) and to the first current electrode of said fifth transistor (24).

7. The current source circuit of claim 6 wherein said bias current means (14) comprise:

a ninth transistor (27) of said first conductivity type having a first current electrode coupled to said first supply voltage terminal (V_{DD}), and a control electrode coupled to both a second current electrode thereof and the first current electrode of said eighth transistor (26), for providing an output voltage proportional to said output bias current; and



a tenth transistor (28) of said second conductivity type having a first current electrode coupled to the second current electrode of said eighth transistor (26), a control electrode coupled to the control electrodes of said fifth (24) and sixth (23) transistors and to the first current electrode of said sixth transistor (23), and a second current electrode coupled to said second supply voltage (V_{SS}).

8. The current source circuit of claim 7 wherein at least one of said fifth (24), sixth (23), seventh (25), eighth (26) and tenth (28) transistors has its second current electrode connected to the substrate thereof, thereby reducing its threshold voltage.

9. A delta V_{BE} current source circuit comprising: reference voltage means (11) comprising a first diode-connected bipolar transistor (17), for providing a reference voltage proportional to a bias current;

reference current means (12) coupled to the reference voltage means (11) comprising a second bipolar transistor (18) coupled in series with a resistor (19), for providing a reference current proportional to the ratio of the difference in the base to emitter voltages, delta V_{BE} , of said first (17) and second (18) bipolar transistors and proportional to the resistance of said resistor (19);

unity gain amplifier means (13) having a predetermined output impedance coupled to both said reference voltage (11) and said reference current (12) means, for providing a bias voltage proportional to said reference current;

bias current means (14) coupled to said amplifier means (13), for providing an output bias current proportional to said bias voltage; and

buffer means (15) coupled to both said amplifier means (13) and to said bias current means (14), for substantially increasing the output impedance of said amplifier means (13) thereby decreasing power supply variation dependency.

10. The delta V_{BE} current source of claim 9 wherein said amplifier means (13) comprises:

a third transistor (21) of a first conductivity type having a first current electrode coupled to the first bipolar transistor (17), and a control electrode coupled to both its second current electrode and said amplifier means;

a fourth transistor (22) of said first conductivity type having a first current electrode coupled to said resistor (19), a control electrode coupled to the control electrode of said third transistor (21), and a second current electrode coupled to said amplifier means;

a fifth transistor (24) of a second conductivity type having a first current electrode coupled to the second current electrode of said fourth transistor (22), a second current electrode coupled to a supply voltage terminal for receiving a supply voltage (V_{SS}), and a control electrode coupled to both of said buffer means (15) and said bias current means (14); and

a sixth transistor (23) of said second conductivity type having a first current electrode coupled to both its control electrode and the control

electrode of said fifth transistor (24) and a second current electrode coupled to said supply voltage terminal (V_{SS}).

Patentansprüche

1. Stromversorgungsschaltung mit verminderter Fehler, enthaltend:

eine Bezugsspannungseinrichtung (11) mit einer als Diode geschalteten Einrichtung (17) zum Erzeugen einer Bezugsspannung, die proportional einem Vorstrom ist;

eine Bezugsstromeinrichtung (12), die mit der Bezugsspannungseinrichtung verbunden ist, um einen der Bezugsspannung proportionalen Bezugsstrom zu liefern;

eine Einheitsverstärkungseinrichtung (13) mit vorbestimmter Ausgangsimpedanz, die sowohl mit der Bezugsspannungseinrichtung als auch mit der Bezugsstromeinrichtung verbunden ist, um eine Vorspannung abzugeben, die proportional dem Bezugsstrom ist;

eine Vorstromeinrichtung (14), die mit der Einheitsverstärkungseinrichtung verbunden ist, um einen Ausgangsvorstrom abzugeben, der proportional der Vorspannung ist;

eine Puffereinrichtung (15), die sowohl mit der Einheitsverstärkungseinrichtung als auch mit der Vorstromeinrichtung verbunden ist, um die Ausgangsimpedanz der Einheitsverstärkungseinrichtung im wesentlichen zu steigern, um dadurch die Abhängigkeit von Versorgungsspannungsschwankungen zu vermindern.

2. Stromversorgungsschaltung nach Anspruch 1, bei der die Bezugsstromeinrichtung (12) umfaßt:

einen ersten Transistor (18) mit einer ersten Stromelektrode, die mit einem ersten Versorgungsspannungsanschluß (V_{DD}) verbunden ist, um eine erste Versorgungsspannung entgegenzunehmen, die Steuerelektrode, die mit der Bezugsspannungseinrichtung (11; 17) verbunden ist, und einer zweiten Stromelektrode; und

eine Widerstandseinrichtung (19), mit einem ersten Anschluß, der mit der zweiten Stromelektrode des ersten Transistors (18) verbunden ist, und einem zweiten Anschluß, der mit der Einheitsverstärkungseinrichtung (13) verbunden ist.

3. Stromversorgungsschaltung nach Anspruch 2, bei der die zur Diode geschaltete Einrichtung der Bezugsspannungseinrichtung (11) eine zweite Transistor (17) ist, von dem sowohl eine erste Stromelektrode als auch eine Steuerelektrode mit der ersten Versorgungsspannung (V_{DD}) verbunden ist und eine zweite Stromelektrode mit der Einheitsverstärkungseinrichtung (13) verbunden ist.

4. Stromversorgungsschaltung nach Anspruch 3, bei der die ersten und zweiten Transistoren (18, 17) bipolare Transistoren sind.

5. Stromversorgungsschaltung nach Anspruch 3, bei der die Einheitsverstärkungseinrichtung (13) enthält:

einen dritten Transistor (21) eines ersten Leitfähigkeitstyps mit einer ersten Stromelektrode, die



mit der zweiten Stromelektrode des zweiten Transistors (17) verbunden ist, einer zweiten Stromelektrode, die sowohl mit seiner Steuerelektrode und mit der Puffereinrichtung (15) verbunden ist; einen vierten Transistor (22) vom ersten Leitfähigkeitstyp mit einer ersten Stromelektrode, die mit dem zweiten Anschluß der Widerstandseinrichtung (19) verbunden ist, einer Steuerelektrode, die sowohl mit der Steuerelektrode und der zweiten Stromelektrode des dritten Transistors (21) und mit der Einheitsverstärkungseinrichtung (13) verbunden ist, und einer zweiten Stromelektrode;

einen fünften Transistor (24) eines zweiten Leitfähigkeitstyps mit einer ersten Stromelektrode, die mit der zweiten Stromelektrode des vierten Transistors (22) und mit der Puffereinrichtung (15) verbunden ist, einer zweiten Stromelektrode, die mit einem zweiten Versorgungsspannungsanschluß verbunden ist, um einen zweiten Versorgungsspannung (V_{SS}) entgegenzunehmen, und einer Steuerelektrode; und

einen sechsten Transistor (23) vom zweiten Leitfähigkeitstyp mit einer ersten Stromelektrode, die mit seiner Steuerelektrode, mit der Steuerelektrode des fünften Transistors (24), der Puffereinrichtung (15) und der Vorstromeinrichtung (12) verbunden ist, und einer zweiten Stromelektrode, die mit dem zweiten Versorgungsspannungsanschluß (V_{SS}) verbunden ist.

6. Stromversorgungsschaltung nach Anspruch 5, bei der die Puffereinrichtung (15) enthält:

einen siebenten Transistor (25) vom zweiten Leitfähigkeitstyp mit einer ersten Stromelektrode, die mit der zweiten Stromelektrode des dritten Transistors (21) verbunden ist, einer zweiten Stromelektrode, die mit der ersten Stromelektrode des sechsten Transistors (23) verbunden ist, und einer Steuerelektrode; und

einen achten Transistor (26) vom zweiten Leitfähigkeitstyp mit ersten und zweiten Stromelektroden, die mit der Vorstromeinrichtung (14) verbunden sind, und einer Steuerelektrode, die mit der Steuerelektrode des siebenten Transistors (25), der zweiten Stromelektrode des vierten Transistors (22) und der ersten Stromelektrode des fünften Transistors (24) verbunden ist.

7. Stromversorgungsschaltung nach Anspruch 6, bei der die Vorstromeinrichtung (14) enthält:

einen neunten Transistor (27) vom ersten Leitfähigkeitstyp mit einer ersten Stromelektrode, die mit dem ersten Versorgungsspannungsanschluß (V_{DD}) verbunden ist, und einer Steuerelektrode, die sowohl mit seiner zweiten Stromelektrode und mit der ersten Stromelektrode des achten Transistors (26) verbunden ist, um eine Ausgangsspannung zu liefern, die proportional dem Ausgangsvorstrom ist; und

einen zehnten Transistor (28) vom zweiten Leitfähigkeitstyp mit einer ersten Stromelektrode, die mit der zweiten Stromelektrode des achten Transistors (26) verbunden ist, einer Steuerelektrode, die mit den Steuerelektroden der fünften und sechsten Transistoren (24, 23) und mit der ersten Stromelektrode des sechsten Transistors (23) ver-

bunden ist, und einer zweiten Stromelektrode, die mit der zweiten Versorgungsspannung (V_{SS}) verbunden ist.

8. Stromversorgungsschaltung nach Anspruch 7, bei der wenigstens einer der fünften, sechsten, siebenten, achten und neunten Transistoren (24, 23, 25, 26, 28) mit seiner zweiten Stromelektrode mit dem Substrat desselben verbunden ist, um dadurch seine Schwellenspannung zu vermindern.

9. Delta- V_{BE} -Stromversorgungsschaltung, enthaltend:

eine Bezugsspannungseinrichtung (11) mit einer ersten, zur Diode geschalteten bipolaren Transistor (17) zum Erzeugen einer Bezugsspannung, die proportional einem Vorstrom ist;

eine Bezugsstromeinrichtung (12), die mit der Bezugsspannungseinrichtung (11) verbunden ist, enthaltend einen zweiten bipolaren Transistor (18), der in Serie mit einem Widerstand (19) geschaltet ist, um einen Bezugsstrom zu liefern, der proportional dem Verhältnis der Differenz der Basis/Emitter-Spannungen Delta- V_{BE} der ersten und zweiten bipolaren Transistoren (17, 18) und proportional zum Widerstandswert des genannten Widerstandes (19) ist;

eine Einheitsverstärkungseinrichtung (13) mit einer vorbestimmten Ausgangsimpedanz, die sowohl mit der Bezugsspannungseinrichtung (11) als auch mit der Bezugsstromeinrichtung (12) verbunden ist, um eine Vorspannung zu liefern, die proportional dem Bezugsstrom ist;

eine Vorstromeinrichtung (14), die mit der Verstärkungseinrichtung (13) verbunden ist, um einen Ausgangsvorstrom zu liefern, der proportional der Vorspannung ist; und

eine Puffereinrichtung (15), die sowohl mit der Verstärkungseinrichtung (13) als auch mit der Vorstromeinrichtung (14) verbunden ist, um im wesentlichen die Ausgangsimpedanz der Verstärkungseinrichtung (13) zu steigern, um dadurch die Abhängigkeit von Versorgungsspannungsschwankungen zu vermindern.

10. Delta- V_{BE} -Stromquelle nach Anspruch 9, bei der die Verstärkungseinrichtung (13) enthält:

einen dritten Transistor (21) eines ersten Leitfähigkeitstyps mit einer ersten Stromelektrode, die mit dem ersten bipolaren Transistor (17) verbunden ist, und einer Steuerelektrode, die sowohl mit seiner zweiten Stromelektrode als auch mit der Verstärkungseinrichtung verbunden ist;

einen vierten Transistor (22) vom ersten Leitfähigkeitstyp, mit einer ersten Stromelektrode, die mit dem Widerstand (19) verbunden ist, einer Steuerelektrode, die mit der Steuerelektrode des dritten Transistors (21) verbunden ist, und einer zweiten Stromelektrode, die mit der Verstärkungseinrichtung verbunden ist;

einen fünften Transistor (24) eines zweiten Leitfähigkeitstyps, mit einer ersten Stromelektrode, die mit der zweiten Stromelektrode des vierten Transistors (22) verbunden ist, einer zweiten Stromelektrode, die mit dem Versorgungsspannungsanschluß zur Aufnahme einer Versorgungsspannung (V_{SS}) verbunden ist, und einer Steuerelek-



trode, die sowohl mit der Puffereinrichtung (15) als auch mit der Vorstromeinrichtung (14) verbunden ist, und einen sechsten Transistor (26) vom zweiten Leitfähigkeitstyp, mit einer ersten Stromelektrode, die sowohl mit seiner Steuerelektrode als auch mit der Steuerelektrode des fünften Transistors (24) verbunden ist, und einer zweiten Stromelektrode, die mit dem Versorgungsspannungsanschluß (V_{SS}) verbunden ist.

Revendications

1. Circuit de source de courant avec une erreur réduite, comportant:

un dispositif de tension de référence (11) comprenant un dispositif connecté en diode (12) pour produire une tension de référence proportionnelle à un courant de polarisation,

un dispositif de courant de référence (12) connecté audit dispositif de tension de référence pour produire un courant de référence proportionnel à la tension de référence,

un dispositif d'amplificateur à gain unitaire (13) ayant une impédance de sortie prédéterminée couplée avec ladite tension de référence et ledit dispositif de courant de référence pour produire une tension de polarisation proportionnelle audit courant de référence,

un dispositif de courant de polarisation (14) couplé avec ledit dispositif amplificateur à gain unitaire pour produire un courant de polarisation de sortie proportionnel à ladite tension de polarisation, et

un dispositif tampon (15) couplé avec ledit dispositif amplificateur à gain unitaire et ledit dispositif de courant de polarisation pour augmenter substantiellement l'impédance de sortie dudit amplificateur à gain unitaire, en diminuant ainsi la dépendance aux variations d'alimentation.

2. Circuit de source et de courant selon la revendication 1, dans lequel ledit dispositif de courant de référence (12) comporte:

un premier transistor (18) comprenant une première électrode de courant couplée avec une première borne de tension d'alimentation (V_{DD}) pour recevoir une première tension d'alimentation, une électrode de commande couplée avec ledit dispositif de tension de référence (11; 17) et une seconde électrode de courant, et

un dispositif à résistance (19) comprenant une première borne couplée avec la seconde électrode de courant dudit premier transistor (18) et une seconde borne couplée avec ledit dispositif amplificateur à gain unitaire (13).

3. Circuit de source de courant selon la revendication 2, dans lequel le dispositif connecté en diode dudit dispositif de tension de référence (11) est un second transistor (17) comportant une première électrode de courant et une électrode de commande couplée avec la première tension d'alimentation (V_{DD}) et une seconde électrode de courant couplée avec ledit dispositif amplificateur à gain unitaire (13).

4. Circuit de source de courant selon la revendication 3, dans lequel ledit premier (18) et ledit second (17) transistors sont des transistors bipolaires.

5. Circuit de source de courant selon la revendication 3, dans lequel ledit dispositif amplificateur à gain unitaire (13) comporte:

un troisième transistor (21) d'un premier type de conductivité ayant une première électrode de courant couplée avec la seconde électrode de courant dudit second transistor (17), une seconde électrode de courant couplée avec son électrode de commande et ledit dispositif de tampon (15),

un quatrième transistor (22) dudit premier type de conductivité ayant une première électrode de courant couplée avec la seconde borne dudit dispositif à résistance (19), une électrode de commande couplée avec l'électrode de commande et la seconde électrode de courant dudit troisième transistor (21) et avec ledit dispositif amplificateur à gain unitaire (13), et une seconde électrode de courant,

un cinquième transistor (24) d'un second type de conductivité ayant une première électrode de courant couplée avec la seconde électrode de courant dudit quatrième transistor (22) et avec ledit dispositif de tampon (15), une seconde électrode de courant couplée avec une seconde borne de tension d'alimentation pour recevoir une seconde tension d'alimentation (V_{SS}) et une électrode de commande, et

un sixième transistor (23) dudit second type de conductivité ayant une première électrode de courant couplée avec son électrode de commande, avec l'électrode de commande dudit cinquième transistor (24), avec ledit dispositif de tampon (15) et avec ledit dispositif de courant de polarisation (12) et une seconde électrode de courant couplée avec la seconde borne de tension d'alimentation (V_{SS}).

6. Circuit de source de courant selon la revendication 5, dans lequel ledit dispositif de tampon (15) comporte:

un septième transistor (25) dudit second type de conductivité ayant une première électrode de courant couplée avec la seconde électrode de courant dudit troisième transistor (21), une seconde électrode de courant couplée avec la première électrode de courant dudit sixième transistor (23) et une électrode de commande, et

un huitième transistor (26) dudit seconde type de conductivité ayant une première et une seconde électrodes de courant couplées avec ledit dispositif de courant de polarisation (14) et une électrode de commande couplée avec l'électrode de commande dudit septième transistor (25), avec la seconde électrode de courant dudit quatrième transistor (22) et avec la première électrode de courant dudit cinquième transistor (24).

7. Circuit de source de courant selon la revendication 6, dans lequel ledit dispositif de courant de polarisation (14) comporte:

un neuvième transistor (27) dudit premier type de conductivité ayant une première électrode de courant couplée avec ladite première borne de



tension d'alimentation (V_{DD}) et une électrode de commande couplée avec sa seconde électrode de courant et la première électrode de courant dudit huitième transistor (26) pour produire une tension de sortie proportionnelle audit courant de polarisation de sortie, et

un dixième transistor (28) dudit second type de conductivité ayant une première électrode de courant couplée avec la seconde électrode de courant dudit huitième transistor (26), une électrode de commande couplée avec les électrodes de commande dudit cinquième (24) et dudit sixième (23) transistors et avec la première électrode de courant dudit sixième transistor (23) et une seconde électrode de courant couplée avec ladite seconde tension d'alimentation (V_{SS}).

8. Circuit de source de courant selon la revendication 7, dans lequel au moins l'un dudit cinquième (24), dudit sixième (23), dudit septième (27), dudit huitième (26) et dudit dixième (28) transistors comporte sa seconde électrode de courant connectée à son substrat, réduisant ainsi sa tension seuil.

9. Circuit de source de courant delta V_{BE} comportant:

un dispositif de tension de référence (11) comprenant un premier transistor bipolaire (17) connecté en diode pour produire une tension de référence proportionnelle à un courant de polarisation,

un dispositif de courant de référence (12) couplé avec le dispositif de tension de référence (11), comprenant un second transistor bipolaire (18) couplé en série avec une résistance (19) pour produire un courant de référence proportionnel au rapport entre la différence des tensions base-émetteur, delta V_{BE} dudit premier (17) et dudit second (18) transistors bipolaires et proportionnelle à la valeur de ladite résistance (19),

un dispositif amplificateur à gain unitaire (13) ayant une impédance de sortie prédéterminée couplée avec ladite tension de référence (11) et ledit dispositif de courant de référence (12) pour produire une tension de polarisation proportionnelle audit courant de référence,

un dispositif de courant de polarisation (14) couplé avec ledit dispositif amplificateur (13) pour produire un courant de polarisation de sortie proportionnel à ladite tension de polarisation, et

un dispositif de tampon (15) couplé avec ledit dispositif amplificateur (13) et avec ledit dispositif de courant de polarisation (14) pour augmenter substantiellement l'impédance de sortie dudit dispositif amplificateur (13), en diminuant ainsi la dépendance aux variations d'alimentation.

10. Source de courant delta V_{BE} selon la revendication 9, dans lequel ledit dispositif amplificateur (13) comporte:

un troisième transistor (21) d'un premier type de conductivité ayant une première électrode de courant couplée avec le premier transistor bipolaire (17) et une électrode de commande couplée avec sa seconde électrode de courant et avec ledit dispositif amplificateur,

un quatrième transistor (22) dudit premier type de conductivité ayant une première électrode de courant couplée avec ladite résistance (19), une électrode de commande couplée avec l'électrode de commande dudit troisième transistor (21) et une seconde électrode de courant couplée avec ledit dispositif amplificateur,

un cinquième transistor (24) d'un second type de conductivité ayant une première électrode de courant couplée avec la seconde électrode de courant dudit quatrième transistor (22), une seconde électrode de courant couplée avec une borne de tension d'alimentation pour recevoir une tension d'alimentation (V_{SS}) et une électrode de commande couplée avec ledit dispositif de tampon (15) et ledit dispositif de courant de polarisation (14), et

un sixième transistor (23) dudit second type de conductivité ayant une première électrode de courant couplée avec son électrode de commande et avec l'électrode de commande dudit cinquième transistor (24) et une seconde électrode de courant couplée avec ladite borne de tension d'alimentation (V_{SS}).

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