CLAIMS

1. An integrated circuit device, comprising:

a p-type metal oxide semiconductor (PMOS) transistor having a body and source/drain regions supported by a backside of an isolation layer;

an n-type metal oxide semiconductor (NMOS) transistor having a body and source/drain regions supported by a front-side of the isolation layer, opposite the backside, in which the body and source/drain regions of the NMOS transistor are separated from the body and the source/drain regions of the PMOS transistor by the isolation layer; and

a shared contact extending through the isolation layer and electrically coupling a first terminal of the PMOS transistor to a first terminal of the NMOS transistor, the shared contact comprising:

a first shared front-to-backside contact extending through the isolation layer and electrically coupling a gate of the PMOS transistor to a gate of the NMOS transistor, and

a second shared front-to-backside contact extending through the isolation layer and electrically coupling the first terminal of the PMOS transistor to the first terminal of the NMOS transistor.

2. The integrated circuit device of claim 1, further comprising:

a power supply rail (Vdd) coupled to a second terminal of the PMOS transistor; and

a ground rail (Vss) coupled to the second terminal of the NMOS transistor, in which the integrated circuit device comprises an inverter gate, having the first shared front-to-backside contact as an input and the second shared contact as an output.

3. The integrated circuit device of claim 1, in which the PMOS transistor and the NMOS transistor comprise fin-type field effect transistors (FinFETs), in which a front-side fin of the NMOS transistor is offset from a backside fin of the PMOS transistor, and the first shared front-to-backside contact touches a sidewall spacer of the PMOS transistor and a sidewall spacer of the NMOS transistor.

4. The integrated circuit device of claim 1, in which the NMOS transistor and the PMOS transistor comprise gate-all-around nanowires, nanowires, or vertical transistors.

5. The integrated circuit device of claim 1, in which the PMOS transistor and the NMOS transistor comprise planar transistors, in which a gate of the PMOS transistor is offset from the gate of the NMOS transistor according to a staggered arrangement.

6. The integrated circuit device of claim 1, integrated into a radio frequency (RF) front end module, the RF front end module incorporated into at least one of a music player, a video player, an entertainment unit, a navigation device, a communications device, a personal digital assistant (PDA), a fixed location data unit, a mobile phone, and a portable computer.

7. An integrated circuit device, comprising:

a pair of first polarity transistors having body and source/drain regions on a front-side of an isolation layer, the pair of first polarity transistors electrically coupled in parallel;

a pair of second polarity transistors having body and source/drain regions on a backside of the isolation layer, opposite the front-side, the pair of second polarity transistors electrically coupled in series, in which the body and source/drain regions of the pair of first polarity transistors are separated from the body and source/drain regions of the pair of second polarity transistors by the isolation layer;

a first shared contact coupled to a gate of the first transistor of the pair of first polarity transistors and a gate of the first transistor of the pair of second polarity transistors;

a second shared contact coupled to a gate of the second transistor of the pair of first polarity transistors and a gate of the second transistor of the pair of second polarity transistors;

a first voltage contact coupled to a first terminal of each of the pair of first polarity transistors;

a second voltage contact coupled to a first terminal of one of the pair of second polarity transistors; and

an output contact coupled to a second terminal of the other pair of second polarity transistors and also coupled to a second terminal of both of the pair of first polarity transistors.

8. The integrated circuit device of claim 7, in which the integrated circuit device comprises a dual-sided negative AND (NAND) logic gate, the pair of first polarity transistors comprise p-type metal oxide semiconductor (PMOS) transistors, the pair of second polarity transistors comprise n-type metal oxide semiconductor (NMOS) transistors, the first voltage

contact comprises a power supply rail (Vdd), and the second voltage contact comprises a ground rail (Vss).

9. The integrated circuit device of claim 7, in which the integrated circuit device comprises a dual-sided, negative OR (NOR) logic gate, the pair of first polarity transistors comprise n-type metal oxide semiconductor (NMOS) transistors, the first voltage contact comprises a ground rail (Vss), and the second voltage contact comprises a power supply rail (Vdd).

10. The integrated circuit device of claim 7, in which the pair of first polarity transistors and the pair of second polarity transistors comprise fin-type field effect transistors (FinFETs) and the first shared contact touches a sidewall spacer of the first transistor of the pair of first polarity transistors and a sidewall spacer of the first transistor of the pair of second polarity transistors.

11. The integrated circuit device of claim 7, in which the pair of first polarity transistors and the pair of second polarity transistors comprise gate-all-around nanowires, nanowires, or vertical transistors.

12. The integrated circuit device of claim 7, in which the pair of first polarity transistors and the pair of second polarity transistors comprise planar transistors.

13. The integrated circuit device of claim 7, further comprising a radio frequency (RF) front end module, the RF front end module incorporated into at least one of a music player, a video player, an entertainment unit, a navigation device, a communications device, a personal digital assistant (PDA), a fixed location data unit, a mobile phone, and a portable computer.

14. A radio frequency (RF) front end module, comprising:

an integrated RF circuit structure, comprising a p-type metal oxide semiconductor (PMOS) transistor having a body and source/drain regions supported by a backside of an isolation layer, an n-type metal oxide semiconductor (NMOS) transistor having a body and source/drain regions supported by a front-side of the isolation layer, in which the body and source/drain regions of the NMOS transistor are separated from the body and source/drain regions of the PMOS transistor by the isolation layer, and a shared contact extending through the

isolation layer and electrically coupling a first terminal of the PMOS transistor to a first terminal of the NMOS transistor, the shared contact comprising:

a first shared front-to-backside contact extending through the isolation layer and electrically coupling a gate of the PMOS transistor to a gate of the NMOS transistor, and

a second shared front-to-backside contact extending through the isolation layer and electrically coupling the first terminal of the PMOS transistor to the first terminal of the NMOS transistor; and

an antenna coupled to an output of the integrated RF circuit structure.

15. The RF front end module of claim 14, further comprising:

a power supply rail (Vdd) coupled to a second terminal of the PMOS transistor; and

a ground rail (Vss) coupled to the second terminal of the NMOS transistor, in which the integrated RF circuit structure comprises an inverter gate, having the first shared front-to-backside contact as an input and the second shared contact as the output.

16. The RF front end module of claim 14, incorporated into at least one of a music player, a video player, an entertainment unit, a navigation device, a communications device, a personal digital assistant (PDA), a fixed location data unit, a mobile phone, and a portable computer.