CLAIMS

What is claimed is:

1. A method of manufacturing a semiconductor chip comprising:

placing a plurality of die units face up on an encapsulant layer, each die unit having an active front surface and a back surface opposing the active front surface, the active front surface and the back surface joined by at least four side surfaces;

encapsulating the plurality of die units on the active front surface of the encapsulant layer with an encapsulant covering a active front surface and four side surfaces of each of the plurality of die units; and

exposing, through the encapsulant covering on the active front surface, at least one conductive interconnect electrically coupled to a die bond pad.

2. The method of claim 1, wherein the encapsulant layer is a polymer layer.

3. The method of claim 2, wherein the polymer layer is a dielectric film.

4. The method of claim 3, wherein the dielectric film is an epoxy film positioned between the die units and a carrier.

5. The method of claim 4, wherein applying the epoxy film comprises applying the epoxy film having substantially a same thickness as a thickness of the encapsulant covering the active surface after the conductive interconnect is exposed.

6. The method of claim 1, wherein the conductive interconnect is a plated copper post.

7. The method of claim 6, wherein the copper posts are plated over die bond pads on the active surface of the die units.

8. The method of claim 1, wherein encapsulating the plurality of die units further comprises encapsulating through a compression molding process.

9. The method of claim 1, wherein encapsulating the plurality of die units further comprises encapsulating through a lamination process.

10. The method of claim 1, further comprising applying a fan-in redistribution layer to a native device wafer before encapsulating the plurality of die units.

11. The method of claim 10, wherein the conductive interconnect is a plurality of copper posts plated over redistribution layer traces.

12. The method of claim 1, further comprising curing the encapsulant layer.

13. The method of claim 1, wherein the conductive interconnect further electrically couples to a fan-out redistribution layer.

14. The method of claim 1, further comprising applying a dielectric film to a back surface of at least one of the die units.

15. The method of claim 1, wherein the conductive interconnect has a height of at least about 20 microns.

16. The method of claim 1, wherein exposing the at least one conductive interconnect comprises adjusting a thickness of the encapsulant covering the active front surface of the die units by removing encapsulant until the thickness of the encapsulant covering the active front surface is between a ratio of 5:1 and 1:5 compared with a thickness of encapsulant on a back surface of the die units.

17. A wafer level package comprising:

a die unit having an active surface and a back surface opposing the active surface, the active surface and back surface joined by four side surfaces, the back surface in contact with an encapsulant layer;

an encapsulant that encapsulates the die unit and covers the active surface and four side surfaces of the die unit; and

a plurality of conductive interconnects electrically connecting a plurality of die bond pads on the active surface to a first redistribution layer.

18. The wafer level package of claim 17, wherein the first redistribution layer is a fan-out redistribution layer.

19. The wafer level package of claim 17, wherein the conductive interconnects are plated over traces of the redistribution layer.

20. The wafer level package of claim 17, wherein the conductive interconnects are plated over die bond pads on the active surface of the die unit.

21. The wafer level package of claim 17, wherein the encapsulant layer is a polymer layer.

22. The wafer level package of claim 21, wherein the polymer layer is dielectric film.

23. The wafer level package of claim 22, wherein the dielectric film is a compliant epoxy film applied after encapsulation.

24. The wafer level package of claim 17, wherein a thickness of the encapsulant covering the active surface is substantially a same thickness as a thickness of the encapsulant layer covering the back surface.

25. The wafer level package of claim 17, wherein a thickness of the encapsulant covering the active surface has a ratio of between approximately 1/5 and 5 in relation to a thickness of the encapsulant layer covering the back surface.

26. The wafer level package of claim 17, wherein the conductive interconnects have a height of at least about 20 microns.

CLAIMS

1. A method of making a semiconductor package, comprising:

placing a plurality of die units face up on a carrier, each die unit having an active front surface comprising at least one bond pad oriented away from the carrier and a back surface opposing the active front surface, the active front surface and the back surface joined by at least four side surfaces;

forming a plurality of conductive interconnects, each conductive interconnect coupled to the at least one bond pad of one of the plurality of die units;

encapsulating the plurality of die units and the plurality of conductive interconnects with an encapsulant that covers the active front surface and the at least four side surfaces of each of the plurality of die units;

exposing a first surface of each of the plurality of conductive interconnects by removal of a portion of the encapsulant; and

forming a redistribution layer (RDL) disposed over, and in direct contact with, the encapsulant.

2. The method of making the semiconductor package of claim 1, further comprising encapsulating the plurality of die units and the plurality of conductive interconnects in a single step.

3. The method of making the semiconductor package of claim 1, further comprising exposing the first surface of each of the plurality of conductive interconnects, wherein exposing the first surface of each of the plurality of interconnects comprises leaving at least a portion of the encapsulant disposed over the active front surface of each of the plurality of die units.

4. The method of making the semiconductor package of claim 1, further comprising forming the encapsulant as a polymer layer or dielectric film positioned between the plurality of die units and the carrier, the polymer layer or dielectric film being permanently attached to the plurality of die units.

5. The method of making the semiconductor package of claim 1, further comprising disposing a dielectric film over the back surface of the plurality of die units comprising a thickness between a ratio of 5:1 and 1:5 compared with a thickness of the encapsulant covering the active front surface.

6. The method of making the semiconductor package of claim 1, further comprising encapsulating the plurality of die units with a compression molding process or lamination process.

7. The method of making the semiconductor package of claim 1, further comprising forming the

plurality of conductive interconnects as plated posts.

8. The method of making the semiconductor package of claim 1, further comprising coupling the plurality of conductive interconnects to fan-in redistribution layers disposed between each of the plurality of die units and the conductive interconnects.

9. A method of making a semiconductor package, comprising:

providing a first die unit comprising an active front surface comprising a bond pad that is opposite a back surface, the active front surface and the back surface joined by at least four side surfaces;

forming a fan-in redistribution layer (RDL) over the active front surface and coupled to the bond pad;

forming a conductive interconnect coupled to the fan-in RDL and the bond pad of the active front surface;

disposing the first die unit over a carrier with the active front surface oriented away from the carrier; and

encapsulating the first die unit and the conductive interconnect with an encapsulant that covers the active front surface and the at least four side surfaces of the first die unit.

10. The method of making the semiconductor package of claim 9, further comprising encapsulating the first die unit and the conductive interconnect with the encapsulant in a single step.

11. The method of making the semiconductor package of claim 9, further comprising exposing the conductive interconnect through removing a portion of the encapsulant.

12. The method of making the semiconductor package of claim 9, further comprising encapsulating the first die unit and the conductive interconnect before removing the carrier.

13. The method of making the semiconductor package of claim 9, wherein the conductive interconnect has a height of at least about 20 microns.

14. The method of making the semiconductor package of claim 9, further comprising forming a second redistribution layer in direct contact with the encapsulant and disposed over the first die unit.

15. The method of making the semiconductor package of claim 9, further including forming the

conductive interconnect as a copper post plated over the active front surface of the first die unit.

16. The method of making the semiconductor package of claim 9, further comprising a second die unit disposed within the semiconductor package.

17. A semiconductor package comprising:

a first die unit having an active surface comprising a plurality of bond pads and a back surface opposing the active surface, the active surface and back surface joined by at least four side surfaces;

a plurality of conductive posts coupled to the plurality of die bond pads;

a first encapsulant that covers the active surface, the plurality of conductive posts, and the at least four side surfaces of the first die unit; and

a first redistribution layer coupled to ends of the plurality of conductive posts.

18. The semiconductor package of claim 17, further comprising a second encapsulant disposed over the back surface of the first die unit, wherein the second encapsulant comprises a footprint that is substantially equal to a footprint of the first die unit and further comprises a surface that is coplanar with a surface of the first encapsulant.

19. The semiconductor package of claim 18, wherein the first redistribution layer is a fan-out redistribution layer formed over the first encapsulant.

20. The semiconductor package of claim 19, further comprising a second redistribution layer formed over the active surface of the first die unit, wherein the conductive posts are plated over the second redistribution layer.

21. The semiconductor package of claim 18, wherein the conductive posts are plated over the plurality of die bond pads on the active surface of the first die unit.

22. The semiconductor package of claim 18, further including a polymer layer or dielectric film disposed over the active surface.

23. The semiconductor package of claim 22, wherein the first redistribution layer is a fan-in redistribution layer formed over the polymer layer or dielectric film.

24. The semiconductor package of claim 18, further comprising a second die unit disposed within

the semiconductor package.

25. The semiconductor package of claim 24, wherein a thickness of the first encapsulant covering the active surface has a ratio of between approximately 1/5 and 5 in relation to a thickness of the second encapsulant covering the back surface.

26. The semiconductor package of claim 18, wherein the conductive posts have a height of at least about 20 microns.

27. The semiconductor package of claim 18, wherein the first encapsulant or the second encapsulant comprise an epoxy film.

28. The semiconductor package of claim 23, further comprising a second redistribution layer formed as a fan-out redistribution layer.