CLAIMS

What is claimed is:

1. A nanowire transistor, comprising:

at least one nanowire channel having a first end, and an opposing second end;

a source structure proximate the at least one nanowire first end, wherein a first underlayer etch stop structure is disposed between the source structure and the at least one nanowire first end; and

a drain structures proximate the at least one nanowire second end, wherein a second underlayer etch stop structure is disposed between the drain structure and the at least one nanowire second end.

2. The nanowire transistor of claim 1, further including a gate dielectric material abutting the nanowire channel between the nanowire channel first end and the nanowire channel second end.

3. The nanowire transistor of claim 2, further including a gate electrode material abutting the gate dielectric material.

4. The nanowire transistor of claim 3, wherein the gate electrode material abuts the first underlayer etch stop structure and the second underlayer etch stop structure.

5. The nanowire transistor of any one of claims 1 to 4, wherein the nanowire channel, the first underlayer etch stop structure, and the second underlayer etch stop structure are the same material.

6. The nanowire transistor of any one of claims 1 to 4, wherein the nanowire channel, the first underlayer etch stop structure, and the second underlayer etch stop structure are silicon germanium.

7. The nanowire transistor of any one of claims 1 to 4, wherein the nanowire channel, the first underlayer etch stop structure, and the second underlayer etch stop structure are silicon.

8. The nanowire transistor of claim 1, wherein the at least one nanowire channel comprises a plurality of nanowires channels formed above a microelectronic substrate, wherein the nanowire channels are spaced apart from one another.

9. A method of forming a microelectronic structure, comprising:

forming a fin structure on a microelectronic substrate, wherein the fin structure comprises at least one sacrificial material layer alternating with at least one channel material layer;

forming at least two spacers across the fin structure;

forming a sacrificial gate electrode material between the at least two spacers;

removing a portion fin structure external to the sacrificial gate electrode material and the spacers to form a fin structure first end and an opposing fin structure second end;

forming underlayer etch stop structures to abut the fin structure first end and the fin structure second end; and

forming a source structure and a drain structure to abut the underlayer etch stop structures on opposing ends of the fin structure.

10. The method of claim 9, further including:

forming an interlayer dielectric layer over the source structure and the drain structure;

removing the sacrificial gate electrode material from between the spacers;

and selectively removing the sacrificial material layers between the channel material layers to form the at least one channel nanowire.

11. The method of claim 10, further including:

forming a gate dielectric material to surround the channel nanowire between the spacers; and

forming a gate electrode material on the gate dielectric material.

12. The method of claim 9, wherein forming the fin structure on the microelectronic substrate, wherein the fin structure comprises at least one sacrificial material layer alternating with at least one channel material layer, comprises:

forming a microelectronic substrate;

forming a stacked layer comprising at least one sacrificial material layer alternating with at least one channel material layer; and

forming at least one fin structure from the layered stack.

13. The method of any one of claims 9 to 12, wherein the channel material layer, the first underlayer etch stop structure, and the second underlayer etch stop structure are the same material.

14. The method of any one of claims 9 to 12, wherein the channel material layer, the first underlayer etch stop structure, and the second underlayer etch stop structure are silicon germanium.

15. The method of any one of claims 9 to 12, wherein the channel material layer, the first underlayer etch stop structure, and the second underlayer etch stop structure are silicon.

16. A computing device, comprising:

a board including at least one component;

wherein the at least one component includes at least one microelectronic structure comprising at least one nanowire transistor including at least one nanowire channel having a first end, and an opposing second end; a source structure proximate the at least one nanowire first end, wherein a first underlayer etch stop structure is disposed between the source structure and the at least one nanowire first end; and a drain structures proximate the at least one nanowire second end, wherein a second underlayer etch stop structure is disposed between the drain structure and the at least one nanowire second end.

17. The computing device of claim 16, further including a gate dielectric material abutting the nanowire channel between the nanowire channel first end and the nanowire channel second end.

18. The computing device of claim 17, further including a gate electrode material abutting the gate dielectric material.

19. The computing device of claim 18, wherein the gate electrode material abuts the first underlayer etch stop structure and the second underlayer etch stop structure.

20. The computing device of any one of claims 16 to 19, wherein the nanowire channel, the first underlayer etch stop structure, and the second underlayer etch stop structure are the same material.

21. The computing device of any one of claims 16 to 19, wherein the nanowire channel, the first underlayer etch stop structure, and the second underlayer etch stop structure are silicon germanium.

22. The computing device of any one of claims 16 to 19, wherein the nanowire channel, the first underlayer etch stop structure, and the second underlayer etch stop structure are silicon.

23. The computing device of claim 16, wherein the at least one nanowire channel comprises a plurality of nanowires channels formed above a microelectronic substrate, wherein the nanowire channels are spaced apart from one another.

CLAIMS

What is claimed is:

1. A nanowire transistor, comprising:

at least one nanowire channel having a first end, and an opposing second end;

a source structure proximate the at least one nanowire first end, wherein a first underlayer etch stop structure is disposed between the source structure and the at least one nanowire first end; and

a drain structures proximate the at least one nanowire second end, wherein a second underlayer etch stop structure is disposed between the drain structure and the at least one nanowire second end.

2. The nanowire transistor of claim 1, further including a gate dielectric material abutting the nanowire channel between the nanowire channel first end and the nanowire channel second end.

3. The nanowire transistor of claim 2, further including a gate electrode material abutting the gate dielectric material.

4. The nanowire transistor of claim 3, wherein the gate electrode material abuts the first underlayer etch stop structure and the second underlayer etch stop structure.

5. The nanowire transistor of claim 1, wherein the nanowire channel, the first underlayer etch stop structure, and the second underlayer etch stop structure are the same material.

6. The nanowire transistor of claim 5, wherein the nanowire channel, the first underlayer etch stop structure, and the second underlayer etch stop structure are silicon germanium.

7. The nanowire transistor of claim 5, wherein the nanowire channel, the first underlayer etch stop structure, and the second underlayer etch stop structure are silicon.

8. The nanowire transistor of claim 1, wherein the at least one nanowire channel comprises a plurality of nanowires channels formed above a microelectronic substrate, wherein the nanowire channels are spaced apart from one another.

9. A method of forming a microelectronic structure, comprising:

forming a fin structure on a microelectronic substrate, wherein the fin structure comprises at least one sacrificial material layer alternating with at least one channel material layer;

forming at least two spacers across the fin structure;

forming a sacrificial gate electrode material between the at least two spacers;

removing a portion fin structure external to the sacrificial gate electrode material and the spacers to form a fin structure first end and an opposing fin structure second end;

forming underlayer etch stop structures to abut the fin structure first end and the fin structure second end; and

forming a source structure and a drain structure to abut the underlayer etch stop structures on opposing ends of the fin structure.

10. The method of claim 9, further including:

forming an interlayer dielectric layer over the source structure and the drain structure;

removing the sacrificial gate electrode material from between the spacers;

and selectively removing the sacrificial material layers between the channel material layers to form the at least one channel nanowire.

11. The method of claim 10, further including:

forming a gate dielectric material to surround the channel nanowire between the spacers; and

forming a gate electrode material on the gate dielectric material.

12. The method of claim 9, wherein forming the fin structure on the microelectronic substrate, wherein the fin structure comprises at least one sacrificial material layer alternating with at least one channel material layer, comprises:

forming a microelectronic substrate;

forming a stacked layer comprising at least one sacrificial material layer alternating with at least one channel material layer; and

forming at least one fin structure from the layered stack.

13. The method of claim 9, wherein the channel material layer, the first underlayer etch stop structure, and the second underlayer etch stop structure are the same material.

14. The method of claim 13, wherein the channel material layer, the first underlayer etch stop structure, and the second underlayer etch stop structure are silicon germanium.

15. The method of claim 13, wherein the channel material layer, the first underlayer etch stop structure, and the second underlayer etch stop structure are silicon.

16. A computing device, comprising:

a board including at least one component;

wherein the at least one component includes at least one microelectronic structure comprising at least one nanowire transistor including at least one nanowire channel having a first end, and an opposing second end; a source structure proximate the at least one nanowire first end, wherein a first underlayer etch stop structure is disposed between the source structure and the at least one nanowire first end; and a drain structures proximate the at least one nanowire second end, wherein a second underlayer etch stop structure is disposed between the drain structure and the at least one nanowire second end.

17. The computing device of claim 16, further including a gate dielectric material abutting the nanowire channel between the nanowire channel first end and the nanowire channel second end.

18. The computing device of claim 17, further including a gate electrode material abutting the gate dielectric material.

19. The computing device of claim 18, wherein the gate electrode material abuts the first underlayer etch stop structure and the second underlayer etch stop structure.

20. The computing device of claim 16, wherein the nanowire channel, the first underlayer etch stop structure, and the second underlayer etch stop structure are the same material.

21. The computing device of claim 20, wherein the nanowire channel, the first underlayer etch stop structure, and the second underlayer etch stop structure are silicon germanium.

22. The computing device of claim 20, wherein the nanowire channel, the first underlayer etch stop structure, and the second underlayer etch stop structure are silicon.

23. The computing device of claim 16, wherein the at least one nanowire channel comprises a plurality of nanowires channels formed above a microelectronic substrate, wherein the nanowire channels are spaced apart from one another.