METHODS FOR ISOLATING PORTIONS OF A LOOP OF PITCH-MULTIPLIED MATERIAL AND RELATED STRUCTURES

Reference to Related Applications

[0001] This application is related to and incorporates the following by reference in their entireties: U.S. Patent Application No. 10/934,778 to Abatchev *et al.*, filed September 2, 2004 (Attorney Docket No. MICRON.294A); U.S. Patent Application No. 10/931,771 to Tran *et al.*, filed August 31, 2004 (Attorney Docket No. MICRON.295A); U.S. Patent Application No. 11/216,477 to Tran *et al.*, filed August 31, 2005 (Attorney Docket No. MICRON.314A); and U.S. Patent Application No. 11/214,544 to Tran *et al.*, filed August 29, 2005 (Attorney Docket No. MICRON.316A).

Background of the Invention

Field of the Invention

[0002] This invention relates generally to the fabrication of integrated circuits and electronic devices and, more particularly, to fabrication methods and related structures.

Description of the Related Art

[0003] As a consequence of many factors, including demand for increased portability, computing power, memory capacity and energy efficiency, integrated circuits are constantly being reduced in size. The sizes of the constituent features that form the integrated circuits, *e.g.*, electrical devices and interconnect lines, are also constantly being decreased to facilitate this size reduction.

[0004] The trend of decreasing feature size is evident, for example, in memory circuits or devices such as dynamic random access memories (DRAMs), flash memory, static random access memories (SRAMs), ferroelectric (FE) memories, etc. To take one example, DRAM typically includes millions or billions of identical circuit elements, known as memory cells. A memory cell typically consists of two electrical devices: a storage capacitor and an access field effect transistor. Each memory cell is an addressable location that may store one

bit (binary digit) of data. A bit may be written to a cell through the transistor and may be read by sensing charge in the capacitor.

[0005] In another example, flash memory typically includes billions of flash memory cells containing floating gate field effect transistors that can retain a charge. The presence or absence of a charge in the floating gate determines the logic state of the memory cell. A bit may be written to a cell by injecting charge to or removing charge from a cell. Flash memory cells may be connected in different architecture configurations, each with different schemes for reading bits. In a "NOR" architecture configuration, each memory cell is coupled to a bit line and may be read individually. In a "NAND" architecture configuration, memory cells are aligned in a "string" of cells, and an entire bit line is activated to access data in one of the string of cells.

[0006] In general, by decreasing the sizes of the electrical devices that constitute a memory cell and the sizes of the conducting lines that access the memory cells, the memory devices may be made smaller. Additionally, storage capacities may be increased by fitting more memory cells on a given area in the memory devices.

[0007] The concept of pitch may be used to describe one aspect of the sizes of features in an integrated circuit such as a memory device. Pitch is defined as the distance between identical points in two neighboring features, such as features in an array, which are typically arranged in a repeating pattern. These features are typically defined by spaces between adjacent features, which spaces are typically filled by a material, such as an insulator. As a result, pitch may be viewed as the sum of the width of a feature and of the width of the space on one side of the feature separating that feature from a neighboring feature. It will be appreciated that the spaces and features, such as lines, typically repeat to form a repetitive pattern of spacers and features.

[0008] Critical dimension (CD) is another term used to describe the sizes of features. The critical dimension is the smallest dimension of a feature in a particular circuit or masking scheme. Controlling the CD of certain structures, such as shallow trench isolation (STI) structures, during integrated circuit fabrication helps to facilitate the continued size reduction of integrated circuits by, *e.g.*, ensuring predictable circuit performance.

[0009] The continual reduction in feature sizes places ever greater demands on the techniques used to form the features. For example, photolithography is commonly used to pattern features, such as conductive lines, in integrated circuit fabrication. However, due to factors such as optics, light or radiation wavelength and available photoresist materials, photolithography techniques may each have a minimum pitch or critical dimension below which a particular photolithographic technique cannot reliably form features. Thus, the inherent limitations of photolithographic techniques are obstacles to continued feature size reduction.

[0010] "Pitch doubling" or "pitch multiplication" is one proposed method for extending the capabilities of photolithographic techniques beyond their minimum pitch. A pitch multiplication method is illustrated in Figures 1A-1F and described in U.S. Patent No. 5,328,810, issued to Lowrey *et al.*, the entire disclosure of which is incorporated herein by reference. With reference to Figure 1A, a pattern of lines 10 is photolithographically formed in a photoresist layer, which overlies a layer 20 of an expendable material, which in turn overlies a substrate 30. As shown in Figure 1B, the pattern in the photoresist layer is transferred to the layer 20, thereby forming placeholders, or mandrels, 40. The photoresist lines 10 are stripped and the mandrels 40 are etched to increase the distance between neighboring mandrels 40, as shown in Figure 1C. A layer 50 of spacer material is subsequently deposited over the mandrels 40, as shown in Figure 1D. Spacers 60 are then formed on the sides of the mandrels 40. The spacer formation is accomplished by preferentially etching the spacer material from the horizontal surfaces 70 and 80, as shown in Figure 1E. The remaining mandrels 40 are then removed, leaving behind only the spacers 60, which together act as a mask for patterning, as shown in Figure 1F. Thus, where a given pitch previously included a pattern defining one feature and one space, the same width now includes two features and two spaces, with the spaces defined by the spacers 60.

[0011] While the pitch is actually halved in the example above, this reduction in pitch is conventionally referred to as pitch "doubling," or, more generally, pitch "multiplication." Thus, conventionally, "multiplication" of pitch by a certain factor actually involves reducing the pitch by that factor. The conventional terminology is retained herein.

[0012] While allowing for smaller critical dimensions and pitch, pitch multiplication faces continuing development as new challenges emerge, as the requirements of integrated circuit fabrication change. Accordingly, there is a constant need for methods and structures for forming small features.

Brief Description of the Drawings

[0013] Figures 1A-1F are schematic, cross-sectional side views of a sequence of masking patterns for forming conductive lines, in accordance with a prior art pitch doubling method.

[0014] Figure 2 is a schematic top plan view of a partially formed integrated circuit, in accordance with embodiments of the invention.

[0015] Figures 3A and 3B are schematic cross-sectional side and top plan views of the partially formed integrated circuit of Figure 2, in accordance with embodiments of the invention.

[0016] Figures 4A and 4B are schematic cross-sectional side and top plan views of the partially formed integrated circuit of Figures 3A and 3B after forming lines in a photoresist layer in an array region of the integrated circuit, in accordance with embodiments of the invention.

[0017] Figures 5A and 5B are schematic cross-sectional side and top plan views of the partially formed integrated circuit of Figures 4A and 4B after widening spaces between lines in the photoresist layer, in accordance with embodiments of the invention.

[0018] Figure 6 is a schematic, cross-sectional side view of the partially formed integrated circuit of Figures 5A and 5B after depositing a layer of a spacer material, in accordance with embodiments of the invention.

[0019] Figures 7A and 7B are schematic, cross-sectional side and top plan views of the partially formed integrated circuit of Figure 6 after a spacer etch, in accordance with embodiments of the invention.

[0020] Figures 8A and 8B are schematic, cross-sectional side and top plan views of the partially formed integrated circuit of Figures 7A and 7B after removing a remaining

portion of the temporary layer to leave a pattern of spacers in the array region of the integrated circuit, in accordance with embodiments of the invention.

[0021] Figures 9A and 9B are schematic, cross-sectional side and top plan views of the partially formed integrated circuit of Figures 8A and 8B after depositing photoresist between and over the spacers, in accordance with embodiments of the invention.

[0022] Figures 10A and 10B are schematic, cross-sectional side and top plan views of the partially formed integrated circuit of Figures 9A and 9B after forming a pattern in the photoresist, in accordance with embodiments of the invention.

[0023] Figure 11 is a schematic, cross-sectional side view of the partially formed integrated circuit of Figures 10A and 10B after transferring a combined pattern defined by the patterned photoresist and the spacers to an underlying hard mask layer, in accordance with embodiments of the invention.

[0024] Figure 12 is a schematic, cross-sectional side view of the partially formed integrated circuit of Figure 11 after transferring the combined pattern to a primary mask layer, in accordance with embodiments of the invention.

[0025] Figure 13 is a schematic, cross-sectional side view of the partially formed integrated circuit of Figure 12 after transferring the combined pattern to the underlying substrate, in accordance with embodiments of the invention.

[0026] Figures 14A and 14B are schematic, cross-sectional side and top views of the partially formed integrated circuit of Figure 13 after transferring the pattern into the substrate and removing hard mask layers overlying the substrate, in accordance with embodiments of the invention.

[0027] Figure 15 is a schematic, cross-sectional side view of the partially formed integrated circuit of Figures 14A and 14B after filling trenches with a dielectric and forming a sequence of layers corresponding to a gate stack, in accordance with embodiments of the invention.

[0028] Figures 16A, 16B and 16C are schematic, cross-sectional side and top plan views of the partially formed integrated circuit of Figure 15 after depositing and patterning a photoresist layer, in accordance with embodiments of the invention.

[0029] Figures 17A and 17B are schematic, cross-sectional side and top plan views of the partially formed integrated circuit of Figures 16A and 16B after transferring the pattern from the photoresist layer to the sequence of gate stack layers, in accordance with embodiments of the invention.

[0030] Figure 18 is a schematic diagram of a memory cell array of a NAND flash memory device, in accordance with embodiments of the invention.

[0031] Figure 19 is a system block diagram illustrating an electronic device including a memory device, in accordance with embodiments of the invention.

Detailed Description of the Some Embodiments

[0032] Pitch multiplication has the ability to form closely spaced lines by patterning those lines using a mask formed by spacers. Because the spacers are formed on sidewalls of mandrels, the spacers typically form a continuous loop. Using these continuous loops to pattern a substrate may form continuous loops of material in the substrate. However, separated lines are typically desired for use in various applications, such as bit lines or word lines in a memory device. Thus, to utilize the closely spaced pairs of lines patterned using a spacer loop, the ends of the loops are typically etched to physically, electrically disconnect different legs of the loops from each other. Methods and structures for such an etch (called a loop etch) are described in U.S. Patent No. 7,151,040, the entire disclosure of which is incorporated by reference herein.

[0033] For a loop etch, a protective material is typically deposited around and over the loops. The protective material is then patterned to expose the loop ends. The exposed loops are exposed to an etch and removed. The protective material is subsequently removed, leaving physically separated lines. Thus, loop end etching may involve deposition, patterning and material removal steps. It will be appreciated that the patterning step may involve performing photolithography and exposure of protective material to light through a mask. Due to the time needed to perform these steps and, possibly, the time needed to transport a substrate between processing equipment to perform these steps, the loop etch can undesirably add to the time and complexity involved in, *e.g.*, fabricating an integrated circuit using pitch multiplication.

[0034] Advantageously, in accordance with some embodiments of the invention, different legs of a semiconductor loop are electrically isolated without needing to perform a loop etch. Rather, isolation transistors are formed in the loops to electrically isolate the different legs from each other. A gate is formed over the loop of semiconductor material and the regions of the loop neighboring the gate are doped to form source and drain regions. The loop region directly below the gate functions as an active area. The gate is biased in the off state to prevent current flow through the active area, thereby electrically isolating from each other the parts of the loop that lie on either side of the gate. In some embodiments, an isolation transistor is formed at the ends of each leg of the loops, for a total of four such transistors per loop. The isolation transistors define two electrically isolated legs of semiconductor material between each pair of transistors.

[0035] In some embodiments, the loops of semiconductor material, *e.g.*, doped semiconductor material, are formed by a pitch multiplication process. Spacer loops are formed on a level over a substrate. A block of masking material is overlaid on a section of each of the loops, *e.g.*, a different block of masking material is overlaid on each end of the loops in embodiments where the loops are substantially parallel lines of material joined together at their ends. The pattern defined by the spacer loops and the blocks of masking material are transferred to a substrate, thereby forming lines of semiconductor material that terminate at and are contiguous with the blocks of the semiconductor material. A transistor gate is formed on each line of semiconductor material and adjacent each block of semiconductor material. The block of semiconductor material and the part of the line on a side of the gate opposite the block are doped to form source/drain regions. The blocks and the gate are electrically tied together and are biased in the off state to electrically isolate the lines of semiconductor material from the blocks. Thus, each line disposed between the blocks is electrically isolated from other lines without needing to perform a loop etch.

[0036] Advantageously, it will be appreciated that the steps for forming the isolation transistors are typically already part of a process flow for forming other transistors, *e.g.*, the isolation transistors can be formed using the same patterning, doping and deposition steps used to form floating gate transistors and select gates in a memory device. As a result, in many embodiments, the formation of the isolation transistors do not introduce any

additional steps to the process flow. Moreover, by obviating the loop etch, the process steps involved in the loop etch can be omitted. Thus, the process flow is simplified and process throughput is increased.

[0037] In addition, in some embodiments, lines may be formed having a pitch below the minimum pitch of the photolithographic method used to pattern the various photoresist layers illustrated herein. Advantageously, embodiments of the invention allow the formation of lines having a pitch of about 100 nm or less or about 50 nm or less.

[0038] Reference will now be made to the Figures, wherein like numerals refer to like parts throughout. It will be appreciated that these Figures are not necessarily drawn to scale. Moreover, it will be appreciated that only a limited number of features, including mask features and etched features such as bit lines, word lines, spacers, and memory blocks are illustrated for ease of discussion and illustration. Additional numbers of these features can be provided in some embodiments.

[0039] In a first phase of some embodiments of the invention, mask features are formed by pitch multiplication.

[0040] Figure 2 shows a top view of a portion of a partially fabricated integrated circuit 100. While the embodiments of the invention may be used to form any integrated circuit and may be applied to form masks for patterning various substrates, they may particularly advantageously be applied to form devices having arrays of electrical devices, including memory cell arrays for volatile and non-volatile memory devices such as DRAM, ROM or flash memory, including NAND or NOR flash memory, or integrated circuits having logic or gate arrays. For example, the logic array may be a field programmable gate array (FPGA) having a core array similar to a memory array and a periphery with supporting logics. Consequently, the integrated circuit 100 may be, *e.g.*, a memory chip or a processor, which may include both a logic array and embedded memory, or any other integrated circuit having a logic or a gate array.

[0041] With continued reference to Figure 2, a central region 102, the "array," is surrounded by a peripheral region 104, the "periphery." It will be appreciated that, in a fully formed integrated circuit, the array 102 will typically be densely populated with electrically conductive line and electrical devices, including transistors and/or capacitors. In a memory

device, the electrical devices form a plurality of memory cells, which may be arranged in a regular grid pattern at the intersection of word lines and bit lines. Desirably, pitch multiplication may be used to form features such as rows/columns of transistors and/or capacitors in the array 102, as discussed herein. On the other hand, the periphery 104 typically comprises features larger than those in the array 102. Conventional photolithography, rather than pitch multiplication, is preferably used to pattern features, such as logic circuitry, in the periphery 104, because the geometric complexity of logic circuits located in the periphery 104 makes using pitch multiplication difficult, whereas the regular grid typical of array patterns is conducive to pitch multiplication. In addition, some devices in the periphery require larger geometries due to electrical constraints, thereby making pitch multiplication less advantageous than conventional photolithography for such devices. In some cases, the periphery 104 may contain patterns/circuits defined by both conventional lithography and pitch multiplication. In addition to possible differences in relative scale, it will be appreciated by the skilled artisan that the relative positions, and the number of periphery 104 and array 102 regions in the partially fabricated integrated circuit 100 may vary from that depicted.

[0042] Figure 3A shows a cross-sectional side view of the partially formed integrated circuit 100. Various masking layers 120-140 are provided above a substrate 110. The layers 120-140 will be etched to form a mask for patterning the substrate 110, as discussed below. In the illustrated embodiment, a selectively definable layer 120 overlies a hard mask, or etch stop, layer 130, which overlies a primary mask layer 140, which overlies the substrate 110 to be processed (*e.g.*, etched) through a mask.

[0043] The materials for the layers 120-140 overlying the substrate 110 are chosen based upon consideration of the chemistry and process conditions for the various pattern forming and pattern transferring steps discussed herein. Because the layers between the topmost selectively definable layer 120 and the substrate 110 function to transfer a pattern derived from the selectively definable layer 120 to the substrate 110, the layers 130-140 between the selectively definable layer 120 and the substrate 110 are chosen so that they may be selectively etched relative to other exposed materials. It will be appreciated that a material is considered selectively, or preferentially, etched when the etch rate for that material is at least

about 2-3 times greater, at least about 10 times greater, at least about 20 times greater, or at least about 40 times greater than that for surrounding materials. Because a goal of the layers 120-130 overlying the primary hard mask layer 140 is to allow well-defined patterns to be formed in that layer 140, it will be appreciated that one or more of the layers 120-130 may be omitted or substituted if suitable other materials, chemistries and/or process conditions are used. For example, where the substrate is relatively simple and may be selectively etched relative to the hard mask layer 130, the primary hard mask layer 140 may be omitted and patterns may be transferred directly to the substrate using the hard mask layer 130.

[0044] With continued reference to Figure 3A, the selectively definable layer 120 is photodefinable, *e.g.*, formed of a photoresist, including any photoresist, including any positive or negative photoresist, known in the art. For example, the photoresist may be any photoresist compatible with 157 nm, 193 nm, 248 nm or 365 nm wavelength systems, 193 nm wavelength immersion systems, extreme ultraviolet systems (including 13.7 nm wavelength systems) or electron beam lithographic systems. In addition, maskless lithography, or maskless photolithography, may be used to define the selectively definable layer 120. Examples of photoresist materials include argon fluoride (ArF) sensitive photoresist, *i.e.*, photoresist suitable for use with an ArF light source, and krypton fluoride (KrF) sensitive photoresist, *i.e.*, photoresist suitable for use with a KrF light source. ArF photoresists are used with photolithography systems utilizing relatively short wavelength light, *e.g.*, 193 nm wavelength light. KrF photoresists are used with longer wavelength photolithography systems, such as 248 nm systems. In other embodiments, the layer 120 and any subsequent resist layers may be formed of a resist that may be patterned by nano-imprint lithography, *e.g.*, by using a mold or mechanical force to pattern the resist.

[0045] In some embodiments, the material for the hard mask layer 130 comprises an inorganic material. Materials for the hard mask layer 130 include silicon oxide (SiO_2), silicon or an anti-reflective coating (ARC), such as a silicon-rich silicon oxynitride, a silicon-rich nitride, or a film that has the desired etch selectivity relative to the spacers 175 or other exposed materials (Figure 7A). The hard mask layer 130 may also include combinations of layers of materials, *e.g.*, a bottom anti-reflective coating (BARC) over a dielectric anti-reflective coating (DARC). For ease of description, in the illustrated embodiment, the hard

mask layer 130 is an anti-reflective coating, such as DARC. It will be appreciated that using ARCs for the hard mask layer 130 may be particularly advantageous for forming patterns having pitches near the resolution limits of a photolithographic technique. The ARCs can enhance resolution by minimizing light reflections, thus increasing the precision with which photolithography can define the edges of a pattern.

[0046] With continued reference to Figure 3A, embodiments of the invention may utilize a primary masking layer to facilitate pattern transfer to a substrate. As noted above, in common methods of transferring patterns, both the mask and the underlying substrate are exposed to etchant, which may wear away a mask before the pattern transfer is complete. These difficulties are exacerbated where the substrate comprises multiple different materials to be etched. Due to its excellent etch selectivity relative to a variety of materials, including oxides, nitrides and silicon, the primary masking layer may be formed of amorphous carbon.

[0047] The amorphous carbon layer may be formed by chemical vapor deposition using a hydrocarbon compound, or mixtures of such compounds, as carbon precursors. Carbon precursors may include propylene, propyne, propane, butane, butylene, butadiene and acetelyne. A method for forming amorphous carbon layers is described in U.S. Patent No. 6,573,030 B1, issued to Fairbairn *et al.* on June 3, 2003, the entire disclosure of which is incorporated herein by reference. In some embodiments, the amorphous carbon is a form of amorphous carbon that is highly transparent to light and that offers further improvements for photo alignment by being transparent to the wavelengths of light used for such alignment. Deposition techniques for forming such transparent carbon can be found in A. Helmbold, D. Meissner, Thin Solid Films, 283 (1996) 196-203, the entire disclosure of which is incorporated herein by reference. In addition, the amorphous carbon may be doped. A suitable method for forming doped amorphous carbon is described in U.S. Patent Application No. 10/652,174 to Yin *et al.*, the entire disclosure of which is incorporated herein by reference.

[0048] It will be appreciated that the "substrate" to which patterns are transferred may include a layer of a single material, a plurality of layers of different materials, a layer or layers having regions of different materials or structures in them, etc. These materials may include semiconductors, insulators, conductors, or combinations thereof. In the illustrated

embodiment, the substrate is formed of doped semiconductor material, *e.g.*, semiconductor material containing p-type dopant.

[0049] With reference to Figures 4A and 4B, a pattern comprising spaces or trenches 122, which are delimited by photodefinable material features 124, is formed in the photodefinable layer 120. The trenches 122 may be formed by, *e.g.*, photolithography with 248 nm or 193 nm light, in which the layer 120 is exposed to radiation through a reticle and then developed. After being developed, the remaining photodefinable material, photoresist in the illustrated embodiment, forms mask features such as the illustrated lines 124 (shown in cross-section only).

[0050] The pitch of the resulting lines 124 is equal to the sum of the width of a line 124 and the width of a neighboring space 122. To minimize the critical dimensions of features formed using this pattern of lines 124 and spaces 122, the pitch may be at or near the limits of the photolithographic technique used to pattern the photodefinable layer 120. For example, for photolithography utilizing 248 nm light, the pitch of the lines 124 may be about 100 nm. Thus, the pitch may be at the minimum pitch of the photolithographic technique and the spacer pattern discussed below may advantageously have a pitch below the minimum pitch of the photolithographic technique. Alternatively, because the margin of error for position and feature size typically increases as the limits of a photolithographic technique are approached, the lines 124 may be formed having larger feature sizes, *e.g.*, 200 nm or more, to minimize errors in the position and sizes of the lines 124.

[0051] As shown in Figures 5A and 5B, the spaces 122 are widened by etching the photoresist lines 124, to form modified spaces 122a and lines 124a. The photoresist lines 124 are etched using an isotropic etch to "shrink" or trim those features. Suitable etches include etches using an oxygen-containing plasma, *e.g.*, a $SO_2/O_2/N_2/Ar$ plasma, a $Cl_2/O_2/He$ plasma or a $HBr/O_2/N_2$ plasma. The extent of the etch is selected so that the widths of the lines 124a are substantially equal to the desired spacing between the later-formed spacers 175 (Figure 7), as will be appreciated from the discussion below. For example, the width of the lines 124 may be reduced from about 80-120 nm to about 30-70 nm or about 50-70 nm. Advantageously, the width-reducing etch allows the lines 124a to be narrower than would otherwise be possible using the photolithographic technique used to pattern the

photodefinable layer 120. While the critical dimensions of the lines 124a may be etched below the resolution limits of the photolithographic technique, it will be appreciated that this etch does not alter the pitch of the spaces 122a and lines 124a, since the distance between identical points in these features remains the same.

[0052] Next, with reference to Figure 6, a layer 170 of spacer material is blanket deposited conformally over exposed surfaces, including the hard mask layer 150 and the top and sidewalls of the temporary layer 140. The spacer material may be any material that can act as a mask for transferring a pattern to the underlying hard mask layer 130. The spacer material may be, without limitation, silicon, silicon oxide and silicon nitride. In the illustrated embodiment, the spacer material is silicon oxide, which provides particular advantages in combination with other selected materials of the masking stack.

[0053] Methods for spacer material deposition include atomic layer deposition, *e.g.*, using a self- limiting deposition with a silicon precursor and a subsequent exposure to an oxygen or nitrogen precursor to form silicon oxides and nitrides, respectively. In some embodiments, to form silicon oxide, a silicon halide, such as silicon hexachlorodisilane (HCD), is introduced in alternating pulses with an oxygen precursor, such as H_2O. ALD can be performed at relatively low temperatures, *e.g.*, under about 200°C or under about 100°C, which has advantages for preventing thermal damage to underlying carbon-based materials, such as photoresist and amorphous carbon layers. In other embodiments, chemical vapor deposition is used to deposit the spacer material, *e.g.*, using O_3 and TEOS to form silicon oxide.

[0054] The thickness of the layer 170 is determined based upon the desired width of the spacers 175 (Figure 7A). For example, in some embodiments, the layer 170 is deposited to a thickness of about 20-80 nm or about 40-60 nm to form spacers of roughly similar widths. The step coverage is about 80% or greater and or about 90% or greater.

[0055] With reference to Figures 7A and 7B, the silicon oxide spacer layer 170 is subjected to an anisotropic etch to remove spacer material from horizontal surfaces 180 of the partially formed integrated circuit 100.

[0056] With reference to Figures 8A and 8B, the selectively definable layer 120 is next removed to leave freestanding spacers 175. The selectively definable layer 120 may be selectively removed using an organic strip process.

[0057] Thus, pitch–multiplied mask features have been formed. In the illustrated embodiment, the spacers 175 form elongated loops and have substantially parallel legs which are joined at their ends. The pitch of the spacers 175 is roughly half that of the photoresist lines 124 and spaces 122 (Figures 4A and 4B) originally formed by photolithography. Where the photoresist lines 124 had a pitch of about 200 nm, spacers 175 having a pitch of about 100 nm or less may be formed. It will be appreciated that because the spacers 175 are formed on the sidewalls of the features or lines 124b, the spacers 175 generally follow the outline of the pattern of features or lines 124a in the modified photodefinable layer 120a and, so, form a closed loop in the spaces 122a between the lines 124a.

[0058] Next, in a second phase of methods according to some embodiments of the invention, blocks of mask material are overlaid the spacers 175 and the resulting pattern is transferred to the substrate 110.

[0059] With reference to Figures 9A and 9B, a layer 200 of mask material, *e.g.*, photoresist, is deposited between and over the spacers 175. The photoresist layer 200 can be formed of positive or negative photoresist.

[0060] With reference to Figures 10A and 10B, the photodefinable layer 200 is patterned by photolithography to form masking material blocks 210, 212 at the ends of the loops of spacers 175. The blocks 210, 212 extend across and contact opposite ends of the spacers 175. Advantageously, the blocks 210, 212 have dimensions sufficiently large to be patterned with photolithography and without performing pitch multiplication. Thus, a mixed pattern 177 formed of pitch multiplied and non-pitch multiplied mask features can be formed. The blocks 210, 212 may be patterned simultaneously with other relatively large features formed in the periphery region of the partially fabricated integrated circuit 100. Methods for combining pitch multiplied and non-pitch multiplied features are disclosed in U.S. Patent Nos. 7,115,525 and 7,253,118 and U.S. Patent Application No. 11/831,012, filed July 31, 2007 by Luan C. Tran. The entire disclosure of each of these references is incorporated herein by reference.

[0061] With reference to Figure 11, the pattern 177 defined by the blocks 210, 212 and the spacers 175 is transferred to the hard mask layer 130. The pattern transfer may be accomplished by, *e.g.*, anisotropically etching the hard mask layer 130.

[0062] With reference to Figure 12, the pattern 177 is transferred to the primary mask layer 140. The pattern transfer may be accomplished by, *e.g.*, anisotropically etching the primary mask layer 140. With reference to Figure 13, the pattern 177 is transferred to the substrate 110 using an anisotropic etch with the layer 140 acting as a mask for the etch.

[0063] With reference to Figures 14A and 14B, the spacers 175 and mask layers 130 and 140 overlying the substrate 110 are removed. Pitch multiplied lines 310 are formed in the substrate 110. At each of their ends, the lines 310 contact laterally separated blocks 320, 322.

[0064] With reference to Figure 15, trenches defined by the lines 310 and blocks 320, 322 are filled with insulating material 330, *e.g.*, silicon oxide, for shall trench isolation applications. Memory cell active areas, such as for flash memory, may be defined between the trenches and floating and control gates may be formed over the active areas.

[0065] As part of the formation of the floating and control gates, a stack of layers 340 for forming the floating and control gates is subsequently formed over the lines 310, insulating material 330 and blocks 320, 322 (Figure 14B). It will be appreciated that the composition of the layers 340 can vary across the partially fabricated integrated circuit 100. For example, in some areas, where, *e.g.*, both floating and control gates are desired, the layers 340 can include layers appropriate for the formation of these gates. In other areas, where, *e.g.*, only a select gate is desired, the layers 340 can include fewer layers, as appropriate for formation of the select gate. For example, for forming the select gate, the layers 340 may include a silicide layer over a polysilicon layer, which overlies an oxide-nitride-oxide (ONO) composite layer, which overlies a polysilicon layer.

[0066] With reference to Figure 16A, a mask layer 350 is formed over the stack of layers 340. The mask layer 350 may be a selectively definable layer 350 formed of, *e.g.*, photoresist. With reference to Figures 16B and 16C, the layer 350 is subsequently patterned, thereby forming elongated strips 352-356. The patterned elongated strips 352-356 may be used to form various features in a memory device. For example, the strips 352-355 may be

used to form select gates for regulating reading and writing to memory cells formed along the lines 310, which form active areas. The strips 356 may be used to define word lines and floating and control gates.

[0067] It will be appreciated that the strips 352-356 may be formed in a single step, *e.g.*, by photolithography, or in multiple separate steps. For example, to increase density, the strips 356 may be formed by pitch multiplication. As such, a stack of masking layers as described herein with reference to Figures 3A and 3B can be formed over the layers 340. The stack of masking layers may then be processing as discussed herein with reference to Figures 3A-8B. The resulting spacer loops may then be subjected to a loop etch, thereby forming the strips 356. The mask layer 350 (Figure 16A) may subsequently be deposited between and over the spacers 175. The mask layer 350 is then patterned, *e.g.*, by photolithography where the mask layer 350 is formed of photoresist, thereby forming the strips 352-355 (Figures 16B and 16C). While not illustrated for ease of discussion, as discussed herein, one or more additional masking layers may be provided between the mask layer 350 to facilitate pattern transfer to the layers 340. For example, an ARC layer may be provided directly beneath the mask layer 350 and an amorphous carbon layer may be provided between the ARC layer and the layer 340. Such a sequence of layers would provide the advantages and could be utilized as noted above for the layers 130 and 140 (Figures 3A-13).

[0068] With reference to Figures 17A and 17B, the pattern in the mask layer 350 is then transferred to the layers 340, thereby forming strips 342-346 in those layers. The strips 342-346 may correspond to word lines, floating gates, control gates and select gates in those layers.

[0069] It will be appreciated that the exposed parts of the lines 310 and blocks 320, 322 of semiconductor material are doped (*e.g.*, with an n-type dopant) to form source/drain regions in the lines 310 and blocks 320, 322 on either side of the strips 342-346. In some embodiments, the feature 320 forms a source and the feature 342 form a gate of isolation transistors for each of the lines 310. Similarly, on an opposite end of the lines 310, the feature 322 forms a source and the feature 343 form a gate of additional isolation transistors for each of the lines 310.

[0070] In subsequent processing steps, contacts are made to the various bit and word lines and the bit and word lines are connected to various ancillary circuitry to form a memory device. In some embodiments, the contacts may be made from a level above the bit and word lines. In addition, contacts to the source regions 320, 322 can be electrically connected to the gates 342, 343, respectively, so that the gates and sources of the isolation transistors are tied together for simplicity of operation and reliability, as discussed herein.

[0071] Figure 18 illustrates a block of a NAND flash memory array in a memory device 400 according to some embodiments of the invention. The illustrated flash memory array includes bit lines BL0 to BLM and word lines WL0 to WLN. The bit lines BL0-BLM extend parallel to one another in a column direction. The word lines WL0-WLN extend parallel to one another in a row direction. The NAND flash memory array also includes select transistors 402, 404 used for selecting a bit line. Ancillary logic and other circuitry (not shown) connect to the bit lines using the bit line contacts 406. The gates of the rows of select transistors 402, 404 correspond to the features 344, 345 (Figure 17B).

[0072] Each bit line includes a string of floating gate transistors coupled in series, source to drain. For example, the second bit line BL1 includes floating gate transistors 110 connected in series. The control gates of floating gate transistors 110 of cells in the same row are coupled to the same word line. Each of the floating gate transistors 110 forms a memory cell that stores a charge (or a lack of charge), wherein the amount of stored charge can be used to represent, for example, one or more states, and wherein the one or more states can represent one or more digits (*e.g.*, bits) of data. The bit is read by detecting the absence or presence of charge.

[0073] With continued reference to Figure 18, bit lines BL0 to BLM are shunted together at their ends. Isolation, or select, transistors 412, 414 electrically isolate individual bit lines from each other by preventing current flow to the shunted ends of the bit lines. The shunted ends correspond to the blocks 320 and 322 (Figure 17B) and the gates of the select transistors 412, 414 correspond to the features 342, 343 (Figure 17B).

[0074] It will be appreciated that each pair of bit lines, which can also be viewed as a loop of semiconductor material, may include a total of four isolation transistors. For example, isolation transistors 412a and 412b constitute first and second isolation transistors

proximate one end of the loop and isolation transistors 414a and 414b constitute third and fourth isolation transistors proximate an opposite end of the loop. Thus, a pair of isolation transistors may be utilized to electrically isolate a single bit line, which are formed by substantially parallel, horizontally elongated portions of the loops. The isolation transistors isolate the expanse of one of these elongated portions from an expanse of another of these elongated portions.

[0075] As illustrated in Figure 18, the source/drain regions of the select transistors 412, 414 are electrically tied or connected to the gates of these transistors and are biased in an off state. During read and write cycles, the gates and tied source/drains can be left floating or connected to ground (0V), thereby electrically isolating all bit lines connected to the isolation transistors 412, 414. During erase operations, the transistors 412, 414 may be in an "on" state. However, because all memory cells are erased simultaneously, the state of the transistors 412, 414 is irrelevant; there is no need to isolate individual bit lines, since the same operation is performed on all cells of the NAND flash memory block.

[0076] As noted above, with reference to Figure 19, a fully formed integrated circuit 101 formed from the partially fabricated integrated circuit 100 can be incorporated into various systems or devices. For example, the integrated circuit 101 can be utilized as memory for storing data in an electronic device 102 having a computer processor 103, a user interface 104 and power source 105. Examples of such electronic devices include computerized devices, including any device utilizing a memory circuit, such as data storage and retrieval devices, including music, photo and/or video devices.

[0077] It will be appreciated that various modifications of the illustrated embodiments are possible. For example, while illustrated with blocks of material for shunting together loops of material, the blocks can be omitted in some embodiments. In those embodiments, contact to individual loop ends are made.

[0078] However, the blocks are advantageously for simplifying operation of the isolation transistors and for improving process results. By tying all the loops together, individual access to the loops is obviated, thereby simplifying fabrication and operation of the isolation transistors. Moreover, the blocks can improve process results by facilitating deposition of dielectric into the trenches 312 (Figure 14B). It has been found that the ends of

pitch multiplied loops can be relatively thin relative to mid-portions of the loops. It has also been found that deposition of dielectric into these relatively thin ends can be difficult and prone to void formation. By eliminating these ends by overlying the ends with blocks of masking material, it has been found that filling of the trenches can be improved, leading to integrated circuits with improved reliability.

[0079] In some embodiments, the isolation transistors can be omitted from one end of the loops of material. For example, where the material is shunted together for another reason, *e.g.*, where the lines forming the loop are all tied to ground at one end, it may be unnecessary to form an isolation transistor to electrically isolate the lines on the end that is tied to ground. However, as noted above, the formation of block of material at the ends of the loops has benefits for improving filling of trenches defined by the lines. As a result, it may be desirable to form the blocks at both loop ends, even where electrical isolation is not necessary at one end.

[0080] It will be appreciated that, as used herein "lines" of material need not extend in only a single direction through the entire extent of the "lines". Rather, a "line" of material is an elongated run of material and may curve or otherwise change direction over the expanse of the line of material.

[0081] In addition, in any of the steps described herein, transferring a pattern from an overlying level to an underlying level involves forming features in the underlying level that generally correspond to features in the overlying level. For example, the path of lines in the underlying level will generally follow the path of lines in the overlying level and the location of other features in the underlying level will correspond to the location of similar features in the overlying level. The precise shapes and sizes of features may vary from the overlying level to the underlying level, however. For example, depending upon etch chemistries and conditions, the sizes of and relative spacings between the features forming the transferred pattern may be enlarged or diminished relative to the pattern on the overlying level, while still resembling the same initial "pattern," as can be seen from the example of shrinking the first resist mask in the embodiments described below. Thus, even with some changes in the dimensions of features, the transferred pattern is still considered to be the

same pattern as the initial pattern. In contrast, forming spacers around mask features may change the pattern.

[0082] Consequently, it will be appreciated from the description herein that the invention includes various embodiments. For example, according to some embodiments of the invention, a method is provided. The method comprises providing a substrate having a loop formed of semiconductor material. The loop is defined by a pair of substantially parallel, horizontally elongated portions joined at at least one loop end. A first transistor along the loop is formed to electrically isolate an expanse of a first of the elongate portions from an expanse of a second of the elongate portions. A part of the loop forms an active area of the first transistor.

[0083] According to other embodiments the invention, a process is provided for forming an integrated circuit. The process comprises providing a plurality of mandrels overlying a substrate. A spacers are provided at sidewalls of the mandrels. The mandrels are selectively removed relative to the spacers. A layer of mask material is deposited over the spacers. The layer of mask material is patterned to form first and second laterally-separated blocks of the mask material, the first block contacting a first end of each of the spacers and the second block contacting a second end of each of the spacers. A first pattern defined by the spacers and the first and second blocks are transferred to the substrate.

[0084] According to yet other embodiments of the invention, a process for forming an integrated circuit is provided. The process comprises providing a plurality of elongated loops of a first mask material overlying a substrate. A layer of a second mask material is provided over the loops. The layer is patterned to form a block of the second mask material, the block contacting an end of each of the loops. A first pattern defined by the loops and the block is transferred to the substrate. A layer of semiconductor material is subsequently formed over the substrate. An other layer of mask material is formed over the semiconductor material. The other layer is patterned to form one or more strips of masking material extending across and contacting each of the loops. A second pattern defined by the strips is transferred to the layer of semiconductor material to form strips of semiconductor material. The strips of semiconductor material are electrically connected to substrate features defined by the block of the second mask material.

[0085] According to other embodiments the invention, an integrated circuit is provided. The integrated circuit comprises a plurality of spaced apart lines of semiconductor material. A first block of the semiconductor material is disposed on a same level as the lines of semiconductor material and contact a first end of each of the elongate strips. A first plurality of transistor gates is disposed along the lines of semiconductor material. The first plurality of transistor gates are electrically connected to the first block.

[0086] According to yet other embodiments the invention, an electrical device comprising an integrated circuit is provided. The integrated circuit comprises a plurality of spaced-apart lines of semiconductor material. All of a first end of the lines are electrically interconnected and all of an opposite end of the lines are electrically interconnected. A means for preventing current flow from a mid-portion of the lines to the first end is provided.

[0087] It will also be appreciated by those skilled in the art that various omissions, additions and modifications may be made to the methods and structures described above without departing from the scope of the invention. All such modifications and changes are intended to fall within the scope of the invention, as defined by the appended claims.

I CLAIM:

1. A method, comprising:

providing a substrate having a loop formed of semiconductor material, the loop defined by a pair of substantially parallel, horizontally elongated portions joined at at least one loop end; and

forming a first transistor along the loop to electrically isolate an expanse of a first of the elongate portions from an expanse of a second of the elongate portions, wherein a part of the loop forms an active area of the first transistor.

2. The method of Claim 1, wherein the first transistor is disposed along the first elongate portion, further comprising forming a second transistor along the second elongate portion, a part of the loop forming a active area of the second transistor, wherein the first transistor and the second transistor are disposed proximate the loop end.

3. The method of Claim 2, wherein the elongate portions are joined at an opposite end to the loop end, further comprising forming a third transistor along the first elongate portion proximate the looped end and forming a fourth transistor along the second elongate portion proximate the opposite end.

4. The method of Claim 1, wherein providing the substrate having the loop comprises forming the loop using pitch multiplication.

5. The method of Claim 4, wherein forming the loop using pitch multiplication comprises:

forming a mandrel over the substrate;

forming a spacer on sidewalls of the mandrel;

removing the mandrels to leave a pattern of free-standing spacers; and

etching a pattern defined by the free-standing spacers into a layer comprising the semiconductor material.

6. The method of Claim 1, wherein providing the substrate having the loop comprises providing a plurality of lines of semiconductor material, wherein the lines are each contiguous with a block of semiconductor material at the loop end.

7. The method of Claim 1, wherein forming the first transistor comprises doping either side of the active area to form source/drain regions.

8. The method of Claim 7, wherein forming the first transistor comprises forming a transistor gate directly over the loop, the gate defining the active region thereunder.

9. The method of Claim 8, wherein the looped end is a source region and wherein forming the first transistor comprises shunting together the source region and the gate.

10. A process for forming an integrated circuit, comprising:

providing a plurality of mandrels overlying a substrate;

providing spacers at sidewalls of the mandrels;

selectively removing the mandrels relative to the spacers;

depositing a layer of mask material over the spacers;

patterning the layer of mask material to form first and second laterally-separated blocks of the mask material, the first block contacting a first end of each of the spacers and the second block contacting a second end of each of the spacers; and

transferring a first pattern defined by the spacers and the first and second blocks to the substrate.

11. The process of Claim 10, wherein providing a plurality of mandrels comprises:

providing a photoresist layer overlying a temporary layer;

patterning the photoresist layer to form photoresist features; and

trimming the photoresist features, wherein the trimmed photoresist features form the mandrels.

12. The process of Claim 10, wherein providing spacers at sidewalls of the mandrels comprises:

blanket depositing a layer of spacer material over the photoresist features; and

removing the spacer material from horizontal surfaces to define spacers on sidewalls of the photoresist features.

13. The process of Claim 10, wherein transferring the first pattern defined by the spacers and the first and second blocks to the substrate comprises:

transferring the first pattern defined by the spacers and the first and second blocks to a hard mask layer; and

transferring the first pattern from the hard mask layer to the substrate.

14. The process of Claim 13, further comprising:

providing one or more additional hard mask layers on a level between the spacers and the hard mask layer; and

transferring the first pattern to the one or more additional hard mask layers before transferring the first pattern to the hard mask layer.

15. The process of Claim 13, wherein the hard mask layer is formed of amorphous carbon.

16. The process of Claim 10, wherein depositing a layer of mask material over the spacers comprises depositing a layer of photoresist.

17. A process for forming an integrated circuit, comprising:

providing a plurality of elongated loops of a first mask material overlying a substrate;

providing a layer of a second mask material over the loops;

patterning the layer to form a block of the second mask material, the block contacting an end of each of the loops;

transferring a first pattern defined by the loops and the block to the substrate;

subsequently forming a layer of semiconductor material over the substrate;

forming an other layer of mask material over the semiconductor material;

patterning the other layer to form one or more strips of masking material extending across and contacting each of the loops;

transferring a second pattern defined by the strips to the layer of semiconductor material to form strips of semiconductor material; and

electrically connecting the strips of semiconductor material and substrate features defined by the block of the second mask material.

18. The process of Claim 17, wherein transferring the second pattern defines a gate of a transistor and transferring the first pattern defines a source/drain region of the transistor.

19. The process of Claim 17, wherein transferring the first pattern defines bit lines of a memory device.

20. The process of Claim 19, wherein transferring the second pattern defines word lines of the memory device.

21. The process of Claim 17, wherein the integrated circuit is a flash memory circuit, wherein transferring the first and the second patterns defines floating gate transistors in an array region of the flash memory circuit.

22. The process of Claim 17, wherein patterning the layer defines features in a periphery region of the flash memory circuit.

23. An integrated circuit, comprising:

a plurality of spaced apart lines of semiconductor material;

a first block of the semiconductor material on a same level as the lines of semiconductor material and contacting a first end of each of the elongate strips; and

a first plurality of transistor gates disposed along the lines of semiconductor material, the first plurality of transistor gates electrically connected to the first block.

24. The integrated circuit of Claim 23, further comprising:

a second block of the semiconductor material on a same level as the elongate strips and contacting a second end of the lines of semiconductor material; and

a second plurality of transistor gates disposed along the lines of semiconductor material, the second plurality of transistor gates electrically connected to the second block.

25. The integrated circuit of Claim 23, wherein the first block forms a first source/drain for a first plurality of transistors comprising the first block and the first plurality of transistor gates, and wherein the second block forms a second source/drain for a second plurality of transistors comprising the second block and the second plurality of transistor gates.

26. The integrated circuit of Claim 23, wherein the lines of semiconductor material constitute bit lines of a memory device.

27. The integrated circuit of Claim 26, wherein the first plurality of transistor gates constitute parts of word lines of a memory device.

28. An electrical device comprising an integrated circuit, the integrated circuit comprising:

a plurality of spaced-apart lines of semiconductor material, wherein all of a first end of the lines are electrically interconnected and all of an opposite end of the lines are electrically interconnected; and

a means for preventing current flow from a mid-portion of the lines to the first end.

29. The electrical device of Claim 28, wherein the lines define memory cells in a memory array.

30. The electrical device of Claim 29, wherein the integrated circuit is a flash memory device.

31. The electrical device of Claim 28, wherein the means for preventing current flow comprises:

transistors proximate the first end, wherein the lines form active areas of the transistors and wherein a block of semiconductor electrically connects the lines at the first end, wherein the block of semiconductor material forms source/drain regions of the transistors.

32. The electrical device of Claim 28, further comprising an other means for preventing current flow from a mid-portion of the lines to the second end.

33. The electrical device of Claim 32, wherein the other means comprises:

transistors proximate the second end, wherein the lines form active areas of the transistors and wherein a block of semiconductor electrically connects the lines at the second end, wherein the block of semiconductor material forms source/drain regions of the transistors.