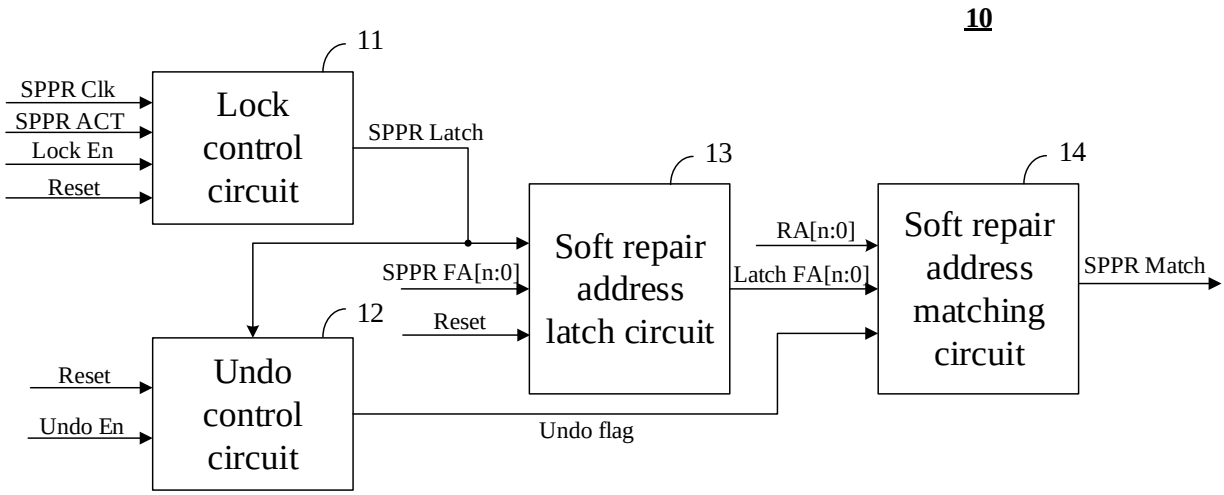


FIG. 1

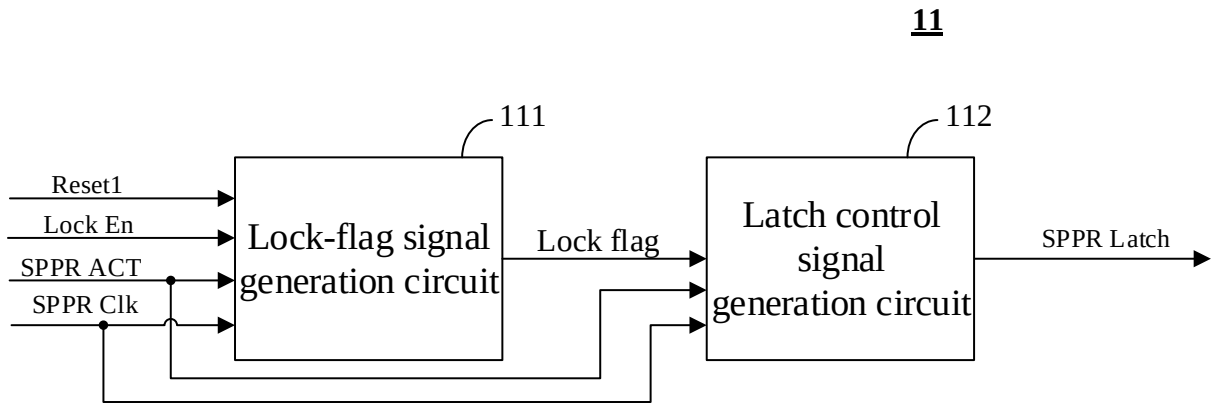


FIG. 2

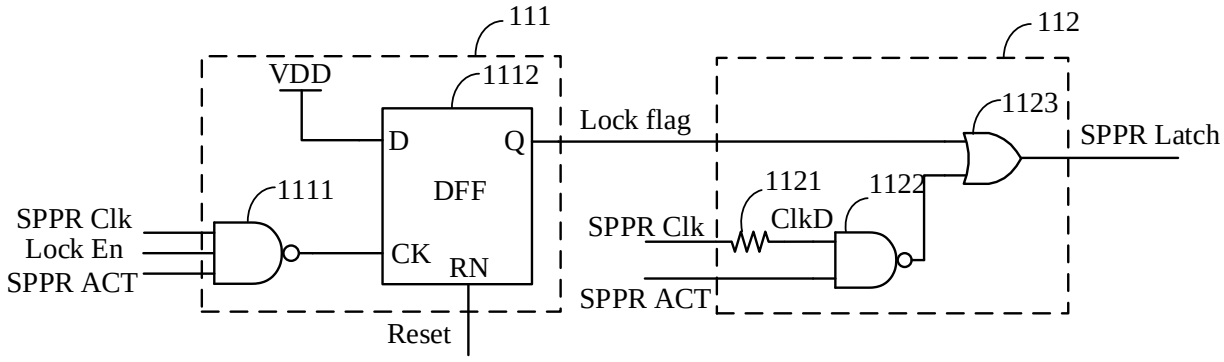


FIG. 3

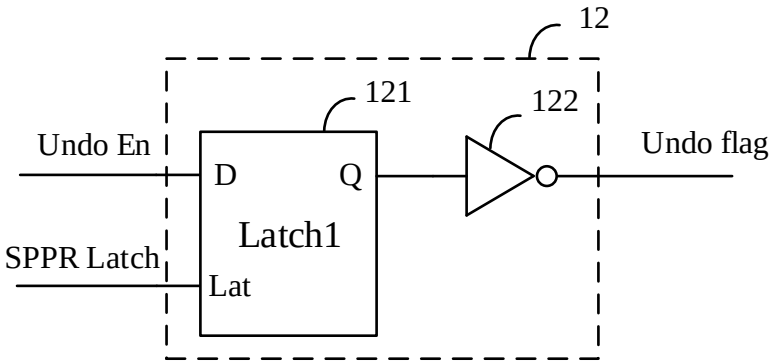


FIG. 4

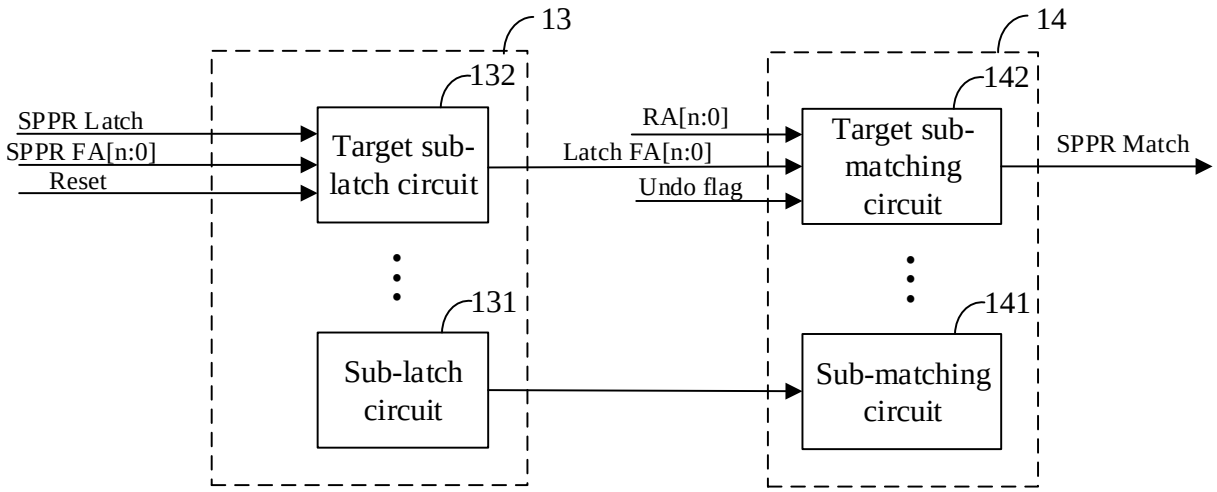


FIG. 5A

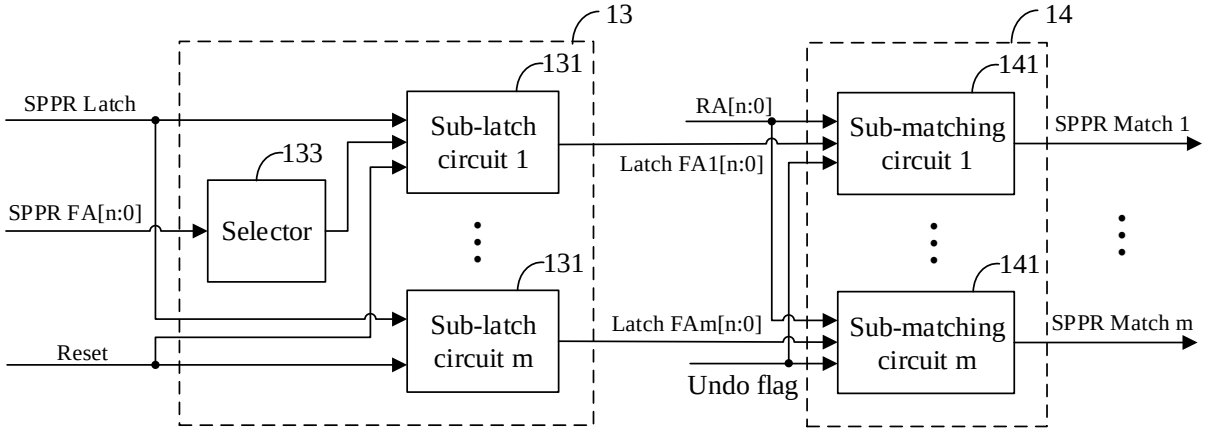


FIG. 5B

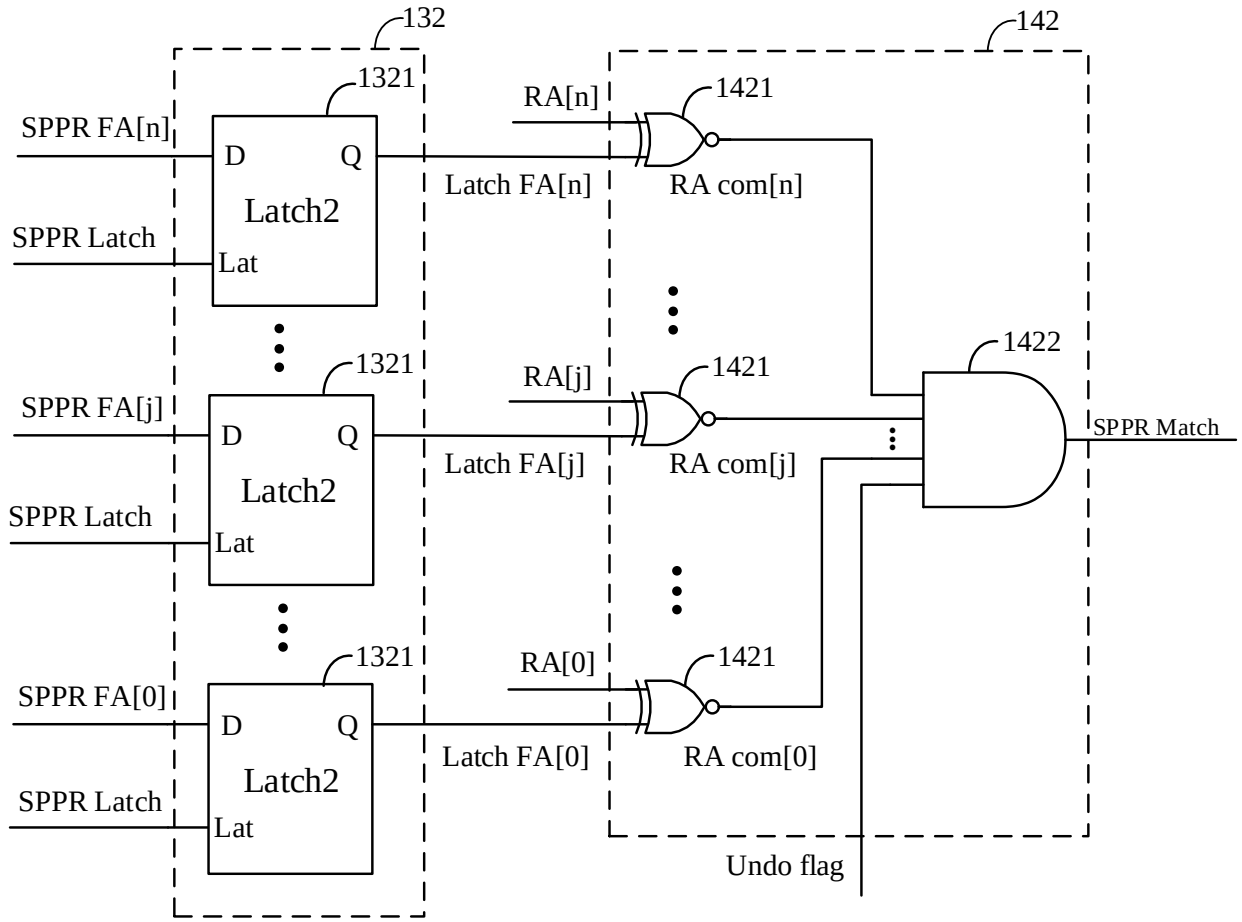

132
142
1321
1421
1422
SPPR FA[n]
SPPR Latch
D
Q
Latch2
Lat
RA[n]
Latch FA[n]
RA com[n]
SPPR FA[j]
RA[j]
Latch FA[j]
RA com[j]
SPPR Match
SPPR FA[0]
RA[0]
Latch FA[0]
RA com[0]
Undo flag

FIG. 6

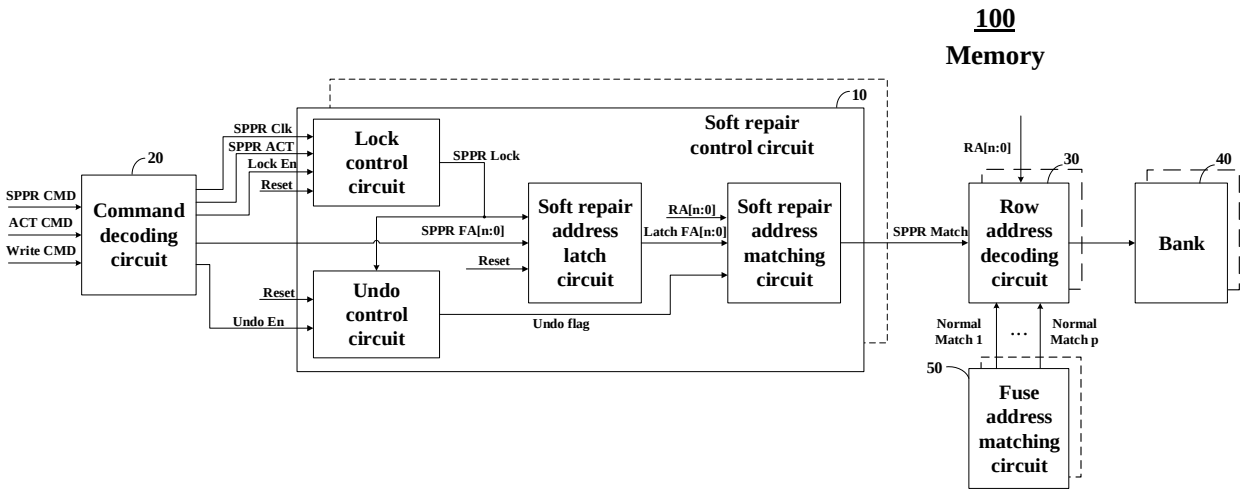

100
Memory
10
Soft repair control circuit
20
Command decoding circuit
SPPR CMD
ACT CMD
Write CMD
SPPR Clk
SPPR ACT
Lock En
Reset
Lock control circuit
SPPR Lock
SPPR FA[n:0]
Reset
Soft repair address latch circuit
RA[n:0]
Latch FA[n:0]
Soft repair address matching circuit
Reset
Undo En
Undo control circuit
Undo flag
SPPR Match
RA[n:0]
30
Row address decoding circuit
40
Bank
Normal Match 1
Normal Match p
50
Fuse address matching circuit

FIG. 7

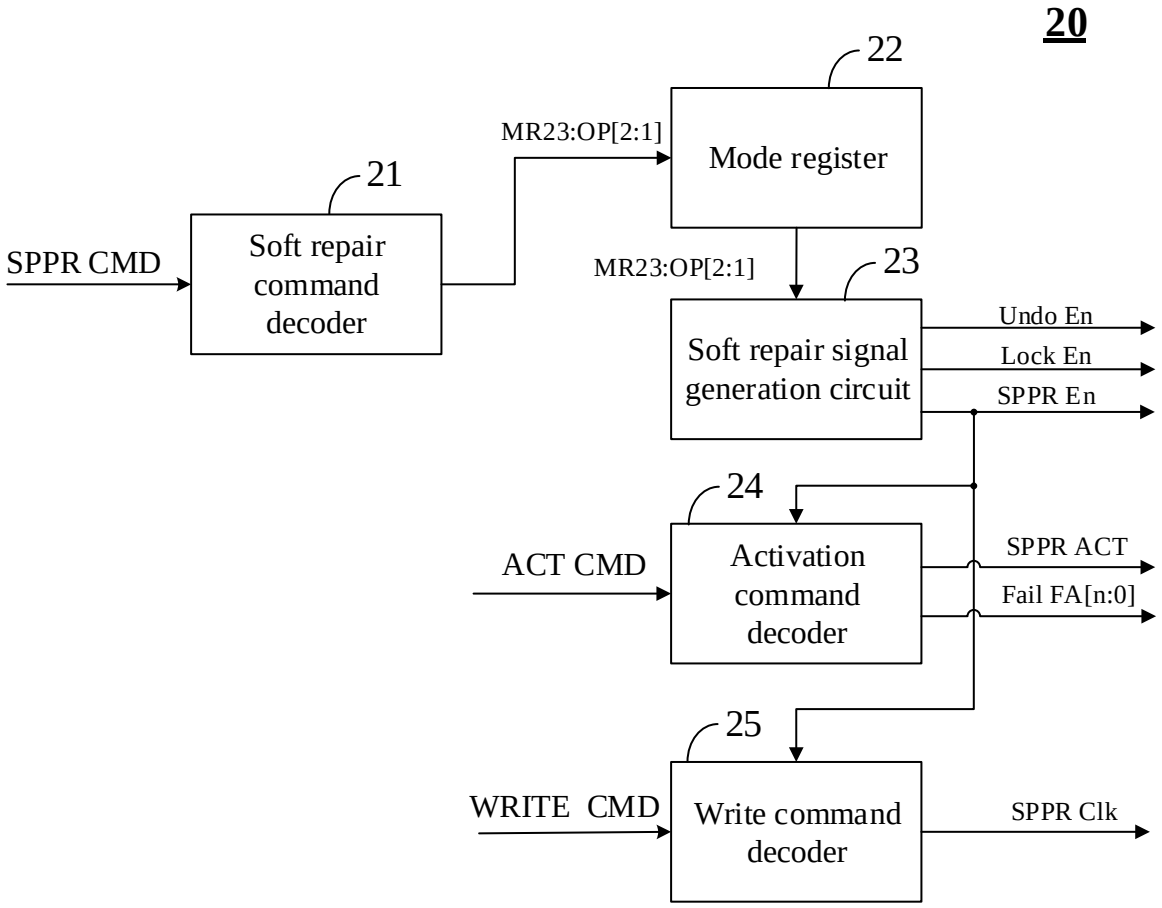

20
22
Mode register
MR23:OP[2:1]
21
SPPR CMD
Soft repair command decoder
MR23:OP[2:1]
23
Soft repair signal generation circuit
Undo En
Lock En
SPPR En
24
ACT CMD
Activation command decoder
SPPR ACT
Fail FA[n:0]
25
WRITE CMD
Write command decoder
SPPR Clk

FIG. 8

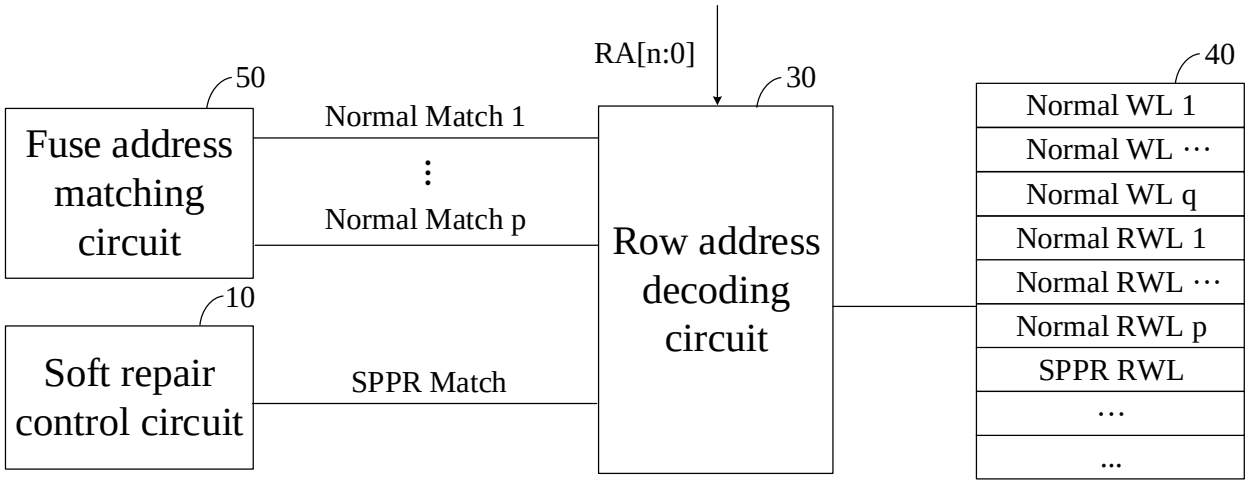

RA[n:0]
50
Fuse address matching circuit
Normal Match 1
Normal Match p
30
Row address decoding circuit
40
Normal WL 1
Normal WL ⋯
Normal WL q
Normal RWL 1
Normal RWL ⋯
Normal RWL p
SPPR RWL
⋯
...
10
Soft repair control circuit
SPPR Match

FIG. 9

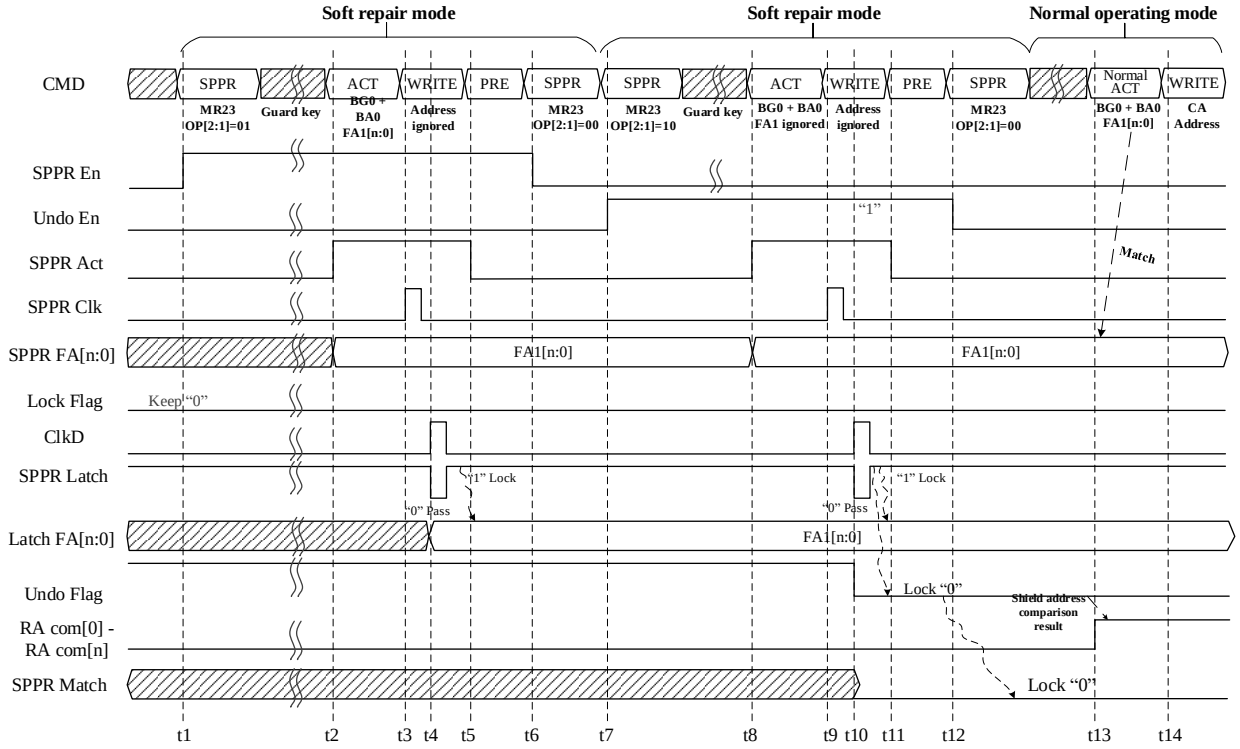

Soft repair mode
Soft repair mode
Normal operating mode
CMD
SPPR
MR23 OP[2:1]=01
Guard key
ACT
BG0 + BA0 FA1[n:0]
WRITE
Address ignored
PRE
SPPR
MR23 OP[2:1]=00
SPPR
MR23 OP[2:1]=10
Guard key
ACT
BG0 + BA0 FA1 ignored
WRITE
Address ignored
PRE
SPPR
MR23 OP[2:1]=00
Normal ACT
BG0 + BA0 FA1[n:0]
WRITE
CA Address
SPPR En
Undo En
"1"
SPPR Act
Match
SPPR Clk
SPPR FA[n:0]
FA1[n:0]
FA1[n:0]
Lock Flag
Keep "0"
ClkD
SPPR Latch
"1" Lock
"0" Pass
"1" Lock
"0" Pass
Latch FA[n:0]
FA1[n:0]
Undo Flag
Lock "0"
Shield address comparison result
RA com[0] - RA com[n]
SPPR Match
Lock "0"
t1
t2
t3
t4
t5
t6
t7
t8
t9
t10
t11
t12
t13
t14

FIG. 10

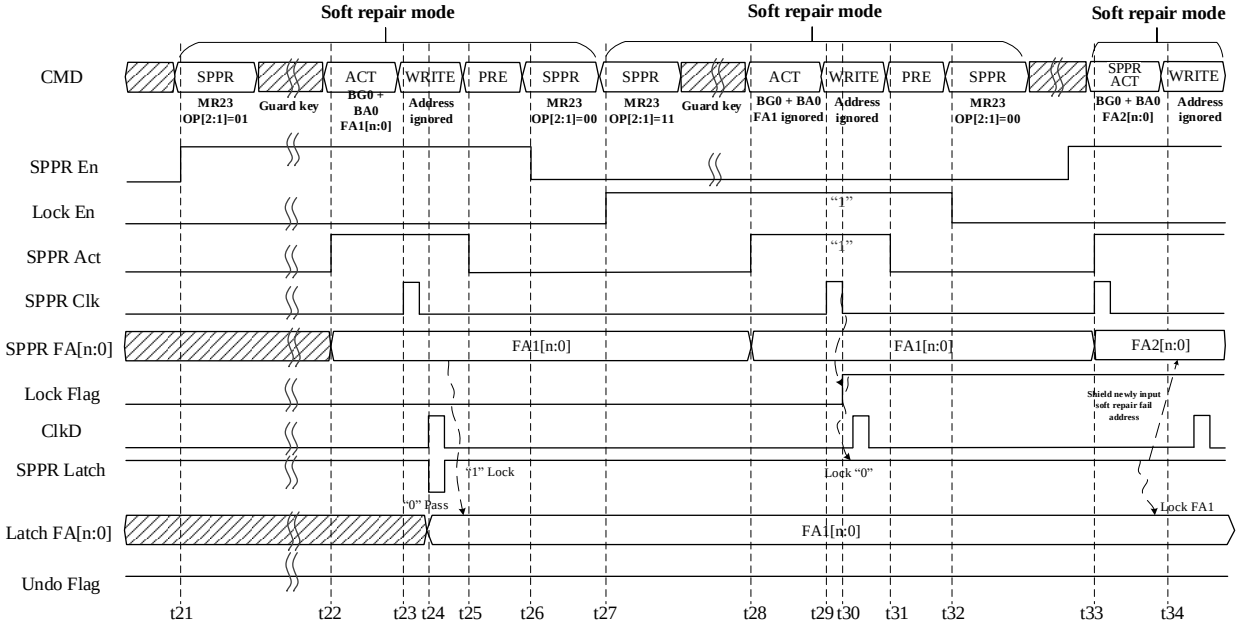

Soft repair mode
Soft repair mode
Soft repair mode
CMD
SPPR
MR23 OP[2:1]=01
Guard key
ACT
BG0 + BA0 FA1[n:0]
WRITE
Address ignored
PRE
SPPR
MR23 OP[2:1]=00
SPPR
MR23 OP[2:1]=11
Guard key
ACT
BG0 + BA0 FA1 ignored
WRITE
Address ignored
PRE
SPPR
MR23 OP[2:1]=00
SPPR ACT
BG0 + BA0 FA2[n:0]
WRITE
Address ignored
SPPR En
Lock En
"1"
SPPR Act
"1"
SPPR Clk
SPPR FA[n:0]
FA1[n:0]
FA1[n:0]
FA2[n:0]
Lock Flag
Shield newly input soft repair fail address
ClkD
SPPR Latch
"1" Lock
"0" Pass
Lock "0"
Lock FA1
Latch FA[n:0]
FA1[n:0]
Undo Flag
t21
t22
t23
t24
t25
t26
t27
t28
t29
t30
t31
t32
t33
t34

FIG. 11

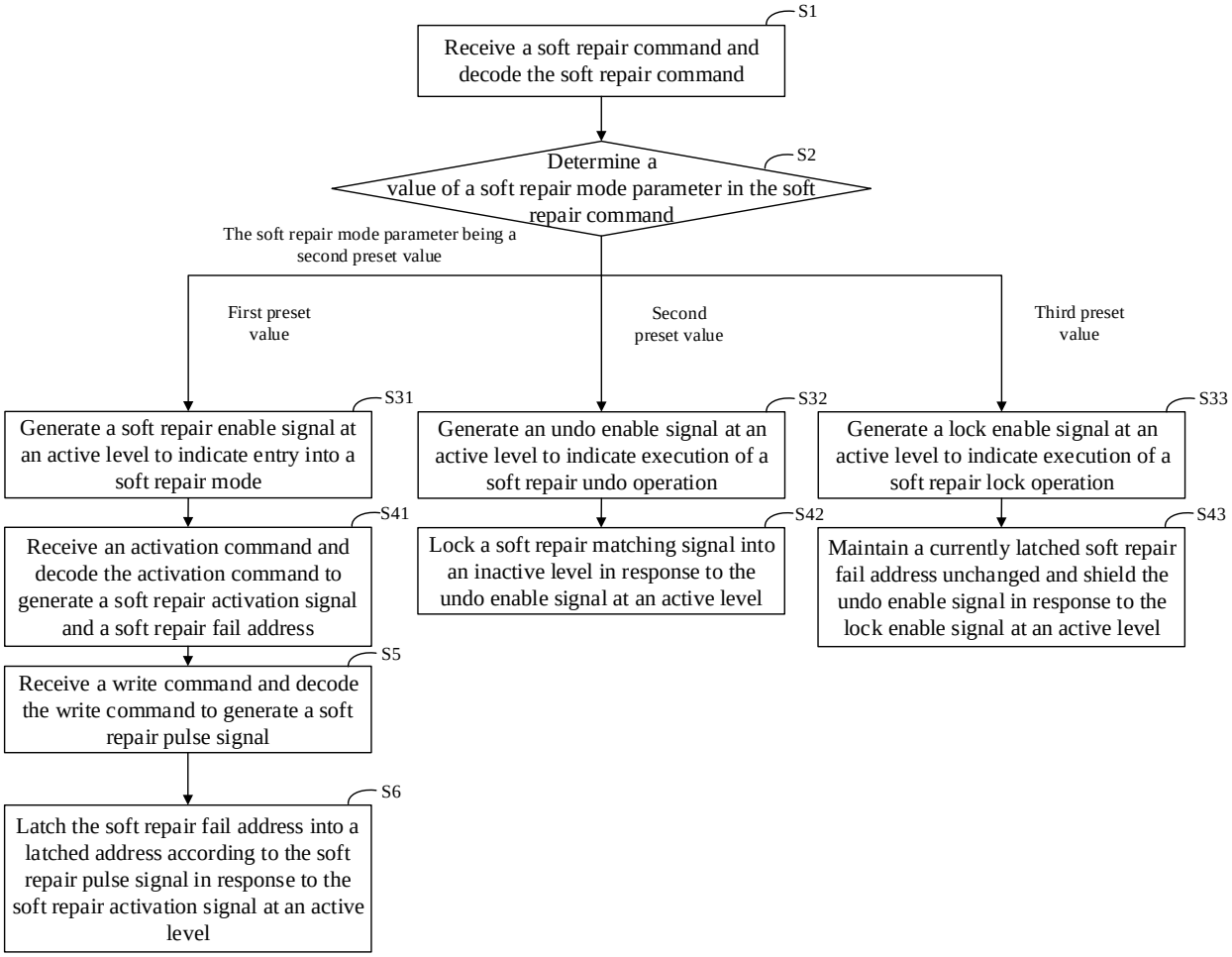

S1
Receive a soft repair command and decode the soft repair command
S2
Determine a value of a soft repair mode parameter in the soft repair command
The soft repair mode parameter being a second preset value
First preset value
Second preset value
Third preset value
S31
Generate a soft repair enable signal at an active level to indicate entry into a soft repair mode
S32
Generate an undo enable signal at an active level to indicate execution of a soft repair undo operation
S33
Generate a lock enable signal at an active level to indicate execution of a soft repair lock operation
S41
Receive an activation command and decode the activation command to generate a soft repair activation signal and a soft repair fail address
S42
Lock a soft repair matching signal into an inactive level in response to the undo enable signal at an active level
S43
Maintain a currently latched soft repair fail address unchanged and shield the undo enable signal in response to the lock enable signal at an active level
S5
Receive a write command and decode the write command to generate a soft repair pulse signal
S6
Latch the soft repair fail address into a latched address according to the soft repair pulse signal in response to the soft repair activation signal at an active level

FIG. 12