We Claim:

1. A method for manufacturing integrated circuit devices, optical devices, micromachines and mechanical precision devices comprising the steps of

(1) providing a substrate having patterned material layers having line-space dimensions of 50 nm and less and aspect ratios of >2;

(2) providing the surface of the patterned material layers with a positive or a negative electrical charge by contacting the semiconductor substrate at least once with an aqueous, fluorine-free solution S containing at least one fluorine-free cationic surfactant A having at least one cationic or potentially cationic group, at least one fluorine-free anionic surfactant A having at least one anionic or potentially anionic group, or at least one fluorine-free amphoteric surfactant A; and

(3) removing the aqueous, fluorine-free solution S from the contact with the substrate.

2. The method according to claim 1, characterized in that the substrate is a semiconductor substrate.

3. The method according to claim 1 or 2, characterized in that the patterned material layers are having a line-space dimensions of 32 nm and less and aspect ratios of >10 for non-photoresist structures and aspect ratios of >2 for photoresist structures.

4. The method according to anyone of the claims 1 to 3, characterized in that the aqueous solution S is used as an immersion liquid S for immersing photoresists during irradiation with actinic light through a mask, a developer solution S for photoresists layers exposed to actinic radiation through a mask and an immersion liquid and/or as a chemical rinse solution S for rinsing the patterned material layers.

5. The method according to anyone of the claims 1 to 4, characterized in that the patterned material layers are selected from the group consisting of patterned

developed photoresist layers, patterned barrier material layers, patterned multi stack material layers and pattern dielectric material layers.

6. The method according to anyone of the claims 1 to 5, characterized in that the potentially cationic and cationic groups are selected from the group consisting of primary, secondary and tertiary amino groups, primary, secondary, tertiary and quaternary ammonium groups, uronium-, thiouronium- und guanidinium groups, quaternary phosphonium groups and tertiary sulfonium groups; and that the potentially anionic and anionic groups are selected from the group consisting of carboxylic acid, sulfonic acid, phosphonic acid, sulfuric acid monoester, phosphoric acid monoester and phosphoric acid diester groups and carboxylate, sulfonate, phosphonates, monoester sulfate, monoester phosphate and diester phosphate groups.

7. The method according to anyone of the claims 1 to 6, characterized in that the solution S contains, based on a complete weight of the solution S, 0.0005 to 1% by weight of the ionic surfactant A.

8. The method according to anyone of the claims 1 to 7, characterized in that the solution S is removed from the contact with the substrate by spin drying or drying processes making use of the Marangoni effect.

9. The method according to anyone of the claims 1 to 8, characterized in that the substrate having patterned material layers having line-space dimensions of 50 nm and less and aspect ratios of >2 is provided by a photolithographic process.

10. The method according to claim 9, characterized in that the photolithographic process comprises the steps of

(i) providing the substrate with an immersion photoresist layer, an extreme UV (EUV) photoresist layer or an electron beam (eBeam) photoresist layer;

(ii) exposing the photoresist layer to actinic radiation through a mask with or without an immersion liquid;

(iii) developing the exposed photoresist layer with a developer solution to obtain a pattern having line-space dimensions of 32 nm and less and an aspect ratio >2;

(iv) applying a chemical rinse solution to the developed patterned photoresist layer; and

(v) spin drying the semiconductor substrate after the application of the chemical rinse solution;

wherein at least one of the following: the immersion liquid, the developer solution and the chemical rinse solution, is an aqueous, fluorine-free solution S.

11. The method according to anyone of the claims 1 to 10, characterized in that it is used for preventing pattern collapse, for reducing line edge roughness, for preventing and removing watermark defects and for reducing defects by removing particles.

12. The method according to anyone of the claims 1 to 11, characterized in that the integrated circuit devices comprise integrated circuits having a large-scale integration (LSI), very-large-scale integration (VLSI) or the ultra-large-scale integration (ULSI).

We claim:

1. A method for manufacturing a device, the method comprising:

(1) contacting a substrate having patterned material layers having line-space dimensions of 50 nm and less and aspect ratios of >2 at least once with an aqueous, fluorine-free solution S comprising i) a fluorine-free cationic surfactant A comprising a cationic or potentially cationic group, ii) a fluorine-free anionic surfactant A comprising an anionic or potentially anionic group, or iii) a fluorine-free amphoteric surfactant A, thereby providing a surface of the patterned material layers with a positive or a negative electrical charge, wherein a replusive electrostatic force is created; and

(2) removing the aqueous, fluorine-free solution S from the contact with the substrate,

wherein the patterned material layers are patterned developed photoresist layers, patterned barrier material layers, patterned multi-stack material layers, or pattern dielectric material layers.

2. The method of claim 1, wherein the substrate is a semiconductor substrate.

3. The method of claim 1, wherein the patterned material layers comprise photoresist structures and have line-space dimensions of 32 nm and less and aspect ratios of >10.

4. The method of claim 1, wherein the aqueous, fluorine-free solution S is an immersion liquid S for immersing photoresists during irradiation with actinic light through a mask, a developer solution S for photoresists layers exposed to actinic radiation through a mask and an immersion liquid, and/or a chemical rinse solution S for rinsing the patterned material layers.

5. The method of claim 1, wherein the potentially cationic and cationic groups are selected from the group consisting of primary, secondary and tertiary amino groups, primary, secondary, tertiary and quaternary ammonium groups, uronium-, thiouronium- and guanidinium groups, quaternary phosphonium groups and tertiary sulfonium groups; and that the potentially anionic and anionic groups are selected from the group consisting of carboxylic acid, sulfonic acid, phosphonic acid, sulfuric acid monoester, phosphoric acid monoester and phosphoric acid diester groups and carboxylate, sulfonate, phosphonates, monoester sulfate, monoester phosphate and diester phosphate groups.

6. The method of claim 1, wherein the aqueous, fluorine-free solution S comprises, based on a complete weight of the aqueous, fluorine-free solution S, from 0.0005 to 1% by weight of the ionic surfactant A.

7. The method of claim 1, wherein the aqueous, fluorine-free solution S is removed from the contact with the substrate by spin drying or drying processes employing the Marangoni effect.

8. The method of claim 1, wherein the substrate having patterned material layers having line-space dimensions of 50 nm and less and aspect ratios of >2 is obtained by a photolithographic process.

9. The method of claim 8, wherein the photolithographic process comprises:

(i) providing the substrate with an immersion photoresist layer, an extreme UV (EUV) photoresist layer, or an electron beam (eBeam) photoresist layer;

(ii) exposing the photoresist layer to actinic radiation through a mask with or without an immersion liquid;

(iii) developing the exposed photoresist layer with a developer solution to obtain a pattern having line-space dimensions of 50 nm and less and an aspect ratio >2;

(iv) applying a chemical rinse solution to the developed patterned photoresist layer; and then

(v) spin drying the substrate after the application of the chemical rinse solution;

wherein at least one of the following: the immersion liquid, the developer solution and the chemical rinse solution, is an aqueous, fluorine-free solution S.

10. The method of claim 1, which prevents pattern collapse, reduces line edge roughness, prevents and removes watermark defects, and reduces defects by removing particles.

11. The method of claim 1, wherein the patterned material layers comprise non-photoresist structures and have line-space dimensions of 32 nm and less and aspect ratios of >2.

12. The method of claim 1, wherein the aqueous, fluorine-free solution S comprises, based on a total weight of the solution S, from 0.005 to 0.8% by weight of i) the fluorine-free cationic surfactant A.

13. The method of claim 1, wherein the content of the i) fluorine-free cationic surfactant A is from 0.01 to 0.6% by weight, based on a total weight of the aqueous, fluorine-free solution S.

14. The method of claim 1, wherein the aqueous, fluorine-free solution S comprises, based on a total weight of the solution S, from 0.005 to 0.8% by weight of ii) the fluorine-free anionic surfactant A.

15. The method of claim 1, wherein the content of the ii) fluorine-free anionic surfactant A is from 0.01 to 0.6% by weight, based on a total weight of the aqueous, fluorine-free solution S.

16. The method of claim 1, wherein the aqueous, fluorine-free solution S comprises, based on a total weight of the aqueous, fluorine-free solution S, from 0.005 to 0.8% by weight of iii) the fluorine-free amphoteric surfactant A.

17. The method of claim 1, wherein the content of the iii) fluorine-free amphoteric surfactant A is from 0.01 to 0.6% by weight, based on a total weight of the aqueous, fluorine-free solution S.

18. The method of claim 1, wherein the device is an integrated circuit device, an optical device, a micromachine, or a mechanical precision device.

19. The method of claim 18, wherein the device is an integrated circuit device, which is an integrated circuit having a large-scale integration (LSI), very-large-scale integration (VLSI), or the ultra-large-scale integration (ULSI).