

BOND PAD FOR MULTI-CONDUCTOR LAYER SEMICONDUCTOR I/C CHIP

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a simple design for a bond pad for a semiconductor integrated circuit device chip having multiple interconnected conductor layers. More particularly, the present invention relates to a simple design for a bond pad for a semiconductor integrated circuit device chip, where an interconnected conducting layer underlying the conducting layer from which the bond pad is formed serves as a buffering element which deflects and dissipates the mechanical stresses formed within the semiconductor integrated circuit device chip incident to the bonding process.

2. Description of the Related Art

It is important in the production of semiconductor integrated circuit device chips, such as Large Scale Integrated (LSI) circuit device chips and Very Large Scale Integrated (VLSI) circuit device chips to provide a reliable and manufacturable mechanism whereby the electrical circuits contained within the semiconductor chip may be connected to other electrical components

external to that chip. The mechanism which is commonly used in the art to accomplish this interconnection is to bond fine wires from the semiconductor chip to an intermediate lead frame which in turn provides connections to external devices such as power supplies, current/voltage measuring devices and other semiconductor chips.

The physical structure formed within a semiconductor integrated circuit device chip surface through which an electrical connection external to the chip may be made is known as a bond pad. Bond pads are usually formed in multiple quantities on the surface of an integrated circuit device chip through intricate processes which typically involve the final metallization layer of the devices contained within that chip. Most commonly, bond pads are located along the periphery of a semiconductor integrated circuit device chip, thus providing an efficient pathway for wire bonding to a lead frame.

Typical methods for forming wire bond connections to bond pads involve the application of pressure or abrasion to the fine gold or aluminum alloy wire which interconnects the bond pad to a lead frame. Specific types of methods of bonding include compression bonding, wedge bonding and ultrasonic bonding. Coincident with the wire bonding process is the formation of substantial mechanical stress which is transmitted through the bond pad into the semiconductor integrated circuit layers which underlie the bond pad. The magnitude and intensity of the stress may be

sufficient to cause cracking localized to the semiconductor integrated circuit device structure beneath the bond pad. In turn, this cracking may lead to functionality or reliability defects within the semiconductor integrated circuit device chip.

Several aspects of bond pads, including improved designs, manufacturing methods and testing protocols have been disclosed in the art. For example, Baba, in U.S. Patent 5,172,212 teaches the manufacture and testing of a bond pad which has a barrier coating on its surface to protect the pad from corrosive elements to which it might otherwise be exposed during manufacturing and use.

More pertinent to the present invention, however, are prior art references which describe methods and materials by which the mechanical stresses incident to wire bonding onto a bond pad may be deflected or dissipated. Most methods are directed towards semiconductor integrated circuit device structures having only a single layer of metallization. These methods typically employ a bond pad bed or equivalent buffering element located beneath the bond pad. The buffering element is constructed of a material of sufficient toughness and strength to dissipate the mechanical stress induced by the bonding process, which stress otherwise may be of sufficient intensity and focus to cause a crack within the semiconductor device structure underlying the bond pad. Schematic diagrams of semiconductor integrated circuit devices which illustrate the positioning of such buffering elements are shown in

Fig. 1 and Fig. 2a.

Fig. 1 shows a cross-sectional diagram of a typical Metal Oxide Semiconductor (MOS) integrated circuit transistor device. The structures of Fig. 1 may be fabricated through manufacturing processes which are known in the art. In Fig. 1, a semiconductor layer 10 has formed within its surface a multiplicity of transistors 16. Deposited upon the semiconductor layer 10 is an insulating layer 12, which insulating layer has formed upon its surface a passivating layer 14. Also formed upon the insulating layer 12 is a bond pad 18 which may be accessed through a window in the passivating layer 14.

Upon the bonding of a bond wire 20 to the bond pad 18, substantial pressure and mechanical stress are transmitted into and through the bond pad 18. In the absence of a mechanism to dissipate or deflect this pressure and stress, a crack 22 may form from the base of the bond pad 18 and extend through both the insulating layer 12 and the semiconductor layer 10. Cracks which form in this location of a semiconductor integrated circuit device chip may provide a pathway for electrical leakage leading to deteriorated functional or reliable performance of the circuits contained within the semiconductor chip.

To inhibit crack formation and propagation incident to conventional wire bonding methods, it is known in the art to

incorporate a buffering element between the bottom portion of the bond pad 18 and the upper surface of the semiconductor substrate 10. Such a buffering element is taught by Satoh et al. in U.S. Patent 5,288,661. Fig. 2a, which illustrates the position of the buffering element, shows a schematic diagram of a semiconductor integrated circuit similar to that shown in Fig. 1. In Fig. 2a is shown a buffering element 24 disposed within the insulating layer 12 between the bottom surface of the bond pad 18 and the upper surface of the semiconductor layer 10.

Additional variations on the buffering element concept of Satoh et al. are shown Fig. 2b and Fig. 2c. In Fig. 2b, the buffering element 24 is disposed between the bottom of the bond pad 18 and the top surface of an electrical conductor 26 contained within the insulator layer 12. In Fig. 2c, the buffering element 24 has been formed from a portion of an electrical conductor 26 which has been severed. For all of the various embodiments of buffering element concepts taught by Satoh, the buffering element 24 is kept at a neutral and floating electrical potential such that any cracks which might form between the bond pad 18 and the buffering element 24 will not result in electrical functionality or reliability defects within the circuits contained within the chip.

Consistent with the buffering elements taught by Satoh et al., Ohshima, in U.S. Patent 5,365,112 also teaches the use of a buffering element beneath a bond pad in a semiconductor integrated

circuit device having a single layer of metallization. In addition, Ohshima teaches that enhanced manufacturing efficiencies for semiconductor integrated circuit devices may be obtained by using, at least in part, the same materials for fabrication of the buffering element as are used in the contact conductor metallurgy of the same integrated circuit device.

With regard to semiconductor integrated circuit device chips having multi-level metallization schemes, Tanaka et al., in U.S. Patent 5,216,280 teaches a semiconductor integrated circuit chip having multiple rows of bond pads, each of which rows is connected to the internal circuitry of the semiconductor device through a different level of conductor metallurgy. A cross-sectional diagram of the conductor layers of the semiconductor integrated circuit device of the Tanaka et al. disclosure is shown in Fig. 3.

Within Fig. 3, bond pads 31a, 31b and 31c are electrically connected respectively to conductor layers 32a, 32b and 32c. The conductor layers are constructed at varying parallel levels spaced within the depth of the semiconductor integrated circuit device through the use of stacked interconnection studs 36 which provide uniform spacing. The conductor layers 32a, 32b and 32c are separated by an interlevel dielectric material 34, and the surface of the device is covered with a passivation layer 35 through which windows have been etched to access the bond pads 31a,

31b and 31c.

Tanaka et al. also teaches the presence of a buffering layer 37 in multi-level wiring schemes. The buffering layer 37 provides a mechanism for dividing into multiple portions the vias through the interlevel dielectric material 34, which vias would otherwise have a sufficiently high aspect ratio to make them difficult to fill with the metallurgy used in the formation of the stacked interconnection studs 36. Although Tanaka et al. teaches that stresses incident upon a conductor layer may be reduced when that layer is deeply buried within a semiconductor device structure, Tanaka does not teach the extension of the buffering layer 37 to a position beneath the bond pad 31c in order to reduce stresses transmitted to the interlevel dielectric material 34 beneath the bond pad 31c upon bonding of a wire to that bond pad.

In contrast to the prior art which is directed to bond pad designs for semiconductor integrated circuit devices having either a single conductor layer or multiple levels of non-interconnected conductor layers, the problem to which the present invention is directed relates to bond pad designs for semiconductor integrated circuit device structures which have multiple levels of interconnected conductors. A cross-sectional diagram of a prior art example of such a bond pad design is shown in Fig. 4.

Fig. 4 shows a first metal layer 44, a portion of the

bottom surface of which is laminated to a conductive layer 46, such as polysilicon. A portion of the top layer of the first metal layer 44 is laminated to the bottom of a second metal layer 42. At the point of lamination of the metal layers, the top surface of the second metal layer 42 forms a bond pad 48. At points where the metal layers are not laminated, an insulating layer 45 underlies the first metal layer, an inter-metallic dielectric layer 43 is disposed between the two metal layers and a passivation layer 41 is formed upon the top surface of the second metal layer 42. A window etched through the passivation layer 41 provides access to the portion of the surface of the second metal layer 42 which serves as the bond pad 48.

The multi-conductor structure as shown in Fig. 4 presents several problems in providing a reliable and functional electrical circuit connection when a wire is bonded to the bond pad 48. A first problem is the significant step height between the surface of the bond pad 48 and the upper surface of the passivation layer 41. Due to the significant depth of the bond pad 48 within the multi-conductor structure, manufacturing problems are often encountered in removing the passivation layer 41 which resides on the sidewall surfaces 49 of the second metal layer 42 when exposing the bond pad 48. To remove the passivation layer 41 which resides on the sidewall surfaces 49, significant over-etching of the passivation layer 41 is required. This over-etching can often damage the bond pad 48 of the second metal layer 42.

A second problem pertinent to bond pad designs similar to that shown in Fig. 4 is the presence of delamination within the weaker interfaces of the structure upon application of the physical force of the wire bonding process. In particular, for bond pad designs similar to those of Fig. 4, the bottom surface of the first metal layer 44 is prone to delaminate from the upper surface of the conductive layer 46 and the upper surface of the insulating layer 45 at the points where those latter two layers meet. This delamination can cause electrical circuit functionality or reliability defects within the integrated circuit device chip within which this delamination occurs.

It is thus an object of the present invention to provide a readily manufacturable simplified bond pad design for semiconductor integrated circuit device chips having multiple interconnected conductor layers, which bond pad design is not susceptible to delamination or cracking of the materials adjoining the bond pad upon bonding of a wire to the bond pad. Although the prior art discloses bond pad designs with buffering elements for single conductor layer schemes and multiple non-interconnected conductor schemes, absent from the prior art is a disclosure of a robust bond pad design for semiconductor integrated circuit device chips having multiple interconnected metal layers.

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SUMMARY OF THE INVENTION

A first object of the present invention is to provide a readily manufacturable bond pad for semiconductor integrated circuit device chips having multiple interconnected conductor layers.

A second object of the present invention is to provide a bond pad in accord with the first object of this invention, which bond pad limits the potential for cracking within the layers underlying the bond pad when a metal wire is bonded to the bond pad.

A third object of the present invention is to provide a bond pad in accord with the first and second objects of this invention, which bond pad is not subject to interfacial delamination of the layered structure beneath the bond pad when a metal wire is bonded to the bond pad.

In accord with the objects of the present invention, a new bond pad design and its method of fabrication are provided. Fabrication of the new bond pad begins with a semiconductor substrate upon which is formed a first insulating layer which has a both a substantially flat region and region through which a plurality of via openings are formed. A first conductive layer is then formed over the surface and deposited into the plurality of

via openings of the first insulating layer. A second insulating layer, at least the top portion of which is formed from a Plasma Enhanced Chemical Vapor Deposition (PECVD) oxide material is then deposited over the first conductive layer. Similarly to the first insulating layer, the second insulating layer also has a substantially flat region and a region through which a plurality of via openings are formed to access underlying interconnected conductor layers. A second conductive layer is then formed over the surface and deposited into the plurality of via openings of the second insulating layer. Deposited upon the second conducting layer is a passivating layer having openings which define a multiplicity of bond pads on the surface of the second conductive layer. The bond pads have beneath them a vertical stack of the substantially flat region of the second insulating layer, the first metal layer and the substantially flat region of the first insulating layer.

In a second and third embodiment of the present invention, conductive contact studs and planarized metal layers are used in place of the non-planar metal layers of the first embodiment, which non-planar metal layers are formed into the via openings of their respective insulating layers. Thus, in the second embodiment of the present invention, the first insulating layer and the second insulating layer have formed, respectively, a plurality of first conductive contact studs and a plurality of second conductive contact studs formed within and through their

respective pluralities of via openings.

The bond pad constructed in accord with the present invention provides an internal buffering element which consists of the portion of the first conductive layer which resides beneath the portion of the second conductive layer from which the bond pad is formed. The buffering element portion of the first conductive layer limits cracking within those portions of the layered semiconductor integrated circuit structure of the present invention which reside beneath the bond pad when a wire is bonded to that bond pad.

The bond pad and buffering element of the present invention may be formed through simple and direct manufacturing methods. Since the buffering element and the bond pad of the present invention are formed from conductive structures within the semiconductor integrated circuit device which would otherwise be required as an integral portion of the semiconductor integrated circuit device, no additional manufacturing steps are required in fabrication of the bond pad of the present invention.

The bond pad of the present invention also allows for choice of inter-conductor insulating layers which exhibit enhanced adhesion to the conductors which they separate. With the choice of optimal inter-conductor insulating layers, adhesion of the inter-conductor insulating regions to conductive layers may be improved,

providing for limited opportunity for delamination of the layered structure underlying the bond pad of the present invention when a bond wire is bonded to that bond pad.

Finally, since the bond pad of the present invention is not deeply recessed within the surface of the semiconductor integrated circuit device chip upon which it is formed, there is only a limited need for over-etching when removing from the surface of the second metal layer those portions of the passivating material needed to form the bond pads. Under conditions of limited over-etching, only limited damage may occur to the surface of the bond pad.

From the foregoing, the bond pad design of the present invention provides a simple readily manufacturable design wherein a single conductor layer within a multiple interconnected conductor scheme of a semiconductor integrated circuit device structure may be used to provide a buffering element beneath the bond pad of that structure. The buffering element so formed provides a mechanism to deflect or dissipate the mechanical stresses associated with the bonding of a metal wire to the bond pad.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 shows a schematic cross-sectional diagram of a

semiconductor integrated circuit device structure which shows a cracking within the device structure due to bonding of a wire onto the bond pad of the device structure.

Fig. 2a to Fig. 2c show schematic cross-sectional diagrams of semiconductor integrated circuit device structures of the prior art similar to the structure of Fig. 1, wherein these devices have incorporated into their structures various buffering elements to deflect and dissipate stresses from the bonding of a wire onto the bond pad of the device structure.

Fig. 3 shows a schematic cross-sectional diagram of a semiconductor integrated circuit device structure of the prior art having stacked studs, the exposed surfaces of which serve as bond pads connected to non-interconnected conductor layers within the device structure.

Fig. 4 shows a schematic cross-sectional diagram of a semiconductor integrated circuit device structure of the prior art having a bond pads connected to multiple laminated non-interconnected conductor layers.

Fig. 5a to Fig. 5c show schematic cross-sectional diagrams of semiconductor integrated circuit device structures corresponding to the preferred embodiments of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Fig. 5a shows the first preferred embodiment of the semiconductor integrated circuit device bond pad of the present invention. Practice of the present invention begins with a semiconductor substrate upon which is formed a region to which the multi-level conductors of the present invention may be connected. In Fig. 5a this region is shown as a conductive substrate 56. The conductive substrate 56 may be formed from a conductive material such as a metal or polysilicon.

In practice, the multi-layer conductors of the present invention may, rather than being connected to the conductive substrate 56, alternatively be connected directly to semiconductor circuit device elements such as transistors, resistors, diodes and the like. Whether the multi-layer interconnected conductors of the present invention are connected directly to semiconductor circuit device elements or to conductive substrate layers is not critical to the present invention.

Deposited upon the conductive substrate 56 of the present invention is a first insulating layer 55. The first insulating layer 55 has a portion of its surface which is substantially flat and another portion of its surface which has a plurality of via

openings formed therethrough to allow connection to the underlying conductive substrate 56. The size of the via openings through the first insulating layer 55 is not critical, however, the vias must be adequately sized to readily allow filling of deposited metal into their depths.

Many materials may be used for the first insulating layer 55. Preferred insulating materials include glasses, oxide materials and nitride materials which may be deposited through deposition techniques which are known in the art. Typical deposition techniques for semiconductor thin film insulating materials include but are not limited to sputtering techniques, Chemical Vapor Deposition (CVD) techniques, plasma enhanced techniques and magnetically enhanced plasma techniques.

The most preferred material for the first insulating layer 55 of the present invention is Boro Phospho Silicate Glass (BPSG) which is preferably deposited through a CVD process with subsequent annealing. The preferred thickness of the BPSG layer is about 4000 to about 7000 angstroms.

Deposited upon the first insulating layer 55 of the present invention is a first conductive layer 54 which makes contact to the conductive substrate 56 through the via openings provided in the first insulating layer 55. Several metals and conductive materials may be used in the formation of the first

conductive layer 54 of the present invention. Metals, metal alloys and conductive metal silicides may all be used in the practice of the present invention. These conductive materials may be deposited through any of several processes which are known in the art to deposit such materials. Such deposition processes include but are not limited to sputtering techniques, thermal and electron beam assisted evaporation techniques, and vapor deposition techniques.

The first conductive layer 54 of the present invention is preferably formed from a multi-layer conductive stack consisting of a top layer of aluminum alloy deposited at a thickness of about 4000 to about 8000 angstroms. Beneath the aluminum alloy is a titanium nitride or a titanium-tungsten refractory barrier metal layer deposited at about 800 to about 2000 angstroms. Finally, the bottom most layer underlying the barrier metal layer is titanium metal deposited at about 200 to 600 angstroms. The titanium metal is preferably deposited through a sputtering process. In total, the first conductive layer 54 has a thickness of about 5000 to about 10600 angstroms.

Formed upon the first conductive layer 54 of the present invention is a second insulating layer 53. Similarly to the first insulating layer 55, the second insulating layer 53 also has a surface, a portion of which is substantially flat and another portion of which has a plurality of via openings formed therethrough to allow access to underlying conductive layers.

It is critical to the practice of the present invention that at least the upper portion of the second insulating layer 53 be formed of a material which exhibits good adhesion to a second metal layer 52 which is subsequently formed upon the surface and into the plurality of via openings of the second insulating layer 53. For the present invention the preferred material for the upper portion of the second insulating layer 53 is a dense silicon oxide layer formed through a Plasma Enhanced Chemical Vapor Deposition (PECVD) process.

Lower portions of the second insulating layer 53 may be formed of a lightly doped PECVD oxide layer or they may be formed of the same PECVD oxide layer material which was deposited for the upper portion of the second insulating layer 53. The preferred thickness of the second insulating layer 53 of the present invention is from about 4000 to about 7000 angstroms.

It is also critical to the present invention that the substantially flat portion of the second insulating layer 53 be aligned over the substantially flat portion of the first insulating layer 55. This disposition of insulating layers provides a multi-layered structure wherein a flat portion of the first conductive layer 54 will provide an interconnected buffering element beneath a flat portion of the second conductive layer 52, a portion of the top of which second conductive layer 52 forms a bond pad 58 for the

multi-layer conductors of the present invention.

Formed upon the second insulating layer 53 is a second conductive layer 52 which makes contact to the first conductive layer 54 through via openings formed in the second insulating layer 53. Analogously to the first conductive layer 54, the second conductive layer 52 may be formed from several metals and metal alloys through processes which are known in the art to deposit those conductive materials. The second conductive layer 52 preferably comprises an aluminum alloy layer of about 4000 to about 10000 angstroms formed upon the second insulating layer 53.

The last layer of the present invention is the passivation layer 51, which is deposited upon the surface of the multi-layer structure described within this invention after the second conductive layer 52 has been deposited. A contact window which is etched through the passivation layer 51 provides access to the surface of the second conductive layer 52 which will serve as a bond pad 58. Neither the thickness nor the composition of the passivation layer 51 is critical to the present invention. However, the passivation layer 51 of the present invention is typically formed from a phospho-silicate glass/silicon nitride material.

A second preferred embodiment of the present invention is shown in Fig. 5b. The second preferred embodiment is analogous to

the first preferred embodiment, with two exceptions. The first exception is that the first conductive layer 54 and the second conductive layer 52 are no longer formed, respectively, into via openings through the first insulating layer 55 and the second insulating layer 53. Rather, in the second preferred embodiment of the present invention contact between the conductive substrate 56 and the first conductive layer 54 is made through a first conductive contact stud 60 formed within and through the first insulating layer 55. Analogously, contact between the first conductive layer 54 and the second conductive layer 52 is made through a second conductive contact stud 62 formed within and through the second insulating layer 53.

The second exception relates to the first exception. Since the second embodiment provides a first conductive layer 54 which no longer makes direct contact with the conductive substrate 56, the first conductive layer 54 need not preferably be formed of a multi-layer conductive stack having a barrier metal layer. Rather, the first conductive layer 54 of the second embodiment preferably comprises an aluminum alloy layer formed at about 4000 to about 10000 angstroms.

The use of conductive contact studs formed within and through insulating layers to connect conductive layers which are separated by those insulating layers is well known in the art. The multi-layered semiconductor structure that results from using such

studs has a higher degree of planarity than the layered structure formed in the absence of studs.

Several metals, metal alloys and conductive materials may be used for forming conductive contact studs through insulating materials which separate adjoining conductor layers. Commonly used in the art are tungsten contact studs, aluminum contact studs and polysilicon contact studs. Conductive contact studs may be formed from other conductive materials provided that: (1) methods may be developed for efficiently depositing the conductive material from which the stud is formed into the via opening formed through the insulating material, and (2) methods may be developed for removing any excess conductive material from the surface of the insulating material after the stud material has been deposited into the via opening.

For the present invention, both the first conductive contact stud 60 and the second conductive contact stud 62 are preferably formed from tungsten metal. Tungsten metal may be deposited through several methods which are known in the art. These methods include, but are not limited to, thermal evaporation methods, electron beam assisted evaporation methods and Chemical Vapor Deposition (CVD) methods.

The tungsten metal for the first conductive contact stud 60 and the second conductive contact stud 62 of the present

invention is preferably deposited through a Chemical Vapor Deposition (CVD) method. The thickness of tungsten metal to be deposited in the formation of these studs corresponds to the thicknesses of the insulating layers into which the studs are formed.

A third preferred embodiment of the present invention is shown in Fig. 5c. Fig. 5c shows a cross-sectional schematic diagram of a semiconductor integrated circuit device structure similar to the second preferred embodiment of the present invention, which is shown in Fig. 5b. The only difference between the second preferred embodiment of the present invention and the third preferred embodiment of the present invention is the stacking of the first conductive contact stud 60 beneath the second conductive contact stud 62 in the third preferred embodiment of the present invention. Within the second preferred embodiment of the present invention, the first conductive contact stud 60 and the second conductive contact stud 62 are staggered.

Conductive contact studs of the third preferred embodiment of this invention provide a semiconductor structure which uses more efficiently the available surface area of the semiconductor wafer upon which the studs are formed.

What is claimed is:

1. A semiconductor device comprising:

a semiconductor substrate;

a first insulating layer formed upon the semiconductor substrate;

the first insulating layer having a first region which is substantially flat and a second region having a plurality of via openings formed therethrough;

a first conductive layer formed over the first insulating layer and deposited into the plurality of via openings formed through the first insulating layer;

a second insulating layer formed over the first conductive layer, at least the top portion of the second insulating layer being formed from a Plasma Enhanced Chemical Vapor Deposited silicon oxide;

the second insulating layer having a first region which is substantially flat and a second region having a plurality of via openings formed therethrough;

a second conductive layer formed over the second insulating layer and deposited into the plurality of via openings formed through the second insulating layer, the second conductive layer making electrical contact with the first conductive layer; and

a passivation layer, the passivation layer having openings formed therethrough which define a plurality of bond pads on the surface of the second conductive layer, the bond pads having beneath them a vertical stack of the first region



of the second insulating layer, the first conductive layer, and the first region of the first insulator layer.

2. The semiconductor device of Claim 1 wherein the first insulating layer is formed from a material chosen from the group of materials consisting of glasses, oxide materials and nitride materials.

3. The semiconductor device of Claim 2 wherein the first insulating layer is formed from Boro Phospho Silicate Glass.

4. The semiconductor device of Claim 1 wherein the thickness of the first insulating layer is from about 4000 to about 7000 angstroms.

5. The semiconductor device of Claim 1 wherein the first conductive layer is formed from a multi-layer conductive stack consisting of a top aluminum alloy layer, a middle refractory barrier metal layer and a bottom titanium metal layer.

6. The semiconductor device of Claim 5 wherein the thickness of the first conductive layer is from about 5000 to about 10600 angstroms.

7. The semiconductor device of Claim 1 wherein the thickness of the second insulating layer is from about 4000 to about



7000 angstroms.

8. The semiconductor device of Claim 1 wherein the second conductive layer comprises an aluminum alloy layer.

9. The semiconductor device of Claim 8 wherein the thickness of the aluminum alloy layer is from about 4000 to about 10000 angstroms.

10. A method for forming a semiconductor device comprising:
providing a semiconductor substrate;
forming a first insulating layer upon the semiconductor substrate;

the first insulating layer having a first region which is substantially flat and a second region having a plurality of via openings formed therethrough;

forming a first conductive layer over the first insulating layer and depositing the first conductive layer into the plurality of via openings formed through the first insulating layer;

forming a second insulating layer over the first conductive layer, at least the top portion of the second insulating layer being formed from a Plasma Enhanced Chemical Vapor Deposited silicon oxide;

the second insulating layer having a first region which is substantially flat and a second region having a plurality



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of via openings formed therethrough;

forming a second conductive layer over the second insulating layer and depositing the second conductive layer into the plurality of via openings formed through the second insulating layer, the second conductive layer making electrical contact with the first conductive layer; and

forming a passivation layer over the second conductive layer, the passivation layer having openings formed therethrough which define a plurality of bond pad regions on the surface of the second conductive layer, the bond pad regions having beneath them a vertical stack of the first region of the second insulating layer, the first conductive layer, and the first region of the first insulator layer.

11. A semiconductor device comprising:

a semiconductor substrate;

a first insulating layer upon the semiconductor substrate;

the first insulating layer having a first region which is substantially flat and a second region having a plurality of via openings formed therethrough;

a plurality of first conductive contact studs formed into and through the plurality of via openings formed through the second region of the first insulating layer, the plurality of first conductive contact studs so formed having a plurality of exposed ends;



a first conductive layer formed over the surface of the first insulating layer and the plurality of exposed ends of the plurality of first conductive contact studs;

a second insulating layer formed over the first metal layer, at least the top portion of the second insulating layer being formed from a Plasma Enhanced Chemical Vapor Deposited silicon oxide material;

the second insulating layer having a first region which is substantially flat and a second region which has a plurality of via openings formed therethrough;

a plurality of second conductive contact studs formed within and through the plurality of via openings formed through the second region of the second insulating layer, the plurality of second conductive contact studs so formed having a plurality of exposed ends;

a second conductive layer formed over the surface of the second insulating layer and the plurality of exposed ends of the plurality of second conductive contact studs; and

a passivation layer, the passivation layer having openings formed therethrough which define a plurality of bond pads on the surface of the second conductive layer, the bond pads having beneath them a vertical stack of the first region of the second insulator layer, the first metal layer, and the first region of the first insulator layer.

12. The semiconductor device of Claim 11 wherein the first



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insulating layer is from about 4000 to about 7000 angstroms thick and is formed from a material chosen from the group of materials consisting of glasses, oxide materials and nitride materials.

13. The semiconductor device of Claim 11 wherein the plurality of first conductive contact studs is formed from a material chosen from the group of materials consisting of tungsten, aluminum and polysilicon.

14. The semiconductor device of Claim 13 wherein the plurality of first conductive contact studs is formed from tungsten.

15. The semiconductor device of Claim 11 wherein the first conductive layer comprises an aluminum alloy layer having a thickness of about 4000 to about 10000 angstroms.

16. The semiconductor device of Claim 11 wherein the plurality of second conductive contact studs is formed from a material chosen from the group of materials consisting of tungsten, aluminum and polysilicon.

17. The semiconductor device of Claim 11 wherein the second insulating layer is about 4000 to about 7000 angstroms thick.



18. The semiconductor device of Claim 11 wherein the second conductive layer comprises an aluminum alloy layer having a thickness of about 4000 to about 10000 angstroms.

19. The semiconductor device of Claim 11 wherein the plurality of first conductive contact studs and the plurality of second conductive contact studs are vertically aligned.

20. The semiconductor device of Claim 11 wherein the plurality of first conductive contact studs and the plurality of second conductive contact studs are vertically staggered.



ABSTRACT OF THE DISCLOSURE

BOND PAD FOR MULTI-CONDUCTOR LAYER SEMICONDUCTOR I/C CHIP

A semiconductor integrated circuit device chip has multiple interconnected conductive layers separated by insulating layers. The chip is fabricated by successive layering of conductive layers onto the surfaces of insulating layers. Upon the surface of the uppermost conductive layer of the chip is formed a passivation layer. Windows are etched through the passivation layer to form bond pads on the exposed surfaces of the uppermost conductive layer. Beneath the bond pads reside flat portions of underlying insulating and conductive layers. The flat portion of an underlying conductive layer serves as a buffering element to dissipate and deflect mechanical stresses which might otherwise cause cracking and delamination within the chip when a bond wire is bonded onto the bond pad.

(Fig. 5A)

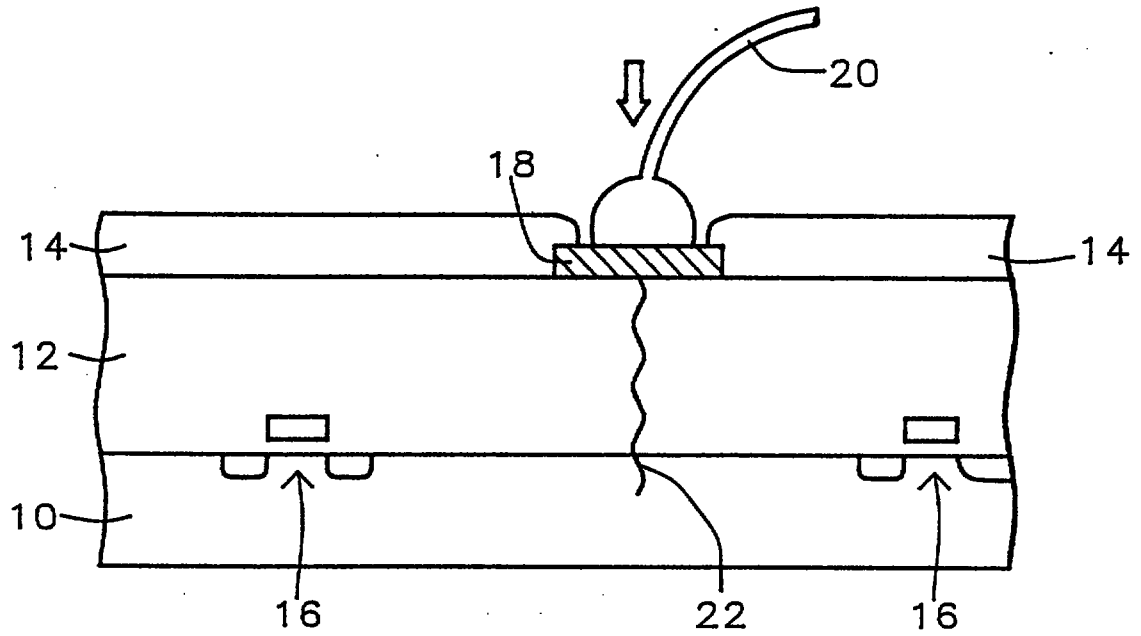


FIG. 1 - Prior Art

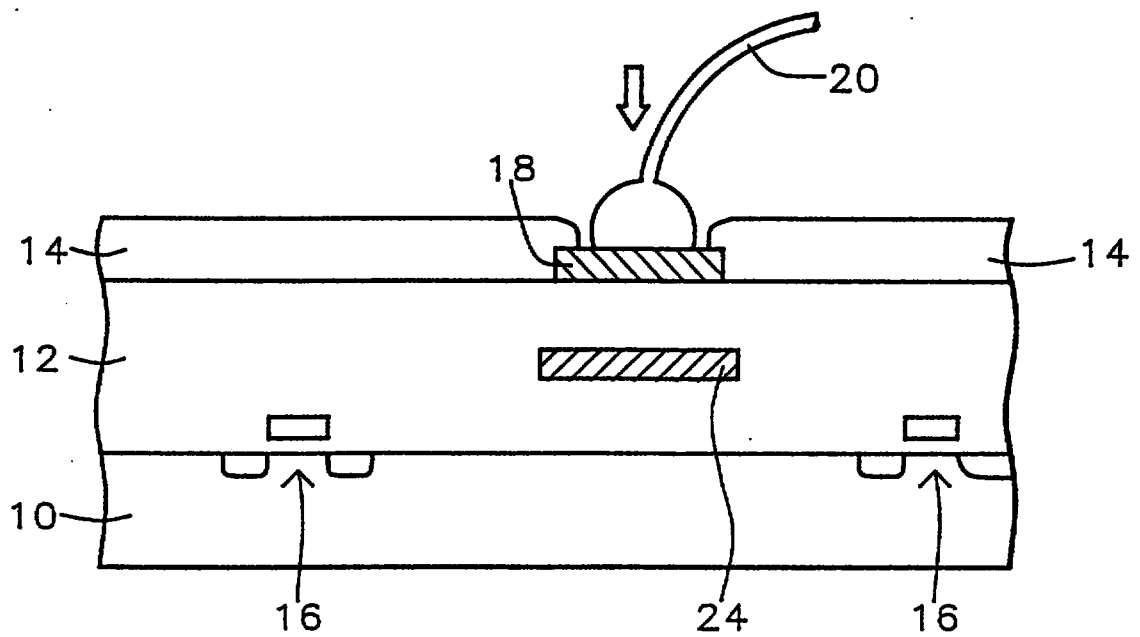


FIG. 2A - Prior Art

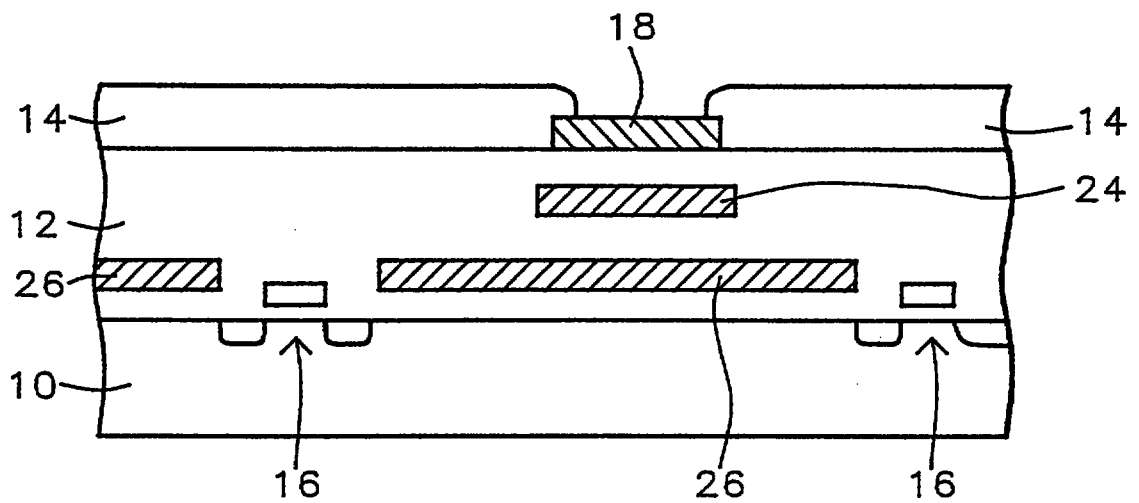


FIG. 2B - Prior Art

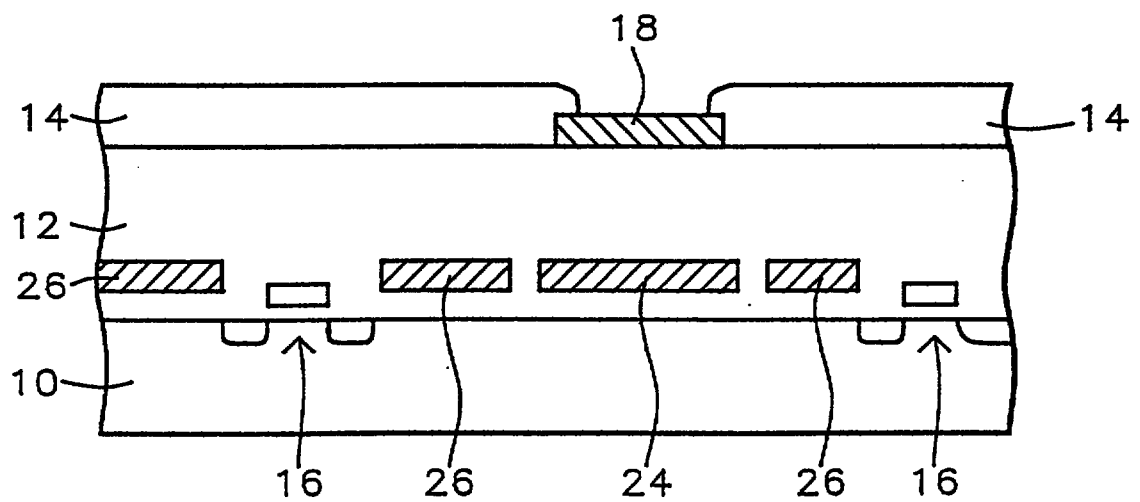


FIG. 2C - Prior Art

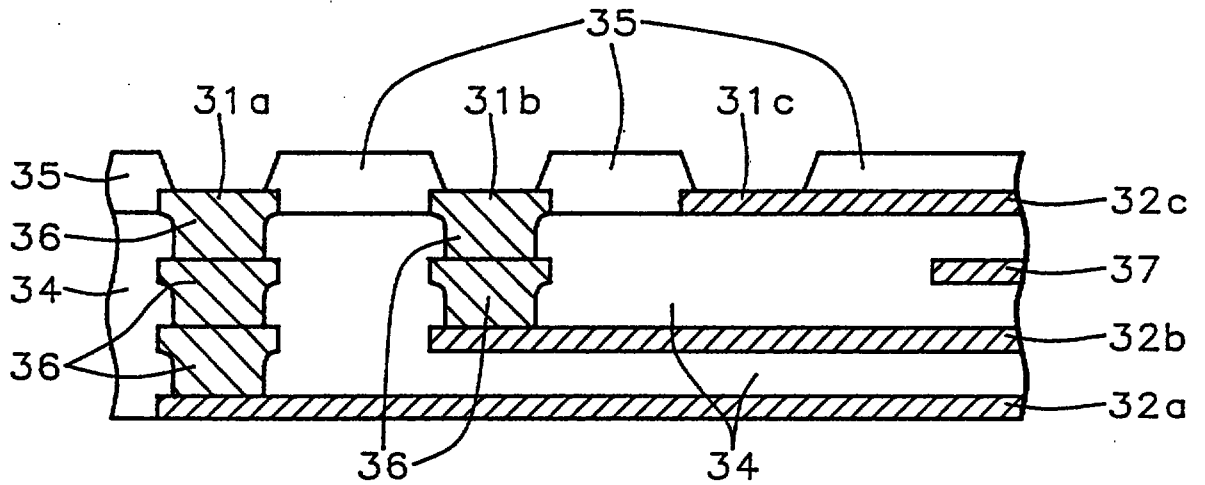


FIG. 3 - Prior Art

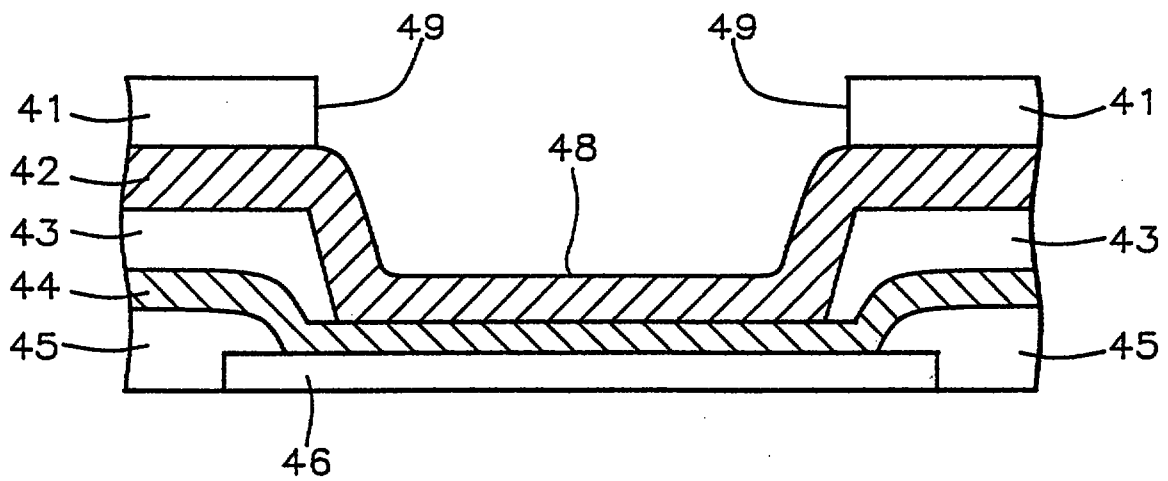


FIG. 4 - Prior Art

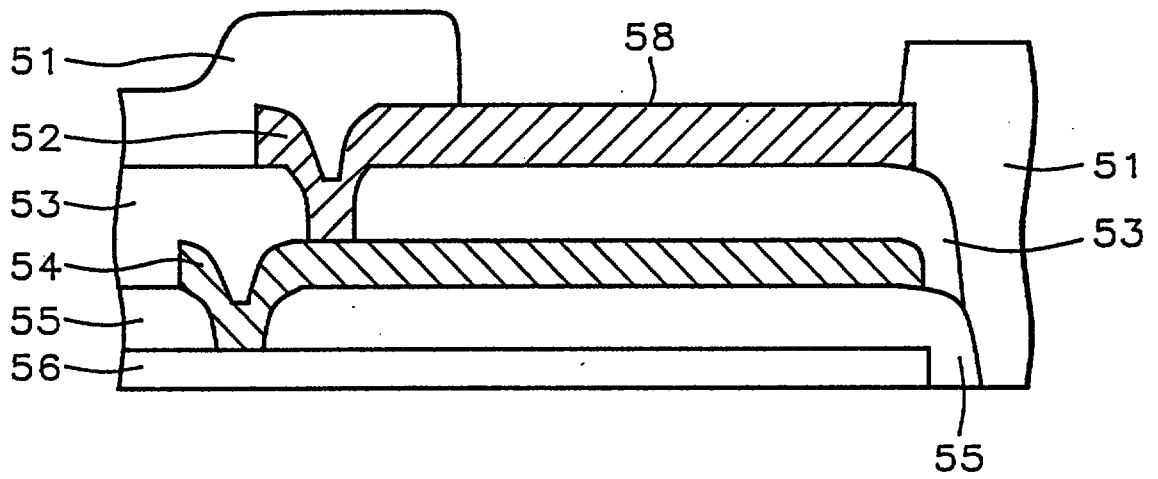


FIG. 5A

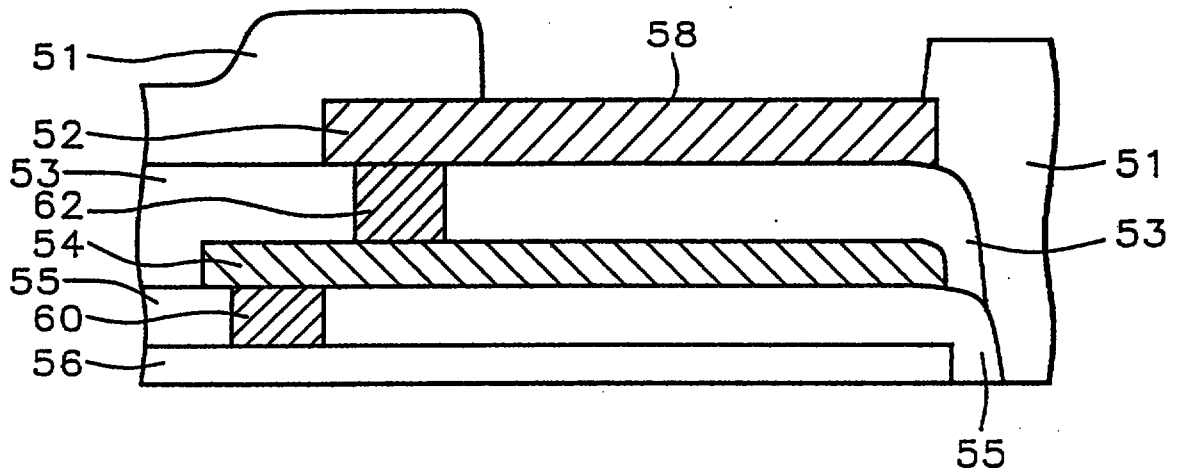


FIG. 5B

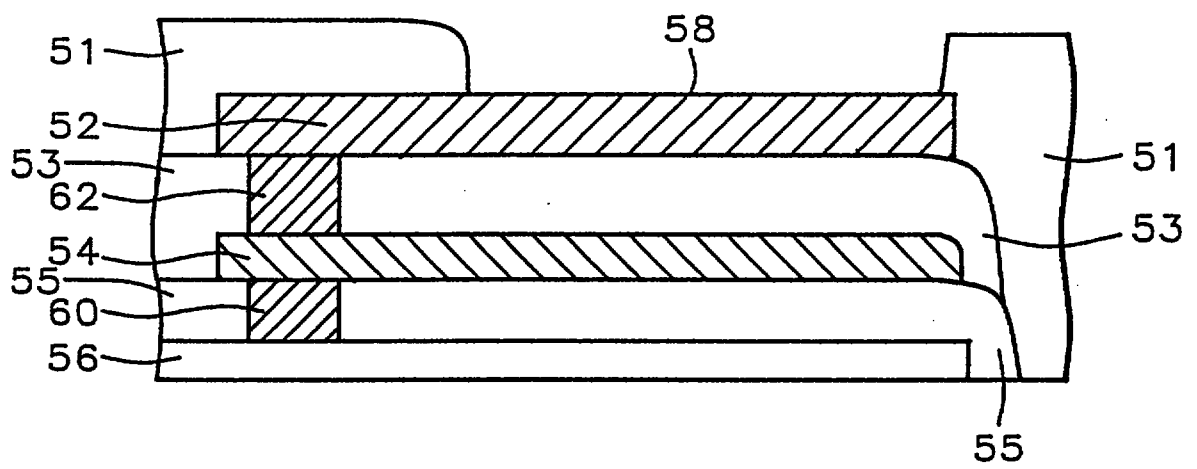


FIG. 5C

(Amended Claim 10)

10. A method for forming a semiconductor device comprising:

providing a semiconductor substrate;

forming a first insulating layer upon the semiconductor substrate, the first insulating layer having a first region which is substantially flat and a second region having a plurality of via openings formed therethrough;

forming a first conductive layer over the first insulating layer and depositing the first conductive layer into the plurality of via openings formed through the first insulating layer;

forming a second insulating layer over the first conductive layer, at least the top portion of the second insulating layer being formed from a Plasma Enhanced Chemical Vapor Deposited silicon oxide, the second insulating layer having a first region which is substantially flat and a second region having a plurality of via openings formed therethrough;

forming a second conductive layer over the second insulating layer and depositing the second conductive layer into the plurality of via openings formed through the second insulating layer, the second conductive layer making electrical contact with the first conductive layer; and

forming a passivation layer over the second conductive layer, the passivation layer having openings formed therethrough which define a plurality of bond pad regions on the surface of the second conductive layer, the bond pad regions having beneath them a vertical stack of the first region of the second insulating layer, the first conductive layer, and the first region of the first insulating layer;

bonding a bond wire to a bond pad region within the plurality of bond pad regions, wherein there is inhibited cracking of integrated circuit layers formed beneath the bond pad region.

