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(54) PACKAGING OF ELECTRONIC ELEMENTS E.G. SEMICONDUCTOR IC CHIPS

(71) We, HITACHI, LTD., a Japanese Company of 1-5-1 Marunouchi, Chiyoda-ku, Tokyo, Japan, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed to be particularly described in and by the following statement:-

This invention relates to a packaging structure for an electronic element such as a semiconductor IC chip and a method of packaging such an element.

A variety of packaging structures have been used for the purpose of sealing IC chips. Of those structures, the dual inline type glass-sealed structure (hereinafter written for brevity as DIL-G structure) is very widely used since it is inexpensive, reliable and simple in configuration in comparison with the other sealing structures.

The DIL-G structure is as shown in cross-section in Fig. 1 of the accompanying drawings and is assembled as follows. A ceramic base 1 is heated to soften a layer of glass 2 which has a low melting point and is applied to the base 1. To the ceramic base 1 are adhered discrete bracket-shaped lead frames 3 and an IC chip 4. The bonding pad electrodes of the IC chip 4 are connected with the corresponding lead electrodes of the lead frames 3 by fine metal wire 5. The structure thus assembled is capped with a ceramic cap 6 and sealed with glass 2a of low melting point.

Since the DIL-G structure uses discrete bracket-shaped lead frames 3, special jigs for supporting the lead frames 3 in the specific desired positions are needed and therefore the assembly process is complicated and also requires many operational steps.

In order to reduce the production cost of an IC by reduction of labor costs and by automation in the assembly process of such a DIL-G structure, a DIL-G structure has been proposed which uses a lead frame 3*a* consisting of a plurality of flat leads coupled together as shown in Fig. 2, instead of discrete bracket-shaped lead frames 3 as shown in Fig. 1. However, this DIL-G structure shown in Fig. 2 has the following drawback. After the sealing step, the leads of the lead frame 3*a* are to be bent according to the predetermined specification. During the bending step, it sometimes happens that gaps are formed between the leads and the low melting point glass 2, 2*a* used as sealing agent or that cracks are formed in the glass 2, 2*a* as shown in Fig. 3. Accordingly, the sealing efficiency of the glass layer is reduced so that the seal is unreliable.

By the present invention it is possible to provide a packaging structure for an electronic element such as a semi-conductor IC chip which has a high reliability, is free from the above mentioned drawback and is adapted for automatic sealing.

According to this invention there is provided a packaging structure for an electronic element comprising,

a) upper and lower sealing substrates, at least one of which has said electronic element mounted thereon;

b) a glass sealing layer disposed between opposing peripheral surfaces of said sealing substrates and recessed from at least portions of the side edges of said upper and lower sealing substrates, said electronic element being sealingly enclosed by said glass layer and said sealing substrates; and

c) lead members embedded in said glass layer and extending through said layer at locations where the layer is recessed from said side edges of the sealing substrates, said lead members being electrically connected with said electronic element.

In another aspect this invention provides a method of packaging an electronic element, comprising the steps of,

(a) applying a glass layer on opposing peripheral surfaces of upper and lower sealing substrates, said layer being recessed from

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at least portions of the side edges of said substrates,

(b) mounting an electronic element and lead members on the surface of said lower sealing substrate to which the glass layer is applied, said lead members extending outwardly beyond the outer edge of said lower substrate,

(c) electrically connecting said lead members with said electronic element,

(d) mounting the upper sealing substrate on said lower sealing substrate so that the glass layers on said upper and lower substrates are opposite, and

(e) heating said glass layers so as to seal said lead members between said upper and lower sealing substrates, the resultant glass sealing layer being recessed from at least those portions of the side edges of said upper and lower sealing substrates at which the lead members extend outwardly through the glass layer.

The following is a description of embodiments of this invention, which are given by way of example, and is to be read in connection with the attached drawings, in which:

Figs. 1 to 3 shown in cross-section previously proposed packaging structures as discussed above;

Fig. 4 shows in cross-section a semiconductor IC package according to this invention;

Figs. 5 and 7 are plans of ceramic bases used as a part of a package according to this invention;

Figs. 6 and 8 are bottom views of ceramic caps used as a part of a package according to this invention; and

Fig. 9 is a plan of a lead frame used in a package according to this invention.

In Fig. 4, reference numeral 11 indicates a ceramic base; 12, 12*a* glass of low melting point; 13 a lead frame; 14 a semiconductor IC chip; 15 bonding wire, e.g. fine metal wire; 16 a ceramic cap; and 17 jigs for supporting the semiconductor IC when the leads of the lead frame 13 are bent.

The illustrated method of mounting the semiconductor IC according to this invention will be described below. On the opposing surfaces of the ceramic base 11 and the ceramic cap 16 of the package is applied a mixed solution of glass consisting of glass powder, a solvent such as aluminium acetate and a binder such as cellulose, the glass mixture having a low melting point and a predetermined viscosity and being applied to a thickness of 0.2 - 0.3 mm. After sintering treatment, a ceramic base 11 and a ceramic cap 16 having respectively the layers 12, 12*a* of low melting point glass are produced as shown in Figs. 5 and 6. In this case, the edges of the glass layers 12 and 12*a* are recessed by less than about 0.1 mm from the edges of the base 11 and cap 16 from between which the leads of the lead frame 13 extend. This configuration is essential for the reason that the ends of the glass layers 12 and 12*a* should be recessed from the outer edges of the sealing substrates (i.e. the ceramic base 11 and cap 16) so as to ensure that it does not extend beyond the edges of the base 11 and the cap 16 when the base 11, the cap 16 and the lead frame 13 are bound by the low temperature melting glass 12 and 12*a*. There are obviously numerous variations to the way in which this result is achieved, requiring only that the glass layers are recessed from at least part of the edges of the sealing substrates. For example, it is possible not to apply the glass 12 and 12*a* only to those portions of the ceramic base 11*a* and cap 16*a* where the lead frame 13 is to be located, as shown in Figs. 7 and 8.

The ceramic base 11 having the low temperature melting glass layer 12 of the above-mentioned shape is subjected to heat treatment and the lead frame 13 and the semiconductor IC chip 14 are fastened to the ceramic base 11 through the softening of the glass layer 12 by heat. The bonding pads of the semiconductor chip 14 are connected respectively with the corresponding lead electrodes of the lead frame 13 by fine metal wires 15 such as aluminium wire. The ceramic cap 16 is sealingly fastened to this structure by means of the low temperature melting glass 12*a*.

As shown by Fig. 4, the semiconductor IC sealed within the ceramic base 11 and ceramic cap 16 is then supported by the jigs 17 and the flat lead electrodes are bent. The unwanted portions of the lead frame 13 are removed by cutting so that a semiconductor IC assembly is completed.

With this arrangement therefore, the ends of the glass layers 12 and 12*a* do not extend beyond the edges of the ceramic base 11 and the ceramic cap 16, so that the jigs 17 can be set in position without touching the glass layers 12 and 12*a*, no matter what shapes the glass layers may have, when the leads are bent. Therefore, no harmful external force is exerted to the exposed surfaces of the glass layers 12 and 12*a* so that cracks and/or gaps are not formed in them and the glass layers 12 and 12*a* are not broken. Accordingly, the hermetic seal is not degraded and a semiconductor IC having a high reliability can be obtained.

Moreover, since the illustrated semiconductor IC package can use an initially flat lead frame 13 consisting of a plurality of lead electrodes coupled together as shown in Fig. 9, the mounting process can be completely automatized, resulting in the reduction in labor and production cost.

WHAT WE CLAIM IS:-

1. A packaging structure for an electronic element comprising,

a) upper and lower sealing substrates, at

a least portions of the side edges of said substrates,

(b) mounting an electronic element and lead members on the surface of said lower sealing substrate to which the glass layer is applied, said lead members extending outwardly beyond the outer edge of said lower substrate,

(c) electrically connecting said lead members with said electronic element,

(d) mounting the upper sealing substrate on said lower sealing substrate so that the glass layers on said upper and lower substrates are opposite, and

(e) heating said glass layers so as to seal said lead members between said upper and lower sealing substrates, the resultant glass sealing layer being recessed from at least those portions of the side edges of said upper and lower sealing substrates at which the lead members extend outwardly through the glass layer.

The following is a description of embodiments of this invention, which are given by way of example, and is to be read in connection with the attached drawings, in which:

Figs. 1 to 3 shown in cross-section previously proposed packaging structures as discussed above;

Fig. 4 shows in cross-section a semiconductor IC package according to this invention;

Figs. 5 and 7 are plans of ceramic bases used as a part of a package according to this invention;

Figs. 6 and 8 are bottom views of ceramic caps used as a part of a package according to this invention; and

Fig. 9 is a plan of a lead frame used in a package according to this invention.

In Fig. 4, reference numeral 11 indicates a ceramic base; 12, 12*a* glass of low melting point; 13 a lead frame; 14 a semiconductor IC chip; 15 bonding wire, e.g. fine metal wire; 16 a ceramic cap; and 17 jigs for supporting the semiconductor IC when the leads of the lead frame 13 are bent.

The illustrated method of mounting the semiconductor IC according to this invention will be described below. On the opposing surfaces of the ceramic base 11 and the ceramic cap 16 of the package is applied a mixed solution of glass consisting of glass powder, a solvent such as aluminium acetate and a binder such as cellulose, the glass mixture having a low melting point and a predetermined viscosity and being applied to a thickness of 0.2 - 0.3 mm. After sintering treatment, a ceramic base 11 and a ceramic cap 16 having respectively the layers 12, 12*a* of low melting point glass are produced as shown in Figs. 5 and 6. In this case, the edges of the glass layers 12 and 12*a* are recessed by less than about 0.1 mm from the edges of the base 11 and cap 16 from between which the leads of the lead frame 13 extend. This configuration is essential for the reason that the ends of the glass layers 12 and 12*a* should be recessed from the outer edges of the sealing substrates (i.e. the ceramic base 11 and cap 15) so as to ensure that it does not extend beyond the edges of the base 11 and the cap 15 when the base 11, the cap 16 and the lead frame 13 are bound by the low temperature melting glass 12 and 12*a*. There are obviously numerous variations to the way in which this result is achieved, requiring only that the glass layers are recessed from at least part of the edges of the sealing substrates. For example, it is possible not to apply the glass 12 and 12*a* only to those portions of the ceramic base 11*a* and cap 16*a* where the lead frame 13 is to be located, as shown in Figs. 7 and 8.

The ceramic base 11 having the low temperature melting glass layer 12 of the above-mentioned shape is subjected to heat treatment and the lead frame 13 and the semiconductor IC chip 14 are fastened to the ceramic base 11 through the softening of the glass layer 12 by heat. The bonding pads of the semiconductor chip 14 are connected respectively with the corresponding lead electrodes of the lead frame 13 by fine metal wires 15 such as aluminium wire. The ceramic cap 16 is sealingly fastened to this structure by means of the low temperature melting glass 12*a*.

As shown by Fig. 4, the semiconductor IC sealed within the ceramic base 11 and ceramic cap 16 is then supported by the jigs 17 and the flat lead electrodes are bent. The unwanted portions of the lead frame 13 are removed by cutting so that a semiconductor IC assembly is completed.

With this arrangement therefore, the ends of the glass layers 12 and 12*a* do not extend beyond the edges of the ceramic base 11 and the ceramic cap 16, so that the jigs 17 can be set in position without touching the glass layers 12 and 12*a*, no matter what shapes the glass layers may have, when the leads are bent. Therefore, no harmful external force is exerted to the exposed surfaces of the glass layers 12 and 12*a* so that cracks and/or gaps are not formed in them and the glass layers 12 and 12*a* are not broken. Accordingly, the hermetic seal is not degraded and a semiconductor IC having a high reliability can be obtained.

Moreover, since the illustrated semiconductor IC package can use an initially flat lead frame 13 consisting of a plurality of lead electrodes coupled together as shown in Fig. 9, the mounting process can be completely automatized, resulting in the reduction in labor and production cost.

WHAT WE CLAIM IS:-

1. A packaging structure for an electronic element comprising,

a) upper and lower sealing substrates, at

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(11)

least one of which has said electronic element mounted thereon;

b) a glass sealing layer disposed between opposing peripheral surfaces of said sealing substrates and recessed from at least portions of the side edges of said upper and lower sealing substrates, said electronic element being sealingly enclosed by said glass layer and said sealing substrates; and

c) lead members embedded in said glass layer and extending through said layer at locations where the layer is recessed from said side edges of the sealing substrates, said lead members being electrically connected with said electronic element.

2. A packaging structure according to claim 1 wherein the glass of said glass layer has a low melting point.

3. A packaging structure according to claim 1 or claim 2 wherein said lead members are bent in the direction of said lower substrate.

4. A packaging structure according to any one of the preceding claims wherein said glass layer is recessed only from portions of said side edges of the sealing substrates between which the lead members extend.

5. A packaging structure according to any one of the preceding claims wherein said glass layer is recessed by about 0.1 mm from the side edges of said upper and lower sealing substrates at the said portions where it is recessed.

6. A packaging structure according to any one of the preceding claims wherein said electronic element comprises a semiconductor chip and said upper and lower sealing substrates are made of ceramics.

7. A method of packaging an electronic element, comprising the steps of

(a) applying a glass layer on opposing peripheral surfaces of upper and lower sealing substrates, said layer being recessed from at least portions of the side edges of said substrates,

(b) mounting an electronic element and lead members on the surface of said lower sealing substrate to which the glass layer is applied, said lead members extending outwardly beyong the outer edge of said lower substrate,

(c) electrically connecting said lead members with said electronic element,

(d) mounting the upper sealing substrate on said lower sealing substrate so that the glass layer on said upper and lower substrates are opposite, and

(e) heating said glass layers so as to seal said lead members between said upper and lower sealing substrates, the resultant glass sealing layer being recessed from at least those portions of the side edges of said upper and lower sealing substrates at which the lead members extend outwardly through the glass layer.

8. The method of claim 7 further including the step of

(f) bending said lead members whilst holding portions thereof at the vicinity of the side edges of said upper and lower substrates.

9. A packaging structure of an electronic element substantially as any herein described with reference to and as shown in Figs. 4 to 9 of the accompanying drawings.

10. A method of packaging an electronic element substantially as any herein described with reference to Figs. 4 to 9 of the accompanying drawings.

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