THIS SHEET HAS BEEN REPLACED

This Sheet Has Been Replaced

DESCRIPTION

Semiconductor Device

Technical Field:

The present invention relates to a method of isolation among devices within a semiconductor device.

Background Art:

Heretofore, in an integrated circuit employing insulated-gate field effect transistors (hereinafter, abbreviated to 'MOS transistors') or bipolar transistors (hereinafter, abbreviated to 'BIP transistors'), the isolation among the devices has been performed by applying reverse bias voltages to p-n junctions. The details are stated in, for example, "Integrated Circuit Technology (1)" (Corona Publishing Co., Ltd.) by Yanai and Nagata, p. 21 - p. 31.

On the other hand, in a logic LSI or SRAM (static RAM), attention has been riveted in recent years to the so-called BiCMOS system wherein a bipolar transistor and a CMOS transistor device (a complementary MOS transistor device composed of both n-channel and p-channel MOS transistors) are combined to exploit the features of the high speed of the former and the high density and low power dissipation of the latter, thereby to realize a logic LSI or SRAM of high speed, high density and low power dissipation. It is stated in detail in "Nikkei Electronics," August 12, 1985, p. 187 - p. 208, etc. Also in such a BiCMOS system, a device isolation method similar to the above is adopted.

Fig. 1 illustrates the fundamental sectional structure of the BiCMOS system. Shown in the figure are one n-channel MOS (nMOS) transistor, as well as one p-channel MOS (pMOS) transistor, and an n-p-n bipolar (npnBIP) transistor.

Here, letters S, G and D affixed to the nMOS or pMOS indicate the nodes of the source, gate and drain thereof, respectively, while letters C, E and B affixed

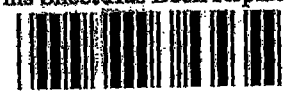
This Sheet Has Been Replaced

THIS SHEET HAS BEEN REPLACED

to the npnBIP transistor indicate the nodes of the collector, emitter and base thereof, respectively (in the following drawings, these node names shall be omitted). Besides, in the figure, diffusion layers have only the impurity types thereof written down for the sake of brevity. Accrodingl as regards portions to which the same symbols are assigned, it is merely indicated that the conductivity types are the same, and the impurity materials and impurity concentration are selected at will properly according to the purposes of the portions. Unless particularly specified, these facts hold true also in the ensuing drawings. In such a structure, with the prior art, the isolation among a large number of devices within a chip is executed by applying the lowest potential in the circuitry to a p-type substrate (p-Sub) and the highest potential in the circuitry to the n-type isolation layer (nWELL) for forming the pMOS transistor, whereby the junctions of various parts are prevented from falling into the condition of forward bias. That is, with the prior art, in a case where the circuitry operates between a supply voltage (for example, 5 V) and the earth (0 V), the devices are isolated by applying 0 V to the substrate p-Sub and 5 V to the n-type isolation layer. Since, in such a system, the applied voltage to the substrate p-Sub or to the n-type isolation layer is selected at the lowest voltage required for the device isolation, reverse bias voltages to be applied to the p-n junctions can be rendered small, and therefore it is possible to cope with the problems of lowering in the breakdown voltages of devices, etc. attendant upon the future microminiaturization of the devices. On the other hand, however, a problem to be stated below arises.

Since the input or output terminal of the LSI is directly connected with an external circuit, noise above the supply voltage or below 0 V (in general, surge noise

This Sheet Has Been Replaced



THIS SHEET HAS BEEN REPLACED

such as overshoot or undershoot) might arrive. Since the input or output node is connected to the diffusion layer within the chip in any form, the corresponding junction will then be forward-biased in the prior art. By way of example, when the minus surge noise is applied to the n-type diffusion layer indicated at the source S or drain D of the nMOS transistor in Fig. 1, the junction between the n-type diffusion layer and the substrate p-Sub is forward-biased, and a forward current flows from the substrate p-Sub toward the n-type diffusion layer. As a result, minority carriers (electrons in a p-type substrate) are injected into the substrate p-Sub. Since the minority carriers have a mean free path which is usually as long as several hundred μm, they reach another circuit part and incur, for example, the problem that a stored signal in a memory cell is destroyed in an SRAM or DRAM. The phenomenon of the minority carrier injection might be caused, not only at the input or output node part, but also by a circuit operation inside the chip in such a manner that the potential of the diffusion layer or of the substrate p-Sub fluctuates locally due to capacitive coupling or due to saturated operation of the bipolar transistor. It is therefore impossible to realize high performance of the BiCMOS system.

Disclosure of the Invention:

An object of the present invention is to solve the problem described above, and to provide a semiconductor device which operates stably. Another object of the present invention is to solve the problem described above, and to provide a voltage application method by which a voltage to be applied to a substrate or an isolation region is freely set according to an intended use, as well as a device structure which makes the method possible.

Further objects of the present invention will become

This Sheet Has Been Replaced

THIS SHEET HAS BEEN REPLACED

apparent from the following description of embodiments and drawings.

In the present invention, a voltage which is still negative (in general, when a p-type silicon substrate is used) or positive (in general, when an n-type silicon substrate is used) with respect to the operating voltage of circuitry is applied to a portion liable to the injection of minority carriers, for example, a substrate.

Further, in the present invention, in order to solve problems ascribable to the method of applying the voltage as stated above, for example, the problem that voltages to be applied to individual devices increase to degrade the reliability of a device of low breakdown voltage such as a microminiature device, the isolation region of MOS transistors of identical conductivity type or bipolar transistors of identical conductivity type is divided into several isolated regions, to which suitable isolation voltages are applied according to the respective uses.

Brief Description of the Drawings:

Fig. 1 is a sectional view showing a prior art, Fig. 2 is a sectional view showing the first embodiment of the present invention, Fig. 3 is a sectional view showing the second embodiment of the present invention, Fig. 4 is a sectional view showing the third embodiment of the present invention, Fig. 5 is a sectional view showing an embodiment of a CMOS structure, Fig. 6 is a sectional view showing an embodiment of a bipolar structure, Fig. 7 is a sectional view showing an embodiment of a bipolar-CMOS complex structure, Fig. 8 is a sectional view showing an embodiment of an SOI structure, Fig. 9 is a sectional view showing an embodiment of an SOS structure, Fig. 10 is a block diagram of a memory, Fig. 11 is a diagram showing an embodiment for the application of a substrate isolation voltage to a memory, Figs. 12 - 16 are sectional views

This Sheet Has Been Replaced

THIS SHEET HAS BEEN REPLACED

each showing an embodiment of a MOS dynamic memory, Figs. 17 and 18 are sectional views each showing an embodiment of a bipolar-CMOS complex dynamic memory, Fig. 19 illustrates sectional views showing an embodiment of principal steps for realizing the structure in Fig. 18, Fig. 20 is a sectional view showing another embodiment of the bipolar-CMOS complex dynamic memory, Fig. 21 is a plan view with the embodiment of Fig. 20 seen from the front surface of a chip, and Fig. 22 illustrates sectional views showing an embodiment of principal steps for realizing the structure in Fig. 21.

Best Mode for Carrying Out the Invention:

Now, the details of the present invention will be described in conjunction with embodiments.

[Embodiment 1]

Fig. 2 shows one of the basic embodiments of the present invention, in which the BiCMOS system is applied to a dynamic RAM (DRAM) employing a 1-transistor type cell as a memory cell MC.

In the figure, the sectional structures of nMOS, pMOS and npnBIP transistors and the memory cell MC are illustrated. The information of the memory cell MC is read out to a data line DL or written therein from the data line in such a way that a storage capacitance is formed between n-type diffusion layers and a plate (PL) and between the n-type diffusion layers and a p-type diffusion layer, and that charges stored in the storage capacitance are controlled by a gate WL to which a word line signal is applied. Besides, in the memory cell MC shown in the figure, the p-type diffusion layer is disposed underneath the n-type diffusion layers for storing the charges. This p-type diffusion layer serves to increase the storage capacitance, and also to shield the capacitor portion from minority carriers attributed to radiant rays such as alpha particles entering a substrate (to function as a

This Sheet Has Been Replaced



THIS SHEET HAS BEEN REPLACED

barrier to the minority carriers), thereby to reduce a soft error rate ascribable to the entry of the radiant rays. Such a structure is detailed as the HiC type memory cell in "Technical Digest of International Electron Device Meeting," 1977, pp. 287 - 290, etc. Besides, the phenomenon of soft errors is detailed in "IEEE Transaction on Electron Device," Vol. ED-26, No. 1, Jan., 1979, pp. 2 - 9, etc.

As indicated in the figure, the silicon substrate used is a p-type substrate p-Sub. This is intended to employ an npn BIP transistors of high performance and to isolate them efficiently. The impurity concentration of the substrate is usually selected on the order of 10^{14} - 10^{16} (cm^{-3}) in consideration of the collector-substrate capacitance of the BIP transistor, etc. Symbols nBL and pBL denote buried layers of comparatively high concentrations, which reduce the collector resistance of the BIP transistor so as to realize high performance and simultaneously render the resistance values of well regions nWELL and pWELL smaller so as to prevent the occurrence of a latch-up phenomenon. The latch-up phenomenon is stated in "Technical Digest of International Electron Device Meeting," 1982, pp. 454 - 477, etc. The impurity concentrations of the buried layers nBL and pBL are respectively selected on the orders of 10^{18} - 10^{20} (cm^{-3}) and 10^{16} - 10^{18} (cm^{-3}). The buried layers can be realized by, for example, a method in which they are formed in the substrate p-Sub by diffusion beforehand, followed by the epitaxial growth of silicon and by the formation of the wells pWELL and nWELL, etc., or a method in which they are formed by the implantation of ions at comparatively high energy levels into the substrate p-Sub from the front surface thereof, and the details will be stated later. Either or both of these buried layers is/are omitted for some purposes. Symbol CN

This Sheet Has Been Replaced



THIS SHEET HAS BEEN REPLACED

denotes a heavily-doped layer for lowering the resistance between the collector node C or a node V_{BB2} and the buried layer nBL. Symbols nWELL and pWELL denote regions for forming the pMOS and nMOS transistors, respectively. For this example the collector layer of the BIP transistor is made of nWELL and nBL.

In the construction thus far described, according to the present invention, a voltage which is higher or lower than the operating voltage range of the circuitry is applied as at least one of voltages for isolating the individual devices, V_{BB1} (this voltage is generally called a "substrate voltage" as it is supplied to the substrate through the regions pWELL and pBL) and V_{BB2} (generally called a "well voltage"). Whether such a voltage or voltages is/are applied as either or both of the isolation voltages, may be selected according to purposes. By way of example, under the condition that the circuitry operates between 0 V and V_{CC} (for example, 5 V), a negative voltage below 0 V is applied as the substrate voltage V_{BB1} and the voltage V_{CC} is applied as the well voltage V_{BB2}. Thus, the value of the substrate voltage V_{BB1} is set so that the substrate and the n-type diffusion layer within the region pWELL, for example, may not be forward-biased even when a minus voltage is applied from inside or outside the semiconductor device to the n-type diffusion layer by any cause, thereby making it possible to perfectly solve the phenomenon in which the minority carriers are injected into the substrate and incur the malfunction of the circuitry as the problem of the prior art. This effect is especially remarkable in the DRAM of the type storing information in the form of charges as shown in Fig. 2, but it is a matter of course that marked effects are obtained also in other devices such as a logic LSI, SRAM and ROM. Although, in the above, the well voltage V_{BB2} has been set at the

This Sheet Has Been Replaced



THIS SHEET HAS BEEN REPLACED

supply voltage V_{CC}, a similar effect can be obtained even when a voltage higher than the supply voltage V_{CC} is applied as the well voltage V_{BB2} according to purposes. Moreover, according to the present invention, the well regions pWELL and nWELL and the diffusion layers lying in contact with them are not forward-biased, so that the occurrence of the latch-up phenomenon can be prevented. Furthermore, the reduction of junction capacitances becomes possible.

Although the example employing the p-type substrate has been taken in the present embodiment, an n-type substrate may well be employed in, e. g., a case of using a p-n-p BIP transistor. It is needless to say that, on that occasion, the signs of applied voltages ought to be made opposite. In addition, although the HiC type cell has been illustrated as the memory cell, the embodiment as left intact is also applicable to cases of employing various planar type or vertical type memory cells (such as CCC and STC cells) described in "IEE PROC.," Vol. 130, pt. I, No. 3, JUNE 1983, pp. 127 - 135; "1984, 1985 International Solid-State Circuit Conference," Digest of Technical Papers; etc. It is as stated before that the DRAM is not restrictive, but that the embodiment as left intact is also applicable to other general LSIs such as SRAMs, ROMs and logic LSIs. Besides, although the voltage higher or lower than the operating voltage range of the circuitry is required in the present invention, it can be generated within the semiconductor device by any of methods described in Japanese Utility Model Registration Application No. 54-82150; or 1976 ISSCC Digest of Technical Papers," pp. 138 - 139; etc., and hence, it can also be realized without externally feeding a dedicated voltage. The substrate voltage V_{BB1} may well be applied from the rear surface of the substrate.

The embodiment thus far described has referred to

This Sheet Has Been Replaced

THIS SHEET HAS BEEN REPLACED

the method in which the voltage is uniformly applied to the substrate p-Sub or the well region nWELL within the chip, thereby to solve the problem of the prior art. Next, there will be elucidated a case where unequal isolation voltages are applied in conformity with the purposes of circuit blocks within a chip. For example, an inout circuit block as to which the injection of minority carriers is problematic or a circuit block which needs to reduce its junction capacitance has the isolation voltage higher or lower than the operating voltage range of the circuitry applied thereto as explained in connection with Fig. 2. On the other hand, in the block of the memory cell in Fig. 2, it is desired that the concentration of the p-type impurity layer forming the storage capacitance be heightened to increase the storage capacitance and also to augment the shield effect against the minority carriers created by the entry of alpha particles. It is also desired that devices be microminiaturized to attain a higher density and a higher speed. In these blocks, the breakdown voltages of the devices become lower. Therefore, the highest or lowest voltage within the operating voltage range of circuitry is applied as the isolation voltage of such a block likewise to the prior art. There will be described embodiments on a method which applies any desired voltages according to purposes in this manner, and a semiconductor structure which makes the method possible.

The techniques to be discussed hereinafter can be applied without any change, not only to LSIs of the BiCMOS system, but also to those of the conventional pMOS, nMOS or CMOS system. Therefore, various examples of applications shall be explained without sticking to the BiCMOS system.

[Embodiment 2]

This Sheet Has Been Replaced

THIS SHEET HAS BEEN REPLACED

Fig. 3 illustrates the application of the above measure to an integrated circuit of nMOS transistors. A construction in the figure is such that a p-type substrate (p-Sub) is formed therein with an n-well layer NW, in which p-well layers PW_1 and PW_2 are further formed. The nMOS transistors formed in the two p-wells and the substrate p-Sub are respectively denoted by symbols nMOS1, nMOS2 and nMOS3. In this structure, voltages V_{BB1}, V_{BB2} and V_{BB3} independent of one another can be applied to the isolation layers of the three sorts of nMOS transistors, and they can be selected at suitable voltages according to circuit uses.

On the other hand, the supply voltage V_{CC} or a voltage which is at least higher than both the voltages V_{BB2} and V_{BB3} is applied as V_{BB4} to the n-well layer NW. Although the single nMOS transistor has been shown in Fig. 3, one well usually has a plurality of nMOS transistors in each of three isolation layers.

In addition, although the two p-wells and the single n-well have been shown in Fig. 3, this embodiment is also applicable to a combination wherein a plurality of n-wells are provided and wherein one or more p-wells are designed in each of the n-wells. It is also possible to construct all the nMOS transistors in a p-well. Further, the present invention can be readily applied to a pMOS integrated circuit merely by altering the conductivity types of the substrate, wells and MOS transistors and reversing all the potential relations. The voltage V_{BB1} may be applied to the substrate either from the front surface or from the rear surface thereof.

[Embodiment 3]

Fig. 4 shows an embodiment in which the present invention is applied to an nMOS integrated circuit employing an n-type substrate. Referring to the figure, two p-wells (PW_1, PW_2) are formed in the n-type substrate (n-Sub),

This Sheet Has Been Replaced

THIS SHEET HAS BEEN REPLACED

and nMOS transistors are formed in the respective p-wells. In the illustrated construction, voltages V_{BB2} and V_{BB3} unequal to each other are applied to the respective wells PW_1 and PW_2 by applying the present invention. As these voltages V_{BB2} and V_{BB3}, the optimum voltages can be applied depending upon the circuit portions. By way of example, the ground potential GND can be applied as the voltage V_{BB3}, and a still lower voltage of -3 V as the voltage V_{BB2}. A voltage V_{BB1} to be applied to the substrate n-Sub may be the supply voltage V_{CC}, or a voltage higher than both the voltage V_{BB2} and V_{BB3}.

Although only the two p-wells each including the single nMOS transistor therein have been shown in Fig. 4, the embodiment is readily applicable to the combination between any desired number of p-wells and any desired number of nMOS transistors. On this occasion, two or more voltage values as desired may be selected for the applied voltages of the plurality of p-wells in conformity with uses. Besides, a pMOS integrated circuit can be fabricated by inverting the conductivity types of the substrate, the wells, sources and drains. At this time, positive voltages unequal to each other are applied as the voltages V_{BB2} and V_{BB3}, and the voltage GND or a voltage lower than both the voltages V_{BB2} and V_{BB3} is applied as the voltage V_{BB1}.

[Embodiment 4]

Fig. 5 illustrates an embodiment in which the present invention is applied to a CMOS (complementary MOS) structure. Referring to the figure, three n-wells (NW_1, NW_2, NW_3) are formed in a p-type substrate, and p-wells (PW_1, PW_2) are further formed in the respective n-wells NW_1 and NW_2. Thereafter, nMOS transistors (nMOS1, nMOS2, nMOS3) are respectively formed in the p-wells (PW_1, PW_2) and the substrate p-Sub. Besides, pMOS transistors (pMOS1, pMOS2, pMOS3) are respectively formed in the n-wells

This Sheet Has Been Replaced

THIS SHEET HAS BEEN REPLACED

(NW_1, NW_2, NW_3). In this construction, voltages V_{BB2}, V_{BB4} and V_{BB1} are applied to the p-type isolation layers for the nMOS transistors. On the other hand, voltages V_{BB3}, V_{BB5} and V_{BB6} are applied to the n-type isolation layers for the pMOS transistors. As three voltages V_{BB2}, V_{BB4} and V_{BB1} or as three voltages V_{BB3}, V_{BB5} and V_{BB6}, voltages of at least two values unequal to each other are applied according to circuits used. By way of example, voltages of GND (0 V) and -3 V are applied as the voltages V_{BB2}, V_{BB4} and V_{BB1}, while voltages of V_{CC} (+5 V) and $V_{CC} + \alpha$ (+7 V) are applied as the voltages V_{BB3}, V_{BB5} and V_{BB6}. In this way, the voltages as desired can be applied to the individual isolation layers of the nMOS and pMOS transistors. Although, in Fig. 5, only one MOS transistor has been shown in each of the wells, a plurality of MOS transistors may well be provided as are necessary. In addition, although the numbers of the wells are 3 as the n-wells and 2 as the p-wells in Fig. 5, they may be increased or decreased as are necessary. Further, it is to be understood that the present invention is also applicable to a construction wherein the polarities of the substrate and the wells are inverted. That is to say, p-wells are first formed in an n-type substrate and wherein n-wells are subsequently formed.

While the embodiments described above concern the construction employing only the MOS transistors, there will now be described examples in each of which the present invention is applied to an integrated circuit employing bipolar transistors or an integrated circuit having both bipolar and MOS transistors.

[Embodiment 5]

Fig. 6 illustrates an embodiment in which the present invention is applied to an integrated circuit employing bipolar transistors. Referring to Fig. 6, three n-p-n bipolar transistors (npn1, npn2, npn3) are one p-n-p

This Sheet Has Been Replaced

THIS SHEET HAS BEEN REPLACED

bipolar transistor (pnpl) are formed. In a conventional bipolar integrated circuit, a plurality of n-p-n transistors are constructed in a p-type substrate p-Sub likewise to the transistor npn3 in this figure and are fed with a common substrate voltage as a voltage V_{BB1} from the front surface or rear surface of a chip. When the magnitude of the voltage V_{BB1} is set at the lowest potential GND (0 V) in circuitry or at a still lower potential, the plurality of bipolar transistors can be isolated from one another. In the present invention, p-type isolation layers separated from the substrate p-Sub are further provided as indicated by symbols PW_1 and PW_2, and the n-p-n transistors (npnl, npn2) are formed therein. The p-layers have voltages V_{BB2} and V_{BB3} applied thereto. The values of the voltages V_{BB2} and V_{BB3} can be set independently of the voltage V_{BB1}. A voltage V_{BB4} is applied to an n-type layer (nW) for isolating the substrate p-Sub and the p-layers. When a voltage V_{BB4} (for example, equal to the supply voltage V_{CC}) is higher than the three voltages V_{BB1}, V_{BB2} and V_{BB3}, the transistors npnl, npn2 and npn3 can be perfectly isolated from one another. The p-n-p transistor (pnpl) in the figure can be constructed by employing some of layers used for forming the transistors npnl and npn2. When the conductivity types of all the layers including the substrate are reversed, unequal voltages can be applied to n-type isolation layers forming a plurality of p-n-p transistors.

[Embodiment 6]

Next, there will be elucidated an example in which the present invention is applied to the so-called BiCMOS structure having both CMOS and bipolar transistors in a chip. Fig. 7 illustrates the embodiment in which nMOS transistors (nMOS1, nMOS2, nMOS3) and pMOS transistors (pMOS1, pMOS2) are formed in a p-type substrate p-Sub

This Sheet Has Been Replaced

THIS SHEET HAS BEEN REPLACED

as in Fig. 5, and in which an n-p-n bipolar transistor (npnl) is further formed. As in the foregoing, voltages V_{BB1}, V_{BB2} and V_{BB3} can be independently set as the isolation voltages of the nMOS transistors. In addition, voltages V_{BB4} and V_{BB5} can be independently set as the isolation voltages of the pMOS transistors. The substrate voltage V_{BB1} of the transistor nMOS3 is applied to the isolation region of the bipolar transistor, but this voltage V_{BB1} can be set as an isolation voltage dedicated to the bipolar transistor in the absence of the transistor nMOS3. In addition, when a structure similar to that of the transistor npnl in Fig. 6 is incorporated in the construction of Fig. 7, isolation voltages unequal to each other can be fed to the bipolar transistors. Besides, a p-n-p transistor can be formed as in Fig. 6. Also, when the conductivity types of the substrate, the wells, the sources and drains of the MOS transistors, and the collector, emitter and base of the bipolar transistor are all inverted, a p-n-p transistor and a CMOS structure can be constructed, and the plurality of isolation voltages of the present invention can be applied to such a construction.

[Embodiment 7]

Fig. 8 shows an embodiment in which the present invention is applied to the nMOS portion of a stacked CMOS structure. The figure shows the example which is formed with nMOS transistors on the side of a substrate, and with pMOS transistors on the substrate by the so-called SOI structure wherein polycrystalline Si is grown on an insulator film. By combining such a configuration with a p-well (pW) and an n-well (nW), independent voltages V_{BB2} and V_{BB1} can be applied to the respective isolation portions of the transistor nMOS1 formed in the p-well and the transistor nMOS2 formed in the substrate p-Sub. In addition, when the conductivity types of the substrate

This Sheet Has Been Replaced

THIS SHEET HAS BEEN REPLACED

and the wells are rendered opposite, it is possible to form pMOS transistors on the substrate side and nMOS transistors on the polycrystalline Si side and to apply separate isolation voltages to the isolation portions of the pMOS transistors.

[Embodiment 8]

Fig. 9 illustrates an embodiment in which nMOS and pMOS transistors are constructed on an insulating substrate written as INSULATOR in the SOI (Silicon on Insulator) or SOS (Silicon on Sapphire) structure, and in which the present invention is applied to such a construction. On the insulating substrate, p-type Si (or n-type Si) is formed by crystal growth, whereupon an n-type (or p-type) impurity is introduced into the p-layer deeply enough to reach the substrate, thereby to isolate a plurality of p-type (or n-type) regions. The nMOS transistors are formed in the isolated p-type regions, and the pMOS transistor is formed in the n-type region. Voltages V_{BB1} and V_{BB3} are applied to the respective p-type regions in conformity with the uses of circuits, while a voltage V_{BB2} is applied to the n-type region. The numbers of the p-type and n-type isolation regions in Fig. 9 can be selected as desired, and it is also possible to employ only either pMOS transistors or nMOS transistors.

[Embodiment 9]

Thus far, the various structures for the substrate voltage isolation have been described with reference to Fig. 2 and Figs. 3 - 9. Now, there will be described embodiments in which these structures are applied to semiconductor memories.

Fig. 10 is a block diagram of any of general memories (including a dynamic RAM, a static RAM, a ROM, etc.). Symbol ADR denotes an address input, symbol CS a chip select input, symbol WE a write enable input, symbol DI a data

This Sheet Has Been Replaced

THIS SHEET HAS BEEN REPLACED

input, and symbol DO a data output. The designations of these signals are mere examples, and other designations are sometimes used.

A block I indicates an address buffer as well as a decoder and a driver. A block C indicates a control circuit and a write circuit. A block MC indicates a memory cell array. A block SO indicates a sense circuit and an output circuit. One embodiment of the present invention consists is applying the different voltage to the memory all array MC enclosed with a broken line from to the other portion.

Referring to Fig. 11, a chip which includes the two blocks isolated as in Fig. 10 has a built-in substrate bias voltage generator, and the two outputs V_{BBM1} and V_{BBM2} of the bias voltage generator are applied to the peripheral circuits other than the memory cell array, while a supply voltage V_{CC} and the ground potential GND are applied to the memory cell array as V_{BBM3} and V_{BBM4} respectively. The circuit arrangement of the substrate bias voltage generator has already been disclosed in "1976 ISSCC," pp. 138 - 139 or Japanese Patent Application Laid-open No. 51-117584. In this construction, by way of example, the isolation region (n-well) of the pMOS transistor of the peripheral circuit is fed with the voltage V_{BBM1} (+7 V) and the isolation region (p-well) of the nMOS transistor thereof with the voltage V_{BBM2} (-3 V), while the n-well of the pMOS transistor of the cell array is fed with the voltage V_{CC} and the p-well of the nMOS transistor thereof with 0 V. By supplying the voltage of large absolute values to the isolation regions of the input and output circuits in this manner, the memory becomes stable against the overshoots and undershoots of input and output signals, junction capacitances

This Sheet Has Been Replaced

THIS SHEET HAS BEEN REPLACED

(the capacitances between the sources or drains of MOS transistors and a substrate, and the capacitances between the collectors of bipolar transistors and the substrate) can be reduced, and an impurity concentration profile less prone to soft errors can be selected for the cell array. By the way, the designations of isolation voltages for use in the following embodiments shall correspond to the symbols V_{BBM1}, V_{BBM2}, V_{BBM3} and V_{BBM4} in Fig. 11 in accordance with the roles thereof.

Sectional views of embodiments of chips which are obtained for the embodiment of the chip setup in Figs. 10 and 11 will be elucidated below. Each of them illustrates the sectional structure of the portions of the input circuit and dynamic memory cell of a MOS dynamic RAM in correspondence with the prior-art example in Fig. 1. Although the memory cell is the dynamic cell here, the present invention is similarly applicable to a MOS static memory cell and a bipolar static memory cell.

[Embodiment A]

In an embodiment in Fig. 12, the nMOS transistors of an input protection circuit (an n-type diffused resistor and an nMOS diode) and an input circuit are formed in a p-well (pW), the pMOS transistor of the input circuit is formed in an n-well (nW), and a memory cell made of an nMOS transistor is formed in a p-type substrate p-Sub. In the present embodiment, the p-well of the input circuit and the substrate p-Sub are isolated. Therefc the values of the isolation voltages V_{BBM2} and V_{BBM4} of the respective regions can be independently set. Accordi by way of example, the voltage V_{BBM2} can be selected at −3 V in order to satisfy the specifications of the input circuit, and the voltage V_{BBM4} can be selected at 0 V from the viewpoint of the soft-error immunity of the memory cell. A broken line under the memory cell indicates a p-type high impurity concentration layer.

This Sheet Has Been Replaced

THIS SHEET HAS BEEN REPLACED

In this way, the disadvantage of the prior-art example elucidated in Fig. 1 can be prevented to provide a stable dynamic memory.

[Embodiment B]

In Fig. 13, only the n-type diffused resistor and nMOS diode of an input protection circuit are provided in a p-well, and the nMOS transistors of any other peripheral circuits are formed in a p-type substrate p-Sub likewise to a memory cell. Besides, a pMOS transistor can be formed in an n-well. A voltage V_{BBM2} (for example, -3 V) is applied to the p-well under the n-type diffused resistor and nMOS diode which are input protection devices, while a voltage V_{BBM4} (for example, 0 V) is applied to the substrate p-Sub of the nMOS transistors of the input circuit and the memory cell. A p-type high concentration layer is provided under the memory cell as in Fig. 12. A voltage V_{BBM1} is applied to the n-well. The present embodiment is advantageous over the embodiment of Fig. 12 in that, since only the input protection devices are provided in the well, the layout is simplified, and that, since the nMOS transistors other than the input protection diode are formed under the same concentration condition over the cell and the peripheral circuit, the control of threshold voltages V_{TH} is easy.

[Embodiment C]

Fig. 14 illustrates an embodiment in which a memory cell is formed in a p-well (pW), while the nMOS transistors of an input protection circuit and any other peripheral circuit are formed in a p-type substrate p-Sub. In the present embodiment, the p-well of comparatively high concentration is provided under the memory cell, and it acts as the substitute of the high concentration layer indicated by the broken line in Fig. 12 or 13.

[Embodiment D]

Fig. 15 illustrates an embodiment which employs

This Sheet Has Been Replaced

THIS SHEET HAS BEEN REPLACED

an n-type layer as a substrate and in which a peripheral circuit and a memory cell are formed in p-wells. Whereas the embodiments of Figs. 12 - 14 have the double well structure, a well configuration of single layer suffices in the present embodiment. A voltage V_{BBM2} (for example, −3 V) is applied to the p-well of the nMOS transistor of the peripheral circuit, while a voltage V_{BBM4} (for example, 0 V) is applied to the p-well of the nMOS transistor of the memory cell. In addition, a voltage V_{BBM1} (for example, a supply voltage V_{CC}) is applied to the substrate n-Sub. In the p-well to which the voltage V_{BBM2} is applied, only an input protection circuit may be formed, or peripheral circuits such as an address buffer may well be included.

[Embodiment E]

Fig. 16 illustrates an example in which a pMOS memory cell is formed on a p-type substrate p-Sub. A voltage V_{BBM2} (for example, −3 V) is fed to the substrate of the nMOS transistor of a peripheral circuit, and a voltage V_{BBM1} (for example, +7 V) is applied to the n-well of the pMOS transistor of another peripheral circuit, thereby to reduce the source and drain junction capacitances of the pMOS transistor. A voltage V_{BBM3} (for example, a supply voltage V_{CC}) is applied to the n-well of the memory cell. Thus, it is possible to construct a memory in which the input circuit is immune against undershoots and can attain a high speed, while the memory cell is less prone to soft errors.

[Embodiment 10]

In the above, Embodiments A - E applied to the MOS memories (SRAM, DRAM) have been described as the practicable configurations of Embodiment 9 with reference to Figs. 12 - 16. Next, embodiments in each of which the present invention is applied to a memory by the use of the BiCMOS construction of Fig. 7 having both bipolar

This Sheet Has Been Replaced



THIS SHEET HAS BEEN REPLACED

and MOS devices will be described with reference to Figs. 17 - 21. Among the embodiments, those of Figs. 17 - 19 employ epitaxial layers, and those of Figs. 20 - 22 don't employ epitaxial layers.

[Embodiment F]

Fig. 17 shows the nMOS, pMOS and n-p-n bipolar transistors of peripheral circuits, and a dynamic type nMOS memory cell as viewed from the left.

Under the nMOS memory cell, a p-type buried layer (pBL) of high impurity concentration is put to intensify the soft-error immunity. This layer pBL is also used for the isolation of an n-type buried layer.

Although the nMOS transistor of the peripheral circuit is formed in a p-well, this p-well can be omitted when a p-type epitaxial layer is employed. An n-type buried layer nBL of high concentration is provided under this p-well layer, and an n-layer (CN) of high concentratio is added for feeding a voltage to the layer nBL. Besides, the p-well has its side surrounded with an n-well thereby to be isolated from a p-type substrate p-Sub. A voltage V_{BBM2} (for example, −3 V) is applied to the nMOS transistor of the peripheral circuit, and the voltage V_{BBM1} (for example, a supply voltage V_{CC}) to the n-well of the pMOS transistor. A common voltage V_{BBM4} is applied to the isolation layer of the n-p-n bipolar transistor and that of the nMOS transistor of the memory cell. Buried layers nBL and pBL provided under a well serve to reduce the collector resistance of the bipolar transistor, and are also effective to prevent latch-up through the decrease of a substrate resistance.

[Embodiment G]

Fig. 18 illustrates an embodiment in which a memory cell is formed in a p-type substrate p-Sub, and the difference of which from the embodiment of Fig. 17 consists only in a construction under the memory cell. With

This Sheet Has Been Replaced

THIS SHEET HAS BEEN REPLACED

the construction in Fig. 17, the buried layer pBL of high concentration might rise and cause the threshold voltage V_{TH} of the nMOS transistor to fluctuate. In contrast, according to the construction in Fig. 18, a p-type high concentration layer indicated by a broken line is provided only under a storage capacitor so as to prevent the buried layer from rising to the channel part of the nMOS transistor of the memory cell.

Next, principal steps for realizing the sectional structure of Fig. 18 are illustrated in Fig. 19. At (a) in Fig. 19, n-type buried layers nBL are formed in the front surface of a p-type substrate, and at (b), a p-type buried layer pBL is further formed. Thereafter, a layer Epi is formed by epitaxial growth at (c), and n-wells (nWELL) and p-wells (pWELL) are formed in the layer Epi by steps (d) and (e). At (f), layers CN heavily doped with an n-type impurity are formed so as to connect with the underlying layers nBL. Though not shown in the drawing, the plate of a memory cell, the gates of MOS transistors, the source and drain layers of the MOS transistors, and if necessary, the emitter layer of a bipolar transistor are thereafter formed. Further, steps such as the formation of contact holes and metalizati are thereafter required. In the illustration of Figs. 17 and 18, the layers CN and nBL reduce the collector resistan of the bipolar transistor. On the other hand, the contact interfaces between the sources and drains and the wells of the MOS transistors and between the base and the collector of the bipolar transistor do not establish the contacts between layers of very high concentrations, and they can have their breakdown voltages held at degrees necessary for circuit operations.

[Embodiment H]

The above has been the example of the process employin the epitaxial layer, and embodiments which do not employ

This Sheet Has Been Replaced



THIS SHEET HAS BEEN REPLACED

the epitaxial layer will now be described with reference to Figs. 20 - 22. These embodiments form a high concentratior layer in the place of a p-type substrate at a fixed depth by the use of implantation. For this reason, they can curtail the cost of manufacture as compared with the case of employing the epitaxial layer.

Fig. 20 is a sectional view, and the corresponding conceptual diagram seen from the front surface of a chip is shown in Fig. 21. An nMOS transistor nMOS1 has its p-type isolation layer (pWELL) enclosed with an n-layer (CN or n-well), thereby to be isolated from a p-type substrate p-Sub.

The principal steps of a process for realizing the structure of Figs. 20 and 21 are shown in Fig. 22. At (a), an n-layer of high concentration is provided in a substrate p-Sub at a fixed depth from the front surface thereof by ion implantation. Thereafter, an n-well and a p-well are formed at (b) and (c). The p-well can be omitted in the case of the p-type substrate p-Sub. At (d), n-layers (CN) of high concentration are formed so as to reach the n-type buried layer nBL. Steps after (d), for forming MOS and bipolar devices and metalization are similar to conventional steps.

As described above in conjunction with many embodiments, according to the present invention, independent voltages as desired can be applied to the substrate and isolation layer of a MOS device and the isolation layer of a bipolar device, and the optimum voltages conforming to the purposes of the circuits of the devices can be selected. Thus, the setting of concentration profiles, the setting of isolation voltages, etc. can be freely done in order to cope with the problems of the undershoots of inputs and outputs, junction capacitances, and soft errors.

Industrial Applicability:

Heretofore, the injection of minority carriers

This Sheet Has Been Replaced

THIS SHEET HAS BEEN REPLACED

ascribable to surge noise etc. has arisen at a p-n junction constituting a MOS transistor or a BiP transistor formed in a silicon substrate, and it has formed the cause of such a problem as the destruction of a stored signal in an SRAM or a DRAM.

Such a phenomenon degrades the reliability of the semiconductor device and is unfavorable.

The present invention can prevent the phenomenon, is applicable to various products including MOS, BiP, CMOS, Bi-MOS and Bi-CMOS devices and is capable of enhancemen in the reliability etc., so that it can be effectively utilized.

* C L M S *

This Sheet Has Been Replaced

THIS SHEET HAS BEEN REPLACED

WHAT IS CLAIMED IS:

1. In a semiconductor device which has sources and drains of insulated-gate field effect transistors or collectors, bases and emitters of bipolar transistors within a substrate and a plurality of isolation layers isolated in the substrate; a semiconductor device characteri: in that a voltage outside a varying range of applied voltages to respective electrodes of said source and drain or said collector, base and emitter is applied to at least one of said substrate and said plurality of isolation layers.

2. In a semiconductor device which has sources and drains of insulated-gate field effect transistors or collectors, bases and emitters of bipolar transistors within a substrate and a plurality of isolation layers isolated in the substrate; a semiconductor device characteriz in that at least two unequal isolation voltages are applied to said substrate and the isolation layers which have conductivity types identical to each other, or to the plurality of isolation layers which have conductivity types identical to each other.

3. A semiconductor device having a semiconductor body, a semiconductor element includign at least one p-n junction provided in the body, power source means for the semiconductor element, and power source means for the body; characterized in that said power source means for said body supplies a voltage so as to prevent said p-n junction from being forward-biased even when an input voltage opposite in polarity to an input voltage which is originally expected as an input to said semi-conductor element has arrived.

4. A semiconductor device as defined in Claim 3, characterized in that said semiconductor body is made up of a semiconductor substrate, and an epitaxial grown layer formed on said substrate.

THIS SHEET HAS BEEN REPLACED

5. A semiconductor device as defined in Claim 3, characterized in that said semiconductor body is a semiconduct layer provided on an insulating substrate.

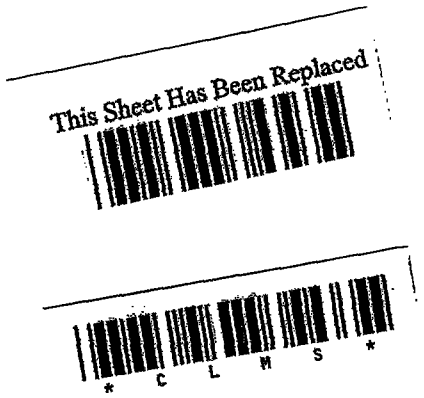
6. A semiconductor device as defined in Claim 4, characterized in that said semiconductor element includes at least a MOS transistor.

7. A semiconductor device as defined in Claim 4, characterized in that said semiconductor element includes at least a bipolar transistor.

8. A semiconductor device as defined in Claim 4, characterized in that said semiconductor element includes at least a MOS transistor and a bipolar transistor.

9. A semiconductor device as defined in Claim 3, characterized in that said semiconductor element is a semiconductor element to which an external input is applied.

10. A semiconductor device as defined in Claim 3, characterized in that said semiconductor element forms a semiconductor memory, and that said semiconductor element having said p-n junction not forward-biased is a semiconductor element to which an external input is applied.



THIS SHEET HAS BEEN REPLACED

ABSTRACT:

The injection of minority carriers into a substrate caused by potential fluctuations ascribable to noise etc. is prevented.

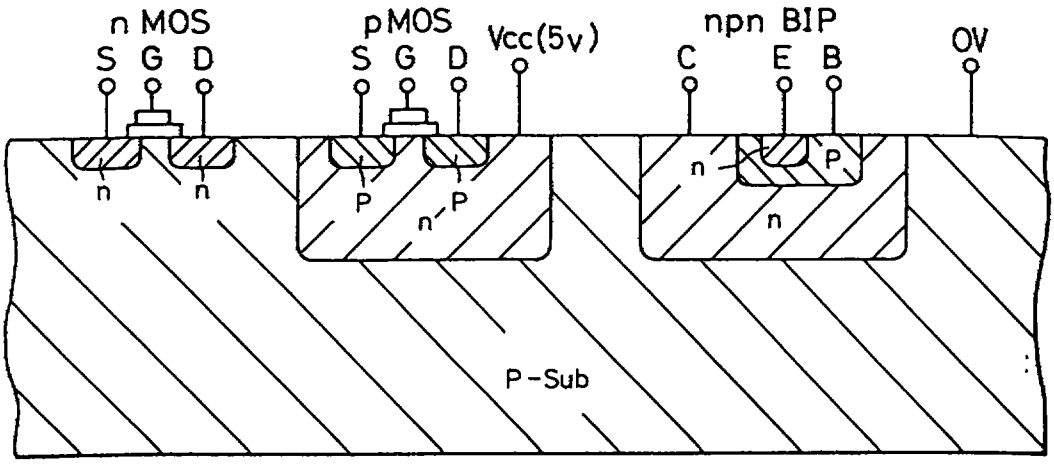
In a semiconductor device which has sources and drains of insulated-gate field effect transistors or collectors, bases and emitters of bipolar transistors within a substrate and/or a plurality of isolation layers isolated in the substrate, voltages having values outside a varying range of applied voltages to respective electrodes of the source and drain or to the collector, base and emitter are applied to the substrate and the isolation layers.

This Sheet Has Been Replaced



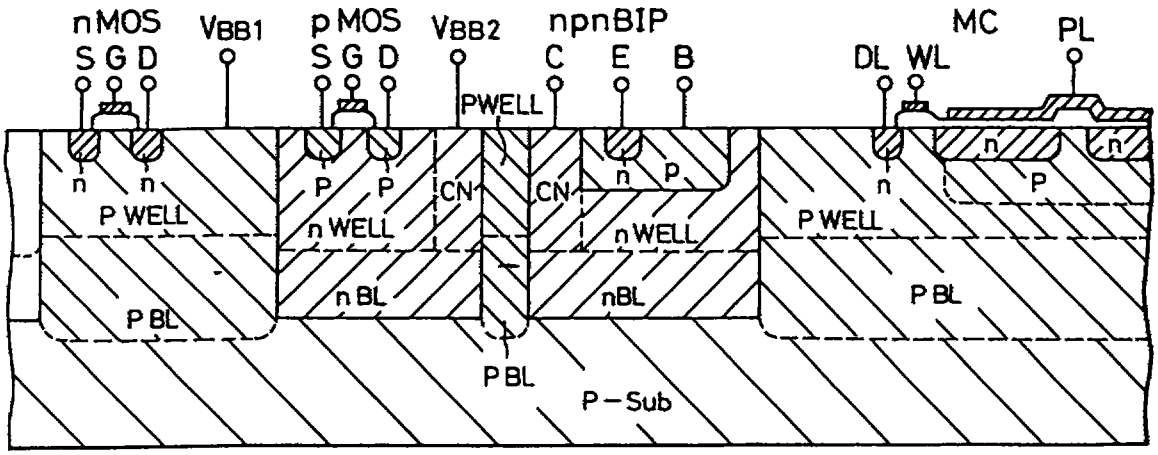
THIS SHEET HAS BEEN REPLACED

FIG. 1



This Sheet Has Been Replaced

FIG. 2



This Sheet Has Been Replaced

THIS SHEET HAS BEEN REPLACED

FIG. 3

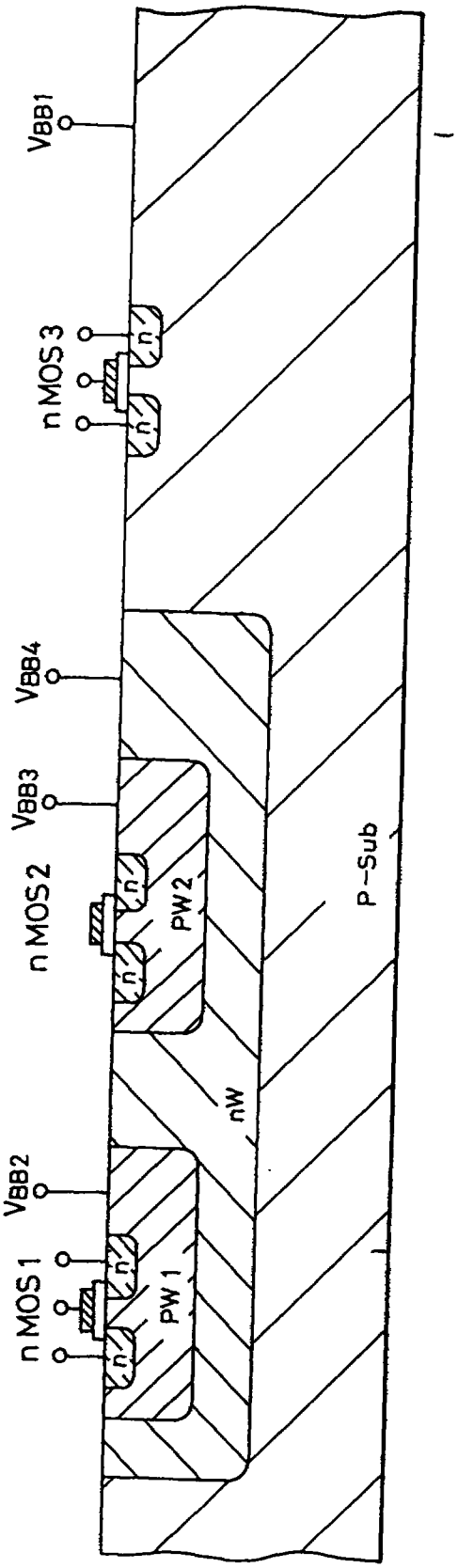
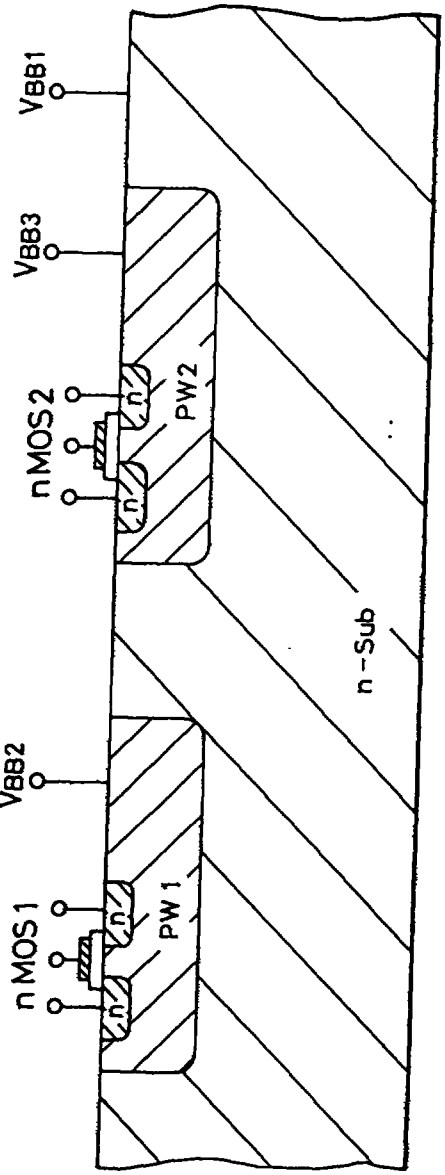


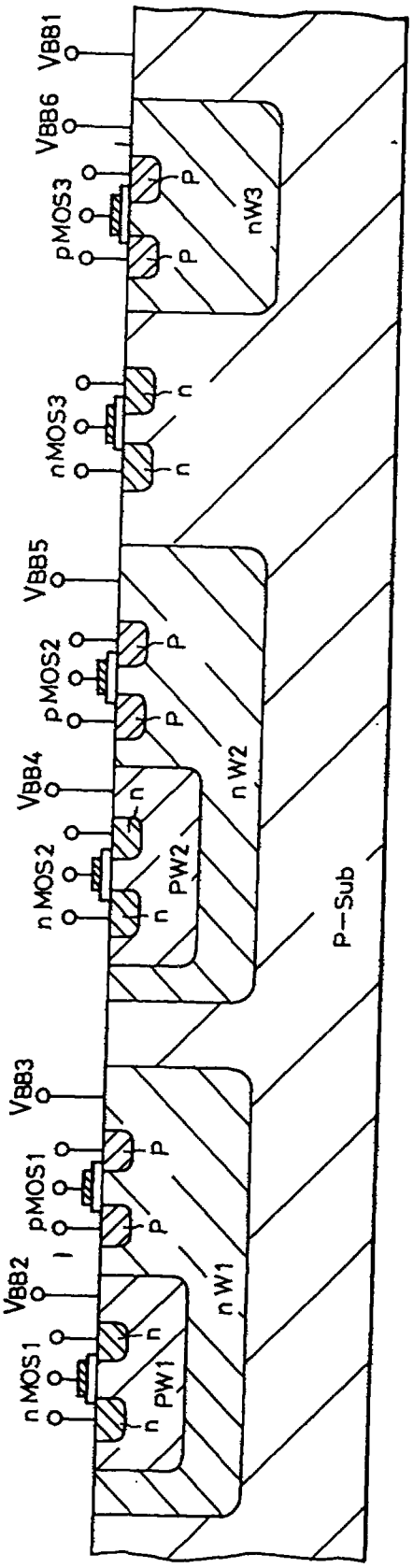
FIG. 4



THIS SHEET HAS BEEN REPLACED

This Sheet Has Been Replaced

FIG. 5



This Sheet Has Been Replaced

THIS SHEET HAS BEEN REPLACED

FIG. 6

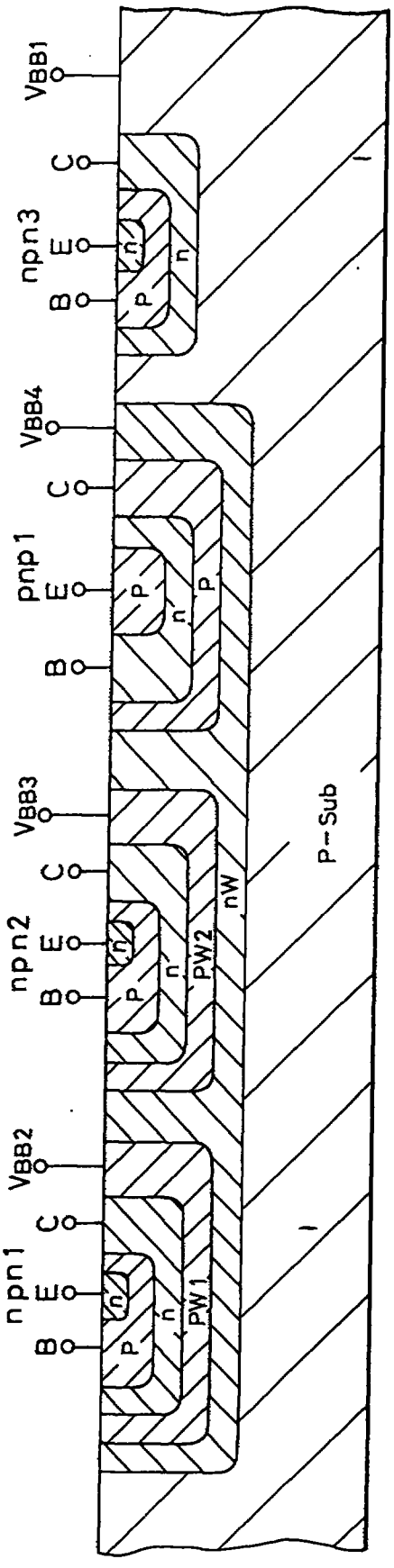
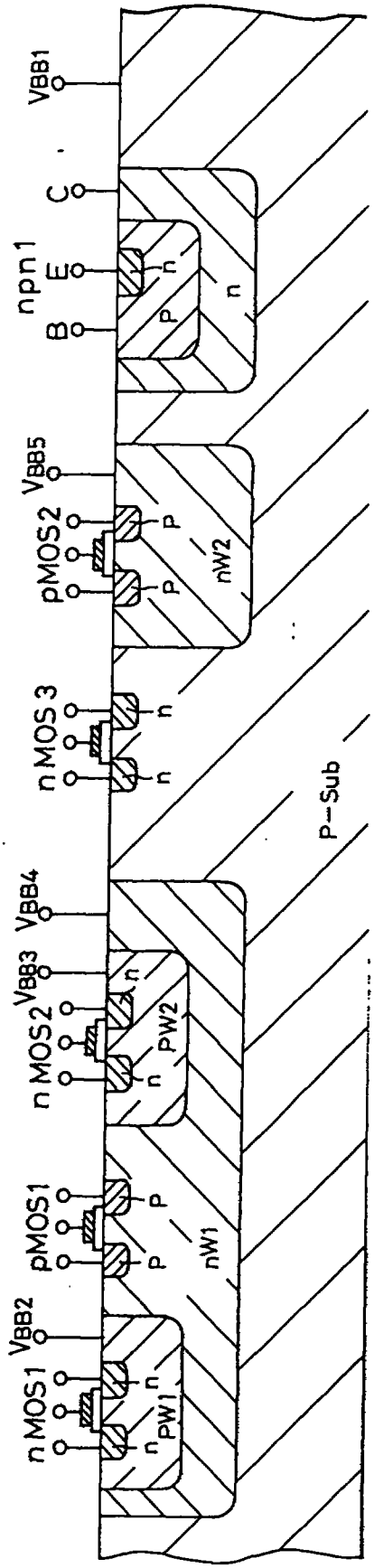
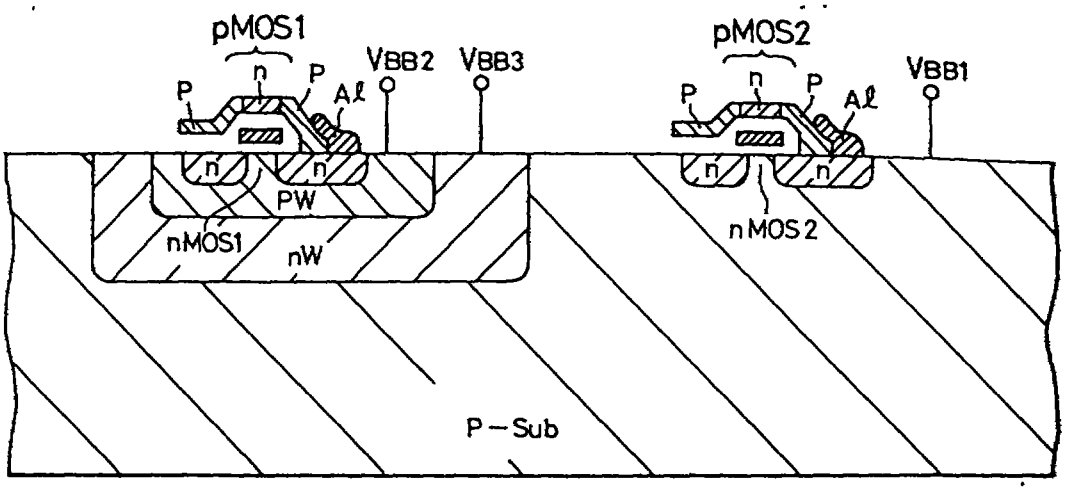


FIG. 7



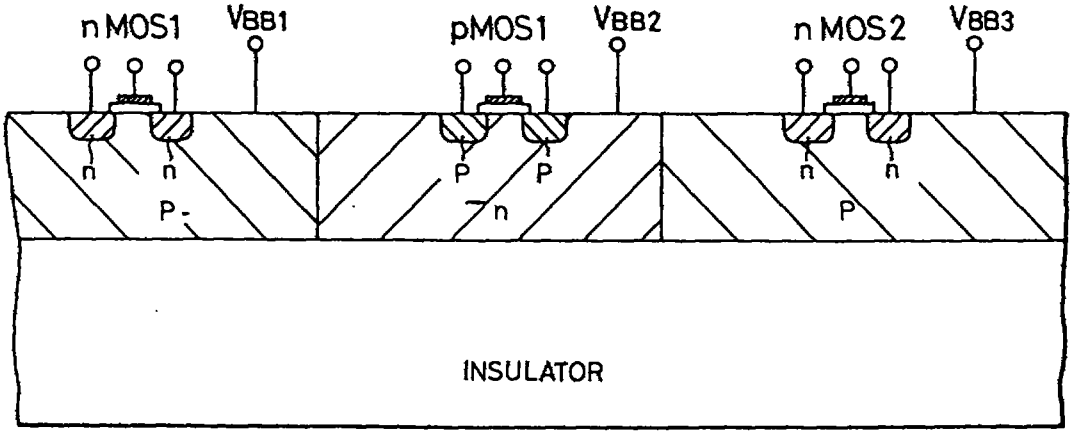
THIS SHEET HAS BEEN REPLACED

FIG. 8



This Sheet Has Been Replaced

FIG. 9



This Sheet Has Been Replaced

THIS SHEET HAS BEEN REPLACED

FIG. 10

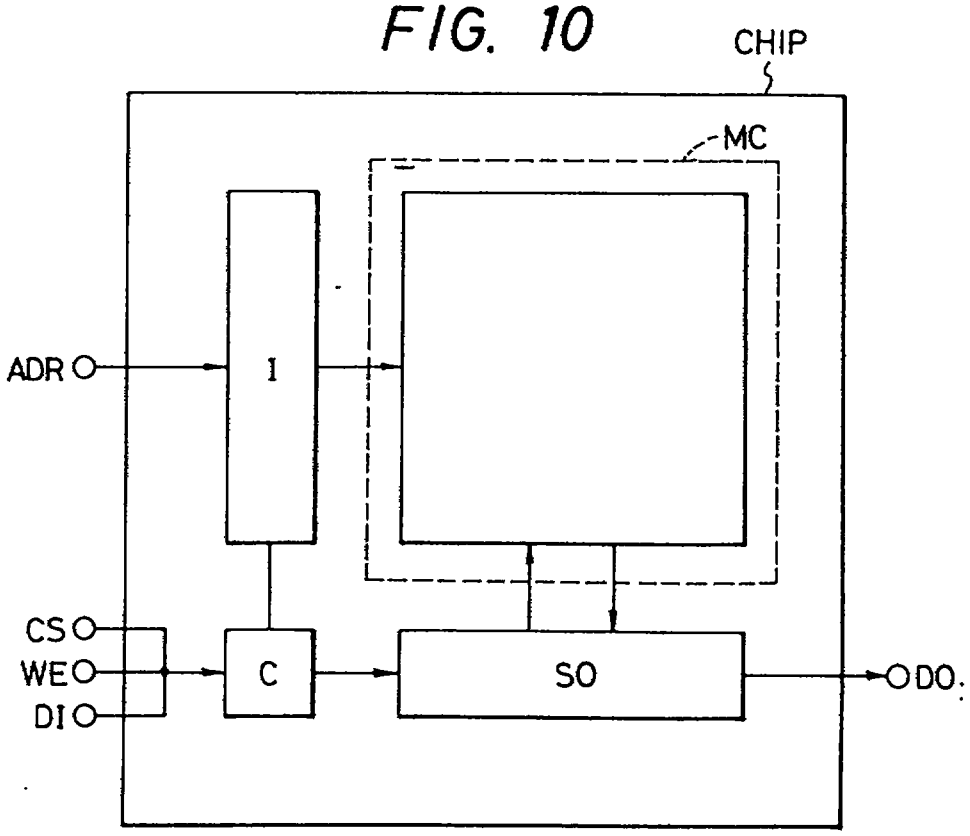
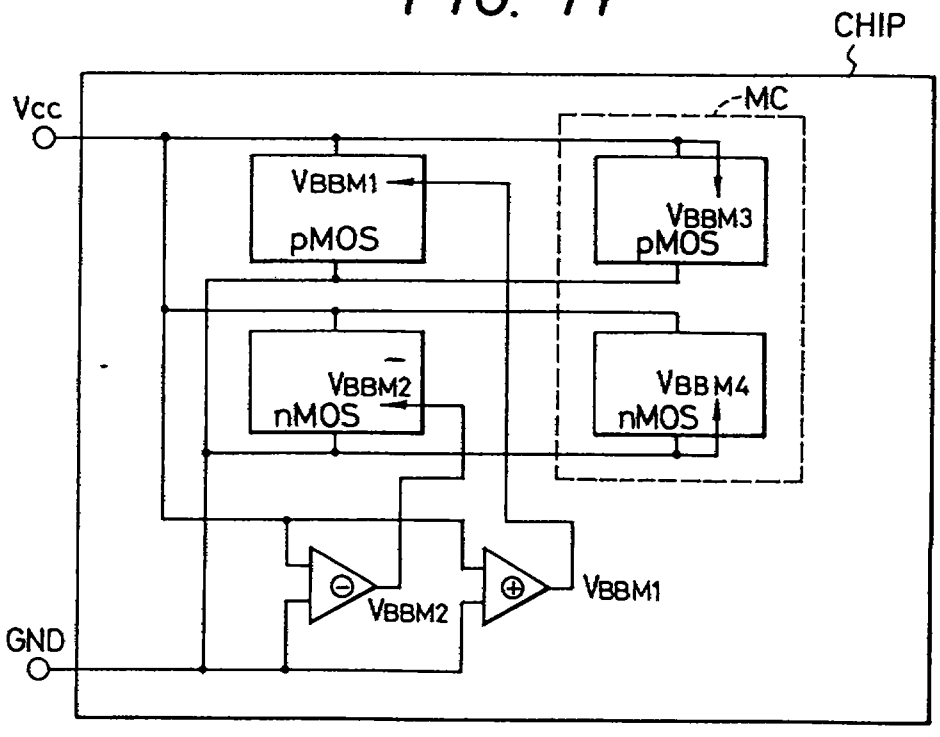


FIG. 11



This Sheet Has Been Replaced



THIS SHEET HAS BEEN REPLACED

FIG. 12

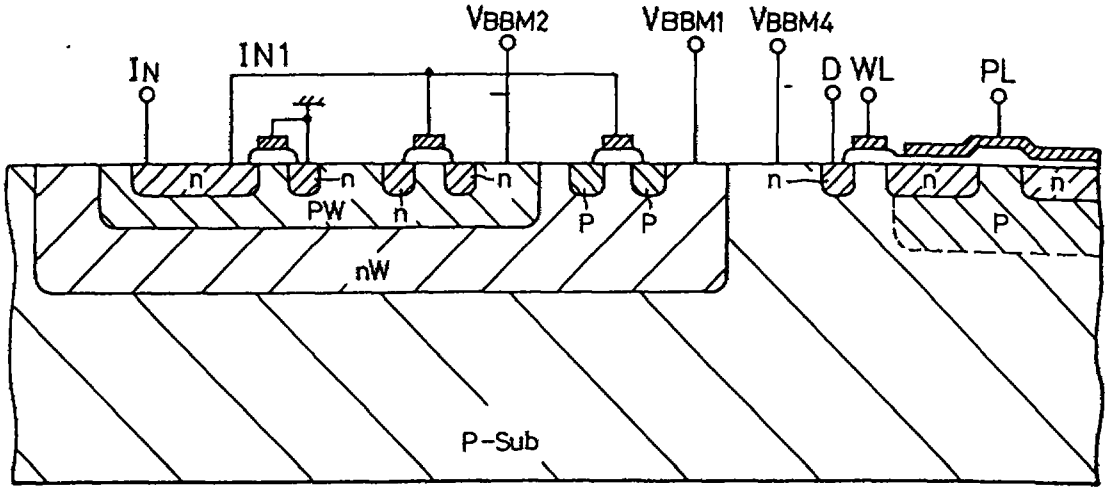


FIG. 13

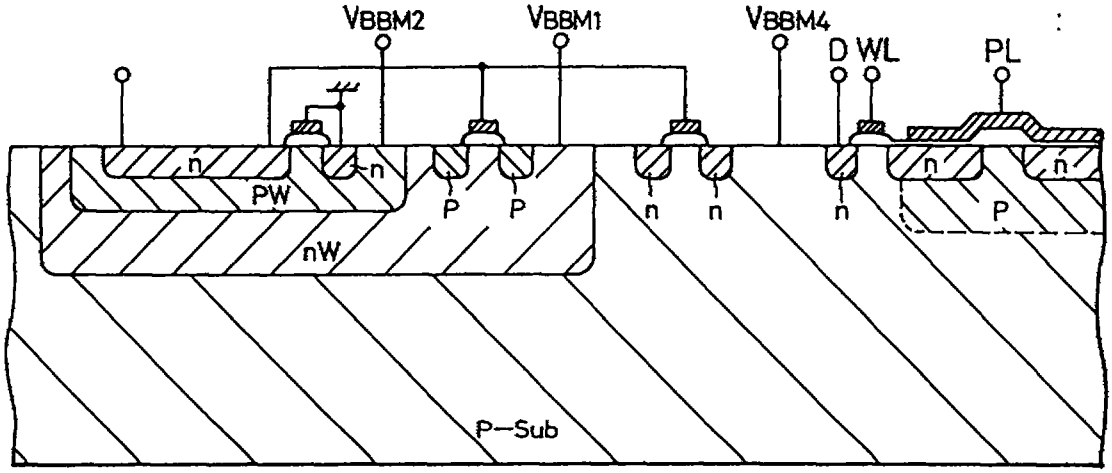
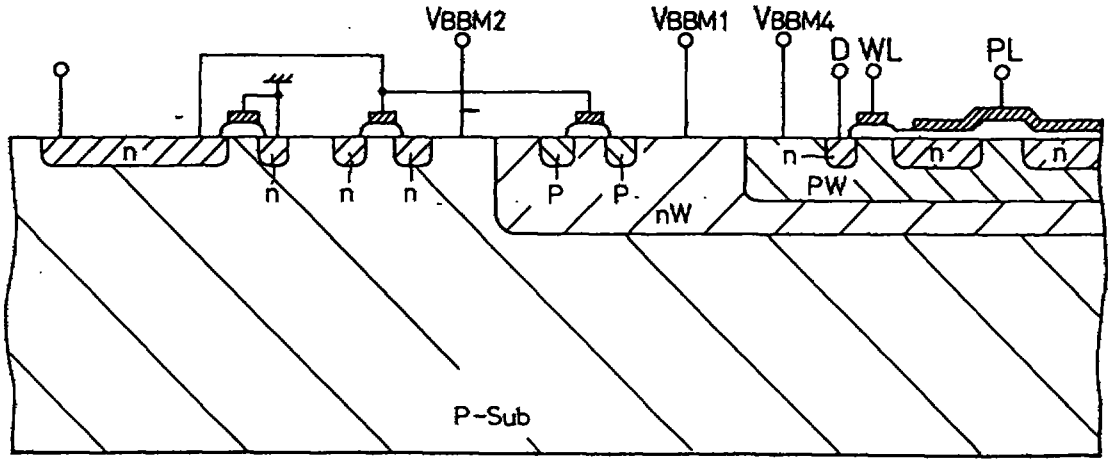
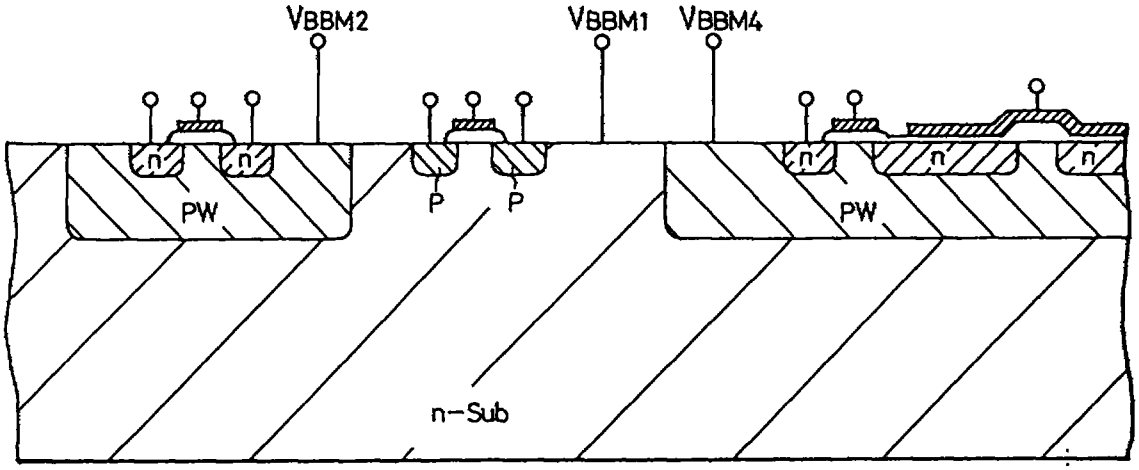


FIG. 14



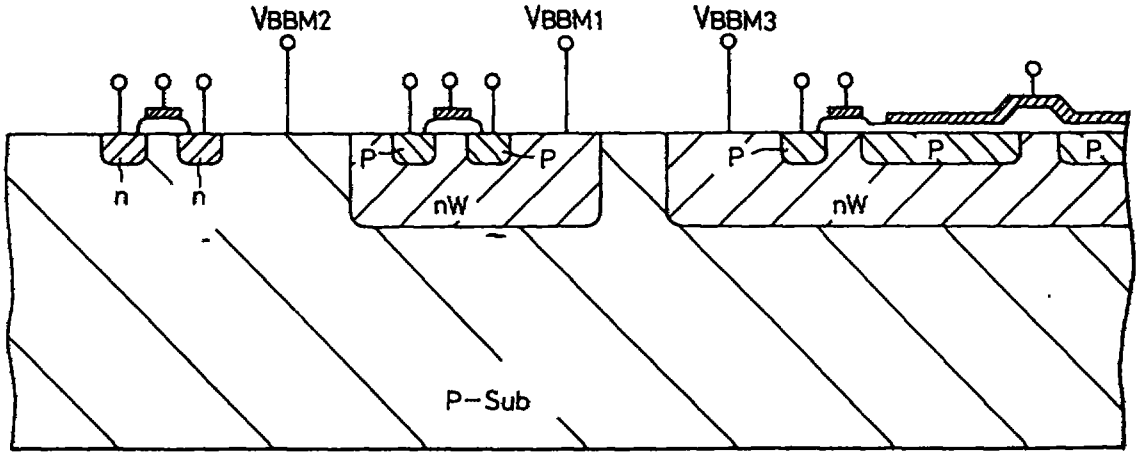
THIS SHEET HAS BEEN REPLACED

FIG. 15

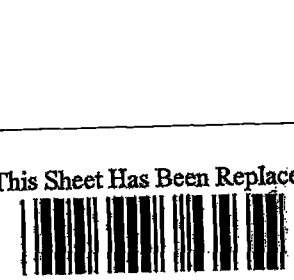


This Sheet Has Been Replaced

FIG. 16



This Sheet Has Been Replaced



THIS SHEET HAS BEEN REPLACED

FIG. 17

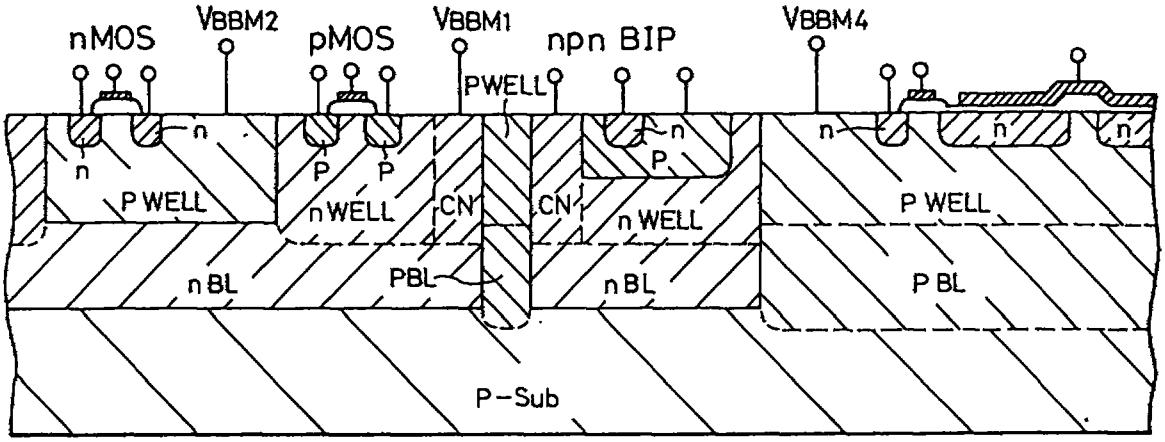
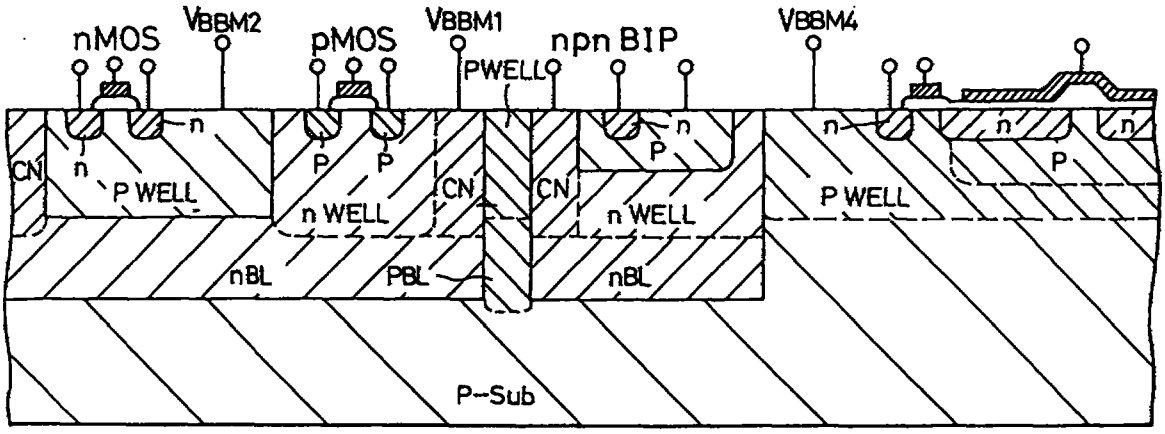
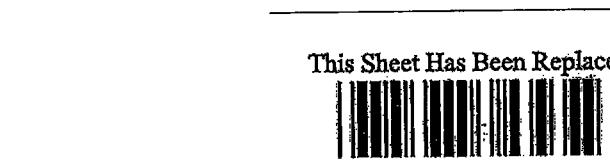


FIG. 18



This Sheet Has Been Replaced



THIS SHEET HAS BEEN REPLACED

FIG. 19

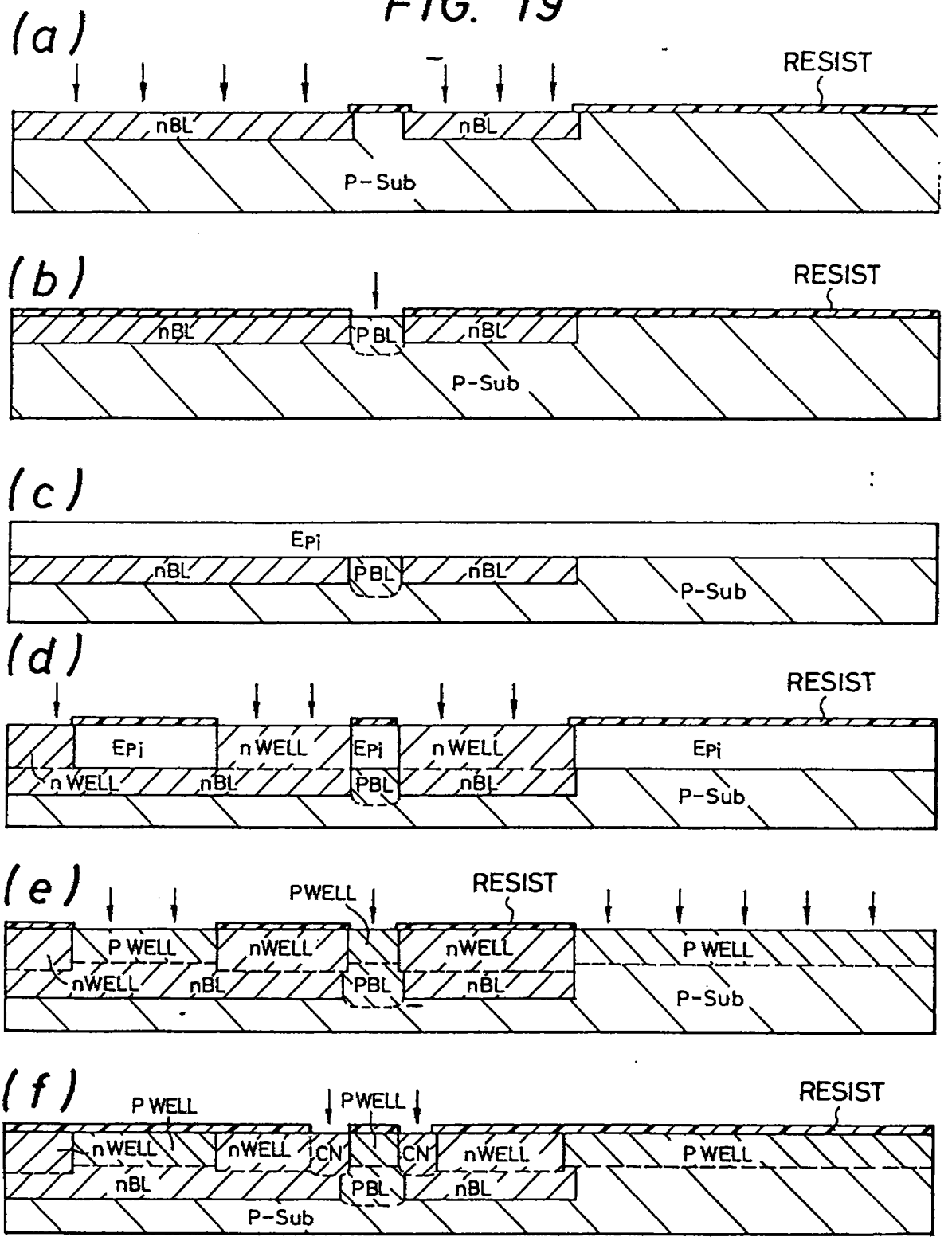


FIG. 20

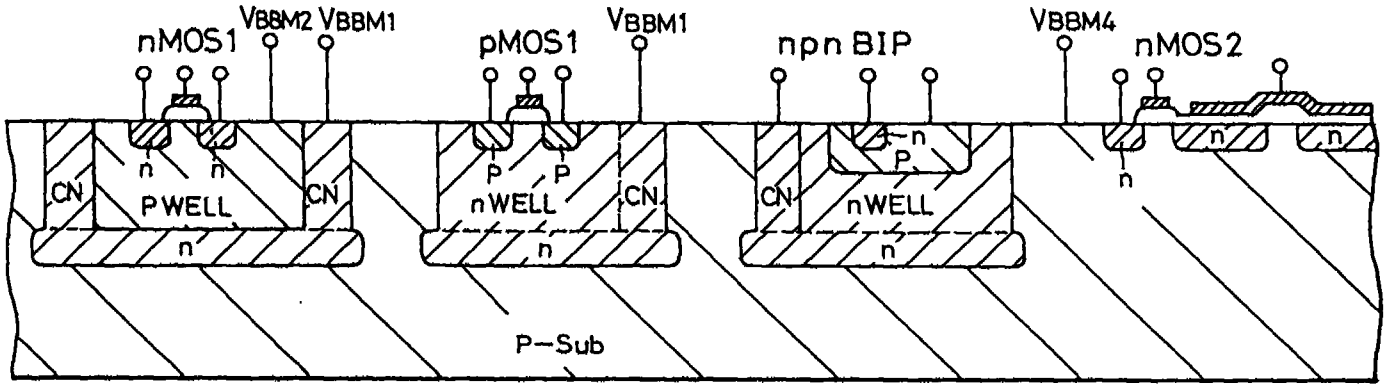
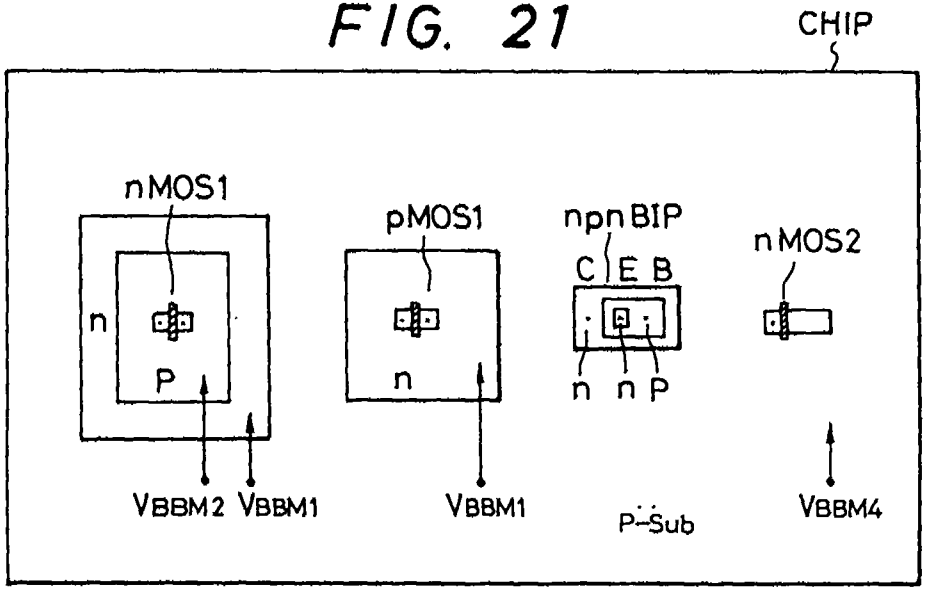


FIG. 21



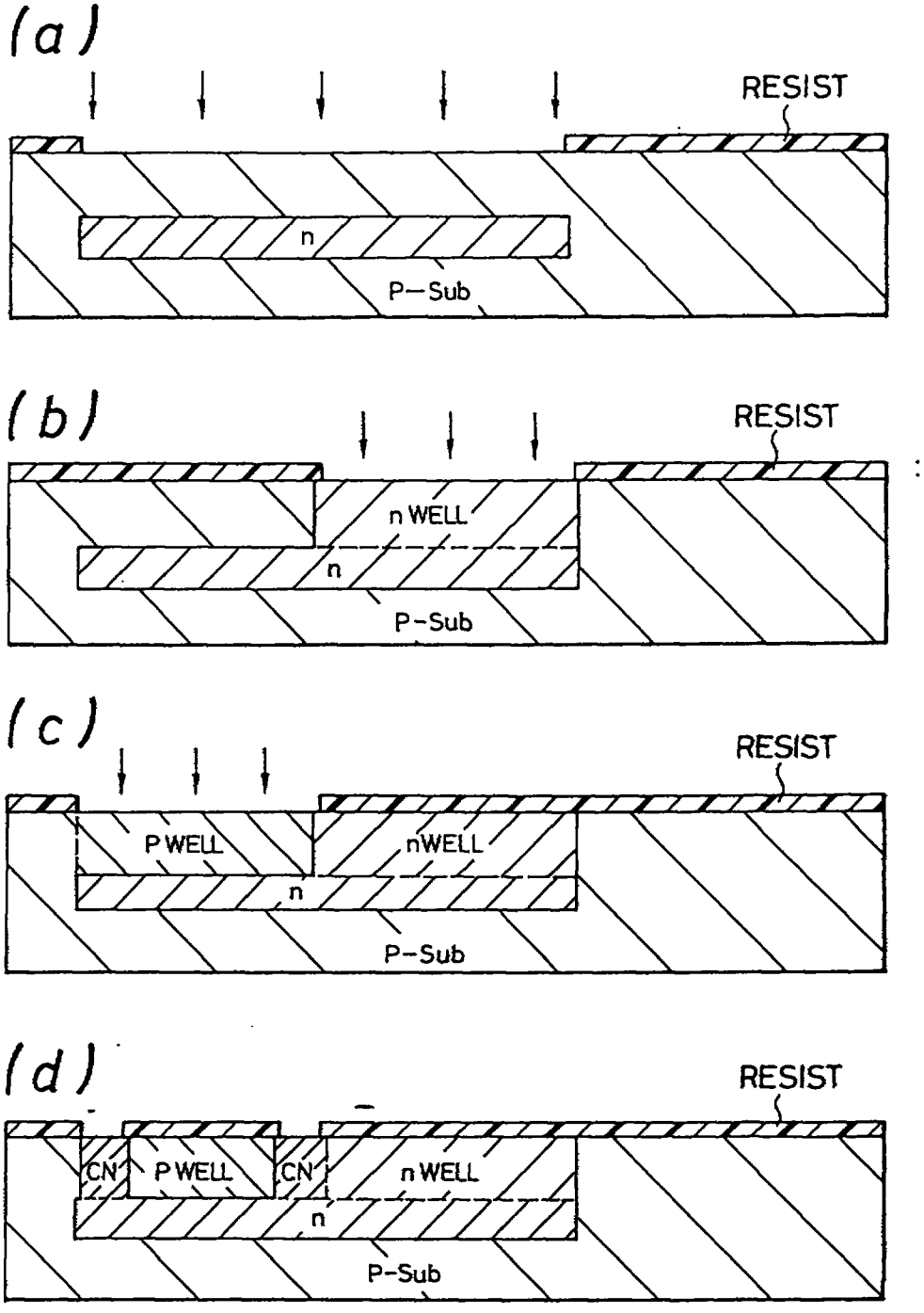
This Sheet Has Been Replaced

THIS SHEET HAS BEEN REPLACED

This Sheet Has Been Replaced

THIS SHEET HAS BEEN REPLACED

FIG. 22



960 9506-2

REPLACEMENT SHEET
28 FEB 1997

DESCRIPTION

Semiconductor Device

Technical Field:

The present invention relates to a method of isolation among devices within a semiconductor device.

Background Art:

Heretofore, in an integrated circuit employing insulated-gate field effect transistors (hereinafter, abbreviated to 'MOS transistors') or bipolar transistors (hereinafter, abbreviated to 'BIP transistors'), the isolation among the devices has been performed by applying reverse bias voltages to p-n junctions. The details are stated in, for example, "Integrated Circuit Technology (1)" (Corona Publishing Co. Ltd.) by Yanai and Nagata, p. 21 - p. 31.

On the other hand, in a logic LSI or SRAM (static RAM), attention has been riveted in recent years to the so-called BiCMOS system wherein a bipolar transistor and a CMOS transistor device (a complementary MOS transistor device composed of both n-channel and p-channel MOS transistors) are combined to exploit the features of the high speed of the former and the high density and low power dissipation of the latter, thereby to realize a logic LSI or SRAM of high speed, high density and low power dissipation. It is stated in detail in "Nikkei Electronics," August 12, 1985, p. 187 - p. 208, etc. Also in such a BiCMOS system, a device isolation method similar to the above is adopted.

Fig. 1 illustrates the fundamental sectional structure of the BiCMOS system. Shown in the figure are one n-channel MOS (nMOS) transistor, as well as one p-channel MOS (pMOS) transistor, and an n-p-n bipolar (npnBIP) transistor.

Here, letters S, G and D affixed to the nMOS or pMOS indicate the nodes of the source, gate and drain thereof, respectively, while letters C, E and B affixed

REPLACEMENT SHEET
28 FEB 1997

to the npnBIP transistor indicate the nodes of the collector, emitter and base thereof, respectively (in the following drawings, these node names shall be omitted). Besides, in the figure, diffusion layers have only the impurity types thereof written down for the sake of brevity. Accordingly as regards portions to which the same symbols are assigned, it is merely indicated that the conductivity types are the same, and the impurity materials and impurity concentration are selected at will properly according to the purposes of the portions. Unless particularly specified, these facts hold true also in the ensuing drawings. In such a structure, with the prior art, the isolation among a large number of devices within a chip is executed by applying the lowest potential in the circuitry to a p-type substrate (p-Sub) and the highest potential in the circuitry to the n-type isolation layer (nWELL) for forming the pMOS transistor, whereby the junctions of various parts are prevented from falling into the condition of forward bias. That is, with the prior art, in a case where the circuitry operates between a supply voltage (for example, 5 V) and the earth (0 V), the devices are isolated by applying 0 V to the substrate p-Sub and 5 V to the n-type isolation layer. Since, in such a system, the applied voltage to the substrate p-Sub or to the n-type isolation layer is selected at the lowest voltage required for the device isolation, reverse bias voltages to be applied to the p-n junctions can be rendered small, and therefore it is possible to cope with the problems of lowering in the breakdown voltages of devices, etc. attendant upon the future microminiaturization of the devices. On the other hand, however, a problem to be stated below arises.

Since the input or output terminal of the LSI is directly connected with an external circuit, noise above the supply voltage or below 0 V (in general, surge noise

REPLACEMENT SHEET
28 FEB 1997

such as overshoot or undershoot) might arrive. Since the input or output node is connected to the diffusion layer within the chip in any form, the corresponding junction will then be forward-biased in the prior art. By way of example, when the minus surge noise is applied to the n-type diffusion layer indicated at the source S or drain D of the nMOS transistor in Fig. 1, the junction between the n-type diffusion layer and the substrate p-Sub is forward-biased, and a forward current flows from the substrate p-Sub toward the n-type diffusion layer. As a result, minority carriers (electrons in a p-type substrate) are injected into the substrate p-Sub. Since the minority carriers have a mean free path which is usually as long as several hundred μm, they reach another circuit part and incur, for example, the problem that a stored signal in a memory cell is destroyed in an SRAM or DRAM. The phenomenon of the minority carrier injection might be caused, not only at the input or output node part, but also by a circuit operation inside the chip in such a manner that the potential of the diffusion layer or of the substrate p-Sub fluctuates locally due to capacitive coupling or due to saturated operation of the bipolar transistor. It is therefore impossible to realize high performance of the BiCMOS system.

Disclosure of the Invention:

An object of the present invention is to solve the problem described above, and to provide a semiconductor device which operates stably. Another object of the present invention is to solve the problem described above, and to provide a voltage application method by which a voltage to be applied to a substrate or an isolation region is freely set according to an intended use, as well as a device structure which makes the method possible.

Further objects of the present invention will become

REPLACEMENT SHEET
28 FEB 1997

apparent from the following description of embodiments and drawings.

In the present invention, a voltage which is still negative (in general, when a p-type silicon substrate is used) or positive (in general, when an n-type silicon substrate is used) with respect to the operating voltage of circuitry is applied to a portion liable to the injection of minority carriers, for example, a substrate.

Further, in the present invention, in order to solve problems ascribable to the method of applying the voltage as stated above, for example, the problem that voltages to be applied to individual devices increase to degrade the reliability of a device of low breakdown voltage such as a microminiature device, the isolation region of MOS transistors of identical conductivity type or bipolar transistors of identical conductivity type is divided into several isolated regions, to which suitable isolation voltages are applied according to the respective uses.

Brief Description of the Drawings:

Fig. 1 is a sectional view showing a prior art, Fig. 2 is a sectional view showing the first embodiment of the present invention, Fig. 3 is a sectional view showing the second embodiment of the present invention, Fig. 4 is a sectional view showing the third embodiment of the present invention, Fig. 5 is a sectional view showing an embodiment of a CMOS structure, Fig. 6 is a sectional view showing an embodiment of a bipolar structure, Fig. 7 is a sectional view showing an embodiment of a bipolar-CMOS complex structure, Fig. 8 is a sectional view showing an embodiment of an SOI structure, Fig. 9 is a sectional view showing an embodiment of an SOS structure, Fig. 10 is a block diagram of a memory, Fig. 11 is a diagram showing an embodiment for the application of a substrate isolation voltage to a memory, Figs. 12 - 16 are sectional views

REPLACEMENT SHEET
28 FEB 1997

each showing an embodiment of a MOS dynamic memory, Figs. 17 and 18 are sectional views each showing an embodiment of a bipolar-CMOS complex dynamic memory, Fig. 19 illustrates sectional views showing an embodiment of principal steps for realizing the structure in Fig. 18, Fig. 20 is a sectional view showing another embodiment of the bipolar-CMOS complex dynamic memory, Fig. 21 is a plan view with the embodiment of Fig. 20 seen from the front surface of a chip, and Fig. 22 illustrates sectional views showing an embodiment of principal steps for realizing the structure in Fig. 21.

Best Mode for Carrying Out the Invention:

Now, the details of the present invention will be described in conjunction with embodiments.

[Embodiment 1]

Fig. 2 shows one of the basic embodiments of the present invention, in which the BiCMOS system is applied to a dynamic RAM (DRAM) employing a 1-transistor type cell as a memory cell MC.

In the figure, the sectional structures of nMOS, pMOS and npnBIP transistors and the memory cell MC are illustrated. The information of the memory cell MC is read out to a data line DL or written therein from the data line in such a way that a storage capacitance is formed between n-type diffusion layers and a plate (PL) and between the n-type diffusion layers and a p-type diffusion layer, and that charges stored in the storage capacitance are controlled by a gate WL to which a word line signal is applied. Besides, in the memory cell MC shown in the figure, the p-type diffusion layer is disposed underneath the n-type diffusion layers for storing the charges. This p-type diffusion layer serves to increase the storage capacitance, and also to shield the capacitor portion from minority carriers attributed to radiant rays such as alpha particles entering a substrate (to function as a

REPLACEMENT SHEET
28 FEB 1997

barrier to the minority carriers), thereby to reduce a soft error rate ascribable to the entry of the radiant rays. Such a structure is detailed as the HiC type memory cell in "Technical Digest of International Electron Device Meeting," 1977, pp. 287 - 290, etc. Besides, the phenomenon of soft errors is detailed in "IEEE Transaction on Electron Device," Vol. ED-26, No. 1, Jan., 1979, pp. 2 - 9, etc.

As indicated in the figure, the silicon substrate used is a p-type substrate p-Sub. This is intended to employ an npn BIP transistors of high performance and to isolate them efficiently. The impurity concentration of the substrate is usually selected on the order of 10^{14} - 10^{16} (cm^{-3}) in consideration of the collector-substrate capacitance of the BIP transistor, etc. Symbols nBL and pBL denote buried layers of comparatively high concentrations, which reduce the collector resistance of the BIP transistor so as to realize high performance and simultaneously render the resistance values of well regions nWELL and pWELL smaller so as to prevent the occurrence of a latch-up phenomenon. The latch-up phenomenon is stated in "Technical Digest of International Electron Device Meeting," 1982, pp. 454 - 477, etc. The impurity concentrations of the buried layers nBL and pBL are respectively selected on the orders of 10^{18} - 10^{20} (cm^{-3}) and 10^{16} - 10^{18} (cm^{-3}). The buried layers can be realized by, for example, a method in which they are formed in the substrate p-Sub by diffusion beforehand, followed by the epitaxial growth of silicon and by the formation of the wells pWELL and nWELL, etc., or a method in which they are formed by the implantation of ions at comparatively high energy levels into the substrate p-Sub from the front surface thereof, and the details will be stated later. Either or both of these buried layers is/are omitted for some purposes. Symbol CN

REPLACEMENT SHEET
28 FEB 1997

denotes a heavily-doped layer for lowering the resistance between the collector node C or a node V_{BB2} and the buried layer nBL. Symbols nWELL and pWELL denote regions for forming the pMOS and nMOS transistors, respectively. For this example the collector layer of the BIP transistor is made of nWELL and nBL.

In the construction thus far described, according to the present invention, a voltage which is higher or lower than the operating voltage range of the circuitry is applied as at least one of voltages for isolating the individual devices, V_{BB1} (this voltage is generally called a "substrate voltage" as it is supplied to the substrate through the regions pWELL and pBL) and V_{BB2} (generally called a "well voltage"). Whether such a voltage or voltages is/are applied as either or both of the isolation voltages, may be selected according to purposes. By way of example, under the condition that the circuitry operates between 0 V and V_{CC} (for example, 5 V), a negative voltage below 0 V is applied as the substrate voltage V_{BB1} and the voltage V_{CC} is applied as the well voltage V_{BB2}. Thus, the value of the substrate voltage V_{BB1} is set so that the substrate and the n-type diffusion layer within the region pWELL, for example, may not be forward-biased even when a minus voltage is applied from inside or outside the semiconductor device to the n-type diffusion layer by any cause, thereby making it possible to perfectly solve the phenomenon in which the minority carriers are injected into the substrate and incur the malfunction of the circuitry as the problem of the prior art. This effect is especially remarkable in the DRAM of the type storing information in the form of charges as shown in Fig. 2, but it is a matter of course that marked effects are obtained also in other devices such as a logic LSI, SRAM and ROM. Although, in the above, the well voltage V_{BB2} has been set at the

REPLACEMENT SHEET
2 8 FEB 1997

supply voltage V_{CC}, a similar effect can be obtained even when a voltage higher than the supply voltage V_{CC} is applied as the well voltage V_{BB2} according to purposes. Moreover, according to the present invention, the well regions pWELL and nWELL and the diffusion layers lying in contact with them are not forward-biased, so that the occurrence of the latch-up phenomenon can be prevented. Furthermore, the reduction of junction capacitances becomes possible.

Although the example employing the p-type substrate has been taken in the present embodiment, an n-type substrate may well be employed in, e. g., a case of using a p-n-p BIP transistor. It is needless to say that, on that occasion, the signs of applied voltages ought to be made opposite. In addition, although the HiC type cell has been illustrated as the memory cell, the embodiment as left intact is also applicable to cases of employing various planar type or vertical type memory cells (such as CCC and STC cells) described in "IEE PROC.," Vol. 130, pt. I, No. 3, JUNE 1983, pp. 127 - 135; "1984, 1985 International Solid-State Circuit Conference," Digest of Technical Papers; etc. It is as stated before that the DRAM is not restrictive, but that the embodiment as left intact is also applicable to other general LSIs such as SRAMs, ROMs and logic LSIs. Besides, although the voltage higher or lower than the operating voltage range of the circuitry is required in the present invention, it can be generated within the semiconductor device by any of methods described in Japanese Utility Model Registration Application No. 54-82150; or 1976 ISSCC Digest of Technical Papers," pp. 138 - 139; etc., and hence, it can also be realized without externally feeding a dedicated voltage. The substrate voltage V_{BB1} may well be applied from the rear surface of the substrate.

The embodiment thus far described has referred to

REPLACEMENT SHEET
28 FEB 1997

the method in which the voltage is uniformly applied to the substrate p-Sub or the well region nWELL within the chip, thereby to solve the problem of the prior art. Next, there will be elucidated a case where unequal isolation voltages are applied in conformity with the purposes of circuit blocks within a chip. For example, an inout circuit block as to which the injection of minority carriers is problematic or a circuit block which needs to reduce its junction capacitance has the isolation voltage higher or lower than the operating voltage range of the circuitry applied thereto as explained in connection with Fig. 2. On the other hand, in the block of the memory cell in Fig. 2, it is desired that the concentration of the p-type impurity layer forming the storage capacitance be heightened to increase the storage capacitance and also to augment the shield effect against the minority carriers created by the entry of alpha particles. It is also desired that devices be microminiaturized to attain a higher density and a higher speed. In these blocks, the breakdown voltages of the devices become lower. Therefore, the highest or lowest voltage within the operating voltage range of circuitry is applied as the isolation voltage of such a block likewise to the prior art. There will be described embodiments on a method which applies any desired voltages according to purposes in this manner, and a semiconductor structure which makes the method possible.

The techniques to be discussed hereinafter can be applied without any change, not only to LSIs of the BiCMOS system, but also to those of the conventional pMOS, nMOS or CMOS system. Therefore, various examples of applications shall be explained without sticking to the BiCMOS system.

[Embodiment 2]

REPLACEMENT SHEET
28 FEB 1997

Fig. 3 illustrates the application of the above measure to an integrated circuit of nMOS transistors. A construction in the figure is such that a p-type substrate (p-Sub) is formed therein with an n-well layer NW, in which p-well layers PW_1 and PW_2 are further formed. The nMOS transistors formed in the two p-wells and the substrate p-Sub are respectively denoted by symbols nMOS1, nMOS2 and nMOS3. In this structure, voltages V_{BB1}, V_{BB2} and V_{BB3} independent of one another can be applied to the isolation layers of the three sorts of nMOS transistors, and they can be selected at suitable voltages according to circuit uses.

On the other hand, the supply voltage V_{CC} or a voltage which is at least higher than both the voltages V_{BB2} and V_{BB3} is applied as V_{BB4} to the n-well layer NW. Although the single nMOS transistor has been shown in Fig. 3, one well usually has a plurality of nMOS transistors in each of three isolation layers.

In addition, although the two p-wells and the single n-well have been shown in Fig. 3, this embodiment is also applicable to a combination wherein a plurality of n-wells are provided and wherein one or more p-wells are designed in each of the n-wells. It is also possible to construct all the nMOS transistors in a p-well. Further, the present invention can be readily applied to a pMOS integrated circuit merely by altering the conductivity types of the substrate, wells and MOS transistors and reversing all the potential relations. The voltage V_{BB1} may be applied to the substrate either from the front surface or from the rear surface thereof.

[Embodiment 3]

Fig. 4 shows an embodiment in which the present invention is applied to an nMOS integrated circuit employing an n-type substrate. Referring to the figure, two p-wells (PW_1, PW_2) are formed in the n-type substrate (n-Sub),

REPLACEMENT SHEET
28 FEB 1997

and nMOS transistors are formed in the respective p-wells. In the illustrated construction, voltages V_{BB2} and V_{BB3} unequal to each other are applied to the respective wells PW_1 and PW_2 by applying the present invention. As these voltages V_{BB2} and V_{BB3}, the optimum voltages can be applied depending upon the circuit portions. By way of example, the ground potential GND can be applied as the voltage V_{BB3}, and a still lower voltage of -3 V as the voltage V_{BB2}. A voltage V_{BB1} to be applied to the substrate n-Sub may be the supply voltage V_{CC}, or a voltage higher than both the voltage V_{BB2} and V_{BB3}.

Although only the two p-wells each including the single nMOS transistor therein have been shown in Fig. 4, the embodiment is readily applicable to the combination between any desired number of p-wells and any desired number of nMOS transistors. On this occasion, two or more voltage values as desired may be selected for the applied voltages of the plurality of p-wells in conformity with uses. Besides, a pMOS integrated circuit can be fabricated by inverting the conductivity types of the substrate, the wells, sources and drains. At this time, positive voltages unequal to each other are applied as the voltages V_{BB2} and V_{BB3}, and the voltage GND or a voltage lower than both the voltages V_{BB2} and V_{BB3} is applied as the voltage V_{BB1}.

[Embodiment 4]

Fig. 5 illustrates an embodiment in which the present invention is applied to a CMOS (complementary MOS) structure. Referring to the figure, three n-wells (NW_1, NW_2, NW_3) are formed in a p-type substrate, and p-wells (PW_1, PW_2) are further formed in the respective n-wells NW_1 and NW_2. Thereafter, nMOS transistors (nMOS1, nMOS2, nMOS3) are respectively formed in the p-wells (PW_1, PW_2) and the substrate p-Sub. Besides, pMOS transistors (pMOS1, pMOS2, pMOS3) are respectively formed in the n-wells

REPLACEMENT SHEET
20 FEB 1997

(NW_1, NW_2, NW_3). In this construction, voltages V_{BB2}, V_{BB4} and V_{BB1} are applied to the p-type isolation layers for the nMOS transistors. On the other hand, voltages V_{BB3}, V_{BB5} and V_{BB6} are applied to the n-type isolation layers for the pMOS transistors. As three voltages V_{BB2}, V_{BB4} and V_{BB1} or as three voltages V_{BB3}, V_{BB5} and V_{BB6}, voltages of at least two values unequal to each other are applied according to circuits used. By way of example, voltages of GND (0 V) and -3 V are applied as the voltages V_{BB2}, V_{BB4} and V_{BB1}, while voltages of V_{CC} (+5 V) and $V_{CC} + \alpha$ (+7 V) are applied as the voltages V_{BB3}, V_{BB5} and V_{BB6}. In this way, the voltages as desired can be applied to the individual isolation layers of the nMOS and pMOS transistors. Although, in Fig. 5, only one MOS transistor has been shown in each of the wells, a plurality of MOS transistors may well be provided as are necessary. In addition, although the numbers of the wells are 3 as the n-wells and 2 as the p-wells in Fig. 5, they may be increased or decreased as are necessary. Further, it is to be understood that the present invention is also applicable to a construction wherein the polarities of the substrate and the wells are inverted. That is to say, p-wells are first formed in an n-type substrate and wherein n-wells are subsequently formed.

While the embodiments described above concern the construction employing only the MOS transistors, there will now be described examples in each of which the present invention is applied to an integrated circuit employing bipolar transistors or an integrated circuit having both bipolar and MOS transistors.

[Embodiment 5]

Fig. 6 illustrates an embodiment in which the present invention is applied to an integrated circuit employing bipolar transistors. Referring to Fig. 6, three n-p-n bipolar transistors (npn1, npn2, npn3) are one p-n-p

REPLACEMENT SHEET
28 FEB 1997

bipolar transistor (pnp1) are formed. In a conventional bipolar integrated circuit, a plurality of n-p-n transistors are constructed in a p-type substrate p-Sub likewise to the transistor npn3 in this figure and are fed with a common substrate voltage as a voltage V_{BB1} from the front surface or rear surface of a chip. When the magnitude of the voltage V_{BB1} is set at the lowest potential GND (0 V) in circuitry or at a still lower potential, the plurality of bipolar transistors can be isolated from one another. In the present invention, p-type isolation layers separated from the substrate p-Sub are further provided as indicated by symbols PW_1 and PW_2, and the n-p-n transistors (npn1, npn2) are formed therein. The p-layers have voltages V_{BB2} and V_{BB3} applied thereto. The values of the voltages V_{BB2} and V_{BB3} can be set independently of the voltage V_{BB1}. A voltage V_{BB4} is applied to an n-type layer (nW) for isolating the substrate p-Sub and the p-layers. When a voltage V_{BB4} (for example, equal to the supply voltage V_{CC}) is higher than the three voltages V_{BB1}, V_{BB2} and V_{BB3}, the transistors npn1, npn2 and npn3 can be perfectly isolated from one another. The p-n-p transistor (pnp1) in the figure can be constructed by employing some of layers used for forming the transistors npn1 and npn2. When the conductivity types of all the layers including the substrate are reversed, unequal voltages can be applied to n-type isolation layers forming a plurality of p-n-p transistors.

[Embodiment 6]

Next, there will be elucidated an example in which the present invention is applied to the so-called BiCMOS structure having both CMOS and bipolar transistors in a chip. Fig. 7 illustrates the embodiment in which nMOS transistors (nMOS1, nMOS2, nMOS3) and pMOS transistors (pMOS1, pMOS2) are formed in a p-type substrate p-Sub

REPLACEMENT SHEET
28 FEB 1987

as in Fig. 5, and in which an n-p-n bipolar transistor (npnl) is further formed. As in the foregoing, voltages V_{BB1}, V_{BB2} and V_{BB3} can be independently set as the isolation voltages of the nMOS transistors. In addition, voltages V_{BB4} and V_{BB5} can be independently set as the isolation voltages of the pMOS transistors. The substrate voltage V_{BB1} of the transistor nMOS3 is applied to the isolation region of the bipolar transistor, but this voltage V_{BB1} can be set as an isolation voltage dedicated to the bipolar transistor in the absence of the transistor nMOS3. In addition, when a structure similar to that of the transistor npnl in Fig. 6 is incorporated in the construction of Fig. 7, isolation voltages unequal to each other can be fed to the bipolar transistors. Besides, a p-n-p transistor can be formed as in Fig. 6. Also, when the conductivity types of the substrate, the wells, the sources and drains of the MOS transistors, and the collector, emitter and base of the bipolar transistor are all inverted, a p-n-p transistor and a CMOS structure can be constructed, and the plurality of isolation voltages of the present invention can be applied to such a construction.

[Embodiment 7]

Fig. 8 shows an embodiment in which the present invention is applied to the nMOS portion of a stacked CMOS structure. The figure shows the example which is formed with nMOS transistors on the side of a substrate, and with pMOS transistors on the substrate by the so-called SOI structure wherein polycrystalline Si is grown on an insulator film. By combining such a configuration with a p-well (pW) and an n-well (nW), independent voltages V_{BB2} and V_{BB1} can be applied to the respective isolation portions of the transistor nMOS1 formed in the p-well and the transistor nMOS2 formed in the substrate p-Sub. In addition, when the conductivity types of the substrate

REPLACEMENT SHEET
28 FEB 1997

and the wells are rendered opposite, it is possible to form pMOS transistors on the substrate side and nMOS transistors on the polycrystalline Si side and to apply separate isolation voltages to the isolation portions of the pMOS transistors.

[Embodiment 8]

Fig. 9 illustrates an embodiment in which nMOS and pMOS transistors are constructed on an insulating substrate written as INSULATOR in the SOI (Silicon on Insulator) or SOS (Silicon on Sapphire) structure, and in which the present invention is applied to such a construction. On the insulating substrate, p-type Si (or n-type Si) is formed by crystal growth, whereupon an n-type (or p-type) impurity is introduced into the p-layer deeply enough to reach the substrate, thereby to isolate a plurality of p-type (or n-type) regions. The nMOS transistors are formed in the isolated p-type regions, and the pMOS transistor is formed in the n-type region. Voltages V_{BB1} and V_{BB3} are applied to the respective p-type regions in conformity with the uses of circuits, while a voltage V_{BB2} is applied to the n-type region. The numbers of the p-type and n-type isolation regions in Fig. 9 can be selected as desired, and it is also possible to employ only either pMOS transistors or nMOS transistors.

[Embodiment 9]

Thus far, the various structures for the substrate voltage isolation have been described with reference to Fig. 2 and Figs. 3 - 9. Now, there will be described embodiments in which these structures are applied to semiconductor memories.

Fig. 10 is a block diagram of any of general memories (including a dynamic RAM, a static RAM, a ROM, etc.). Symbol ADR denotes an address input, symbol CS a chip select input, symbol WE a write enable input, symbol DI a data

REPLACEMENT SHEET
28 FEB 1997

input, and symbol DO a data output. The designations of these signals are mere examples, and other designations are sometimes used.

A block I indicates an address buffer as well as a decoder and a driver. A block C indicates a control circuit and a write circuit. A block MC indicates a memory cell array. A block SO indicates a sense circuit and an output circuit. One embodiment of the present invention consists is applying the different voltage to the memory all array MC enclosed with a broken line from to the other portion.

Referring to Fig. 11, a chip which includes the two blocks isolated as in Fig. 10 has a built-in substrate bias voltage generator, and the two outputs V_{BBM1} and V_{BBM2} of the bias voltage generator are applied to the peripheral circuits other than the memory cell array, while a supply voltage V_{CC} and the ground potential GND are applied to the memory cell array as V_{BBM3} and V_{BBM4} respectively. The circuit arrangement of the substrate bias voltage generator has already been disclosed in "1976 ISSCC," pp. 138 - 139 or Japanese Patent Application Laid-open No. 51-117584. In this construction, by way of example, the isolation region (n-well) of the pMOS transistor of the peripheral circuit is fed with the voltage V_{BBM1} (+7 V) and the isolation region (p-well) of the nMOS transistor thereof with the voltage V_{BBM2} (-3 V), while the n-well of the pMOS transistor of the cell array is fed with the voltage V_{CC} and the p-well of the nMOS transistor thereof with 0 V. By supplying the voltage of large absolute values to the isolation regions of the input and output circuits in this manner, the memory becomes stable against the overshoots and undershoots of input and output signals, junction capacitances

REPLACEMENT SHEET
28 FEB 1997

(the capacitances between the sources or drains of MOS transistors and a substrate, and the capacitances between the collectors of bipolar transistors and the substrate) can be reduced, and an impurity concentration profile less prone to soft errors can be selected for the cell array. By the way, the designations of isolation voltages for use in the following embodiments shall correspond to the symbols V_{BBM1}, V_{BBM2}, V_{BBM3} and V_{BBM4} in Fig. 11 in accordance with the roles thereof.

Sectional views of embodiments of chips which are obtained for the embodiment of the chip setup in Figs. 10 and 11 will be elucidated below. Each of them illustrates the sectional structure of the portions of the input circuit and dynamic memory cell of a MOS dynamic RAM in correspondence with the prior-art example in Fig. 1. Although the memory cell is the dynamic cell here, the present invention is similarly applicable to a MOS static memory cell and a bipolar static memory cell.

[Embodiment A]

In an embodiment in Fig. 12, the nMOS transistors of an input protection circuit (an n-type diffused resistor and an nMOS diode) and an input circuit are formed in a p-well (pW), the pMOS transistor of the input circuit is formed in an n-well (nW), and a memory cell made of an nMOS transistor is formed in a p-type substrate p-Sub. In the present embodiment, the p-well of the input circuit and the substrate p-Sub are isolated. Therefore the values of the isolation voltages V_{BBM2} and V_{BBM4} of the respective regions can be independently set. Accordi by way of example, the voltage V_{BBM2} can be selected at -3 V in order to satisfy the specifications of the input circuit, and the voltage V_{BBM4} can be selected at 0 V from the viewpoint of the soft-error immunity of the memory cell. A broken line under the memory cell indicates a p-type high impurity concentration layer.

REPLACEMENT SHEET
23 FEB 1997

In this way, the disadvantage of the prior-art example elucidated in Fig. 1 can be prevented to provide a stable dynamic memory.

[Embodiment B]

In Fig. 13, only the n-type diffused resistor and nMOS diode of an input protection circuit are provided in a p-well, and the nMOS transistors of any other peripheral circuits are formed in a p-type substrate p-Sub likewise to a memory cell. Besides, a pMOS transistor can be formed in an n-well. A voltage V_{BBM2} (for example, -3 V) is applied to the p-well under the n-type diffused resistor and nMOS diode which are input protection devices, while a voltage V_{BBM4} (for example, 0 V) is applied to the substrate p-Sub of the nMOS transistors of the input circuit and the memory cell. A p-type high concentration layer is provided under the memory cell as in Fig. 12. A voltage V_{BBM1} is applied to the n-well. The present embodiment is advantageous over the embodiment of Fig. 12 in that, since only the input protection devices are provided in the well, the layout is simplified, and that, since the nMOS transistors other than the input protection diode are formed under the same concentration condition over the cell and the peripheral circuit, the control of threshold voltages V_{TH} is easy.

[Embodiment C]

Fig. 14 illustrates an embodiment in which a memory cell is formed in a p-well (pW), while the nMOS transistors of an input protection circuit and any other peripheral circuit are formed in a p-type substrate p-Sub. In the present embodiment, the p-well of comparatively high concentration is provided under the memory cell, and it acts as the substitute of the high concentration layer indicated by the broken line in Fig. 12 or 13.

[Embodiment D]

Fig. 15 illustrates an embodiment which employs

REPLACEMENT SHEET
28 FEB 1997

an n-type layer as a substrate and in which a peripheral circuit and a memory cell are formed in p-wells. Whereas the embodiments of Figs. 12 - 14 have the double well structure, a well configuration of single layer suffices in the present embodiment. A voltage V_{BBM2} (for example, −3 V) is applied to the p-well of the nMOS transistor of the peripheral circuit, while a voltage V_{BBM4} (for example, 0 V) is applied to the p-well of the nMOS transistor of the memory cell. In addition, a voltage V_{BBM1} (for example, a supply voltage V_{CC}) is applied to the substrate n-Sub. In the p-well to which the voltage V_{BBM2} is applied, only an input protection circuit may be formed, or peripheral circuits such as an address buffer may well be included.

[Embodiment E]

Fig. 16 illustrates an example in which a pMOS memory cell is formed on a p-type substrate p-Sub. A voltage V_{BBM2} (for example, −3 V) is fed to the substrate of the nMOS transistor of a peripheral circuit, and a voltage V_{BBM1} (for example, +7 V) is applied to the n-well of the pMOS transistor of another peripheral circuit, thereby to reduce the source and drain junction capacitances of the pMOS transistor. A voltage V_{BBM3} (for example, a supply voltage V_{CC}) is applied to the n-well of the memory cell. Thus, it is possible to construct a memory in which the input circuit is immune against undershoots and can attain a high speed, while the memory cell is less prone to soft errors.

[Embodiment 10]

In the above, Embodiments A - E applied to the MOS memories (SRAM, DRAM) have been described as the practicable configurations of Embodiment 9 with reference to Figs. 12 - 16. Next, embodiments in each of which the present invention is applied to a memory by the use of the BiCMOS construction of Fig. 7 having both bipolar

REPLACEMENT SHEET
28 FEB 1997

and MOS devices will be described with reference to Figs. 17 - 21. Among the embodiments, those of Figs. 17 - 19 employ epitaxial layers, and those of Figs. 20 - 22 don't employ epitaxial layers.

[Embodiment F]

Fig. 17 shows the nMOS, pMOS and n-p-n bipolar transistors of peripheral circuits, and a dynamic type nMOS memory cell as viewed from the left.

Under the nMOS memory cell, a p-type buried layer (pBL) of high impurity concentration is put to intensify the soft-error immunity. This layer pBL is also used for the isolation of an n-type buried layer.

Although the nMOS transistor of the peripheral circuit is formed in a p-well, this p-well can be omitted when a p-type epitaxial layer is employed. An n-type buried layer nBL of high concentration is provided under this p-well layer, and an n-layer (CN) of high concentration is added for feeding a voltage to the layer nBL. Besides, the p-well has its side surrounded with an n-well thereby to be isolated from a p-type substrate p-Sub. A voltage V_{BBM2} (for example, −3 V) is applied to the nMOS transistor of the peripheral circuit, and the voltage V_{BBM1} (for example, a supply voltage V_{CC}) to the n-well of the pMOS transistor. A common voltage V_{BBM4} is applied to the isolation layer of the n-p-n bipolar transistor and that of the nMOS transistor of the memory cell. Buried layers nBL and pBL provided under a well serve to reduce the collector resistance of the bipolar transistor, and are also effective to prevent latch-up through the decrease of a substrate resistance.

[Embodiment G]

Fig. 18 illustrates an embodiment in which a memory cell is formed in a p-type substrate p-Sub, and the difference of which from the embodiment of Fig. 17 consists only in a construction under the memory cell. With

REPLACEMENT SHEET
28 FEB 1997

the construction in Fig. 17, the buried layer pBL of high concentration might rise and cause the threshold voltage V_{TH} of the nMOS transistor to fluctuate. In contrast, according to the construction in Fig. 18, a p-type high concentration layer indicated by a broken line is provided only under a storage capacitor so as to prevent the buried layer from rising to the channel part of the nMOS transistor of the memory cell.

Next, principal steps for realizing the sectional structure of Fig. 18 are illustrated in Fig. 19. At (a) in Fig. 19, n-type buried layers nBL are formed in the front surface of a p-type substrate, and at (b), a p-type buried layer pBL is further formed. Thereafter, a layer Epi is formed by epitaxial growth at (c), and n-wells (nWELL) and p-wells (pWELL) are formed in the layer Epi by steps (d) and (e). At (f), layers CN heavily doped with an n-type impurity are formed so as to connect with the underlying layers nBL. Though not shown in the drawing, the plate of a memory cell, the gates of MOS transistors, the source and drain layers of the MOS transistors, and if necessary, the emitter layer of a bipolar transistor are thereafter formed. Further, steps such as the formation of contact holes and metalizati are thereafter required. In the illustration of Figs. 17 and 18, the layers CN and nBL reduce the collector resistan of the bipolar transistor. On the other hand, the contact interfaces between the sources and drains and the wells of the MOS transistors and between the base and the collector of the bipolar transistor do not establish the contacts between layers of very high concentrations, and they can have their breakdown voltages held at degrees necessary for circuit operations.

[Embodiment H]

The above has been the example of the process employin the epitaxial layer, and embodiments which do not employ

REPLACEMENT SHEET
28 FEB 1997

the epitaxial layer will now be described with reference to Figs. 20 - 22. These embodiments form a high concentration layer in the place of a p-type substrate at a fixed depth by the use of implantation. For this reason, they can curtail the cost of manufacture as compared with the case of employing the epitaxial layer.

Fig. 20 is a sectional view, and the corresponding conceptual diagram seen from the front surface of a chip is shown in Fig. 21. An nMOS transistor nMOS1 has its p-type isolation layer (pWELL) enclosed with an n-layer (CN or n-well), thereby to be isolated from a p-type substrate p-Sub.

The principal steps of a process for realizing the structure of Figs. 20 and 21 are shown in Fig. 22. At (a), an n-layer of high concentration is provided in a substrate p-Sub at a fixed depth from the front surface thereof by ion implantation. Thereafter, an n-well and a p-well are formed at (b) and (c). The p-well can be omitted in the case of the p-type substrate p-Sub. At (d), n-layers (CN) of high concentration are formed so as to reach the n-type buried layer nBL. Steps after (d), for forming MOS and bipolar devices and metalization are similar to conventional steps.

As described above in conjunction with many embodiments, according to the present invention, independent voltages as desired can be applied to the substrate and isolation layer of a MOS device and the isolation layer of a bipolar device, and the optimum voltages conforming to the purposes of the circuits of the devices can be selected. Thus, the setting of concentration profiles, the setting of isolation voltages, etc. can be freely done in order to cope with the problems of the undershoots of inputs and outputs, junction capacitances, and soft errors.

Industrial Applicability:

Heretofore, the injection of minority carriers

REPLACEMENT SHEET
28 FEB 1997

ascribable to surge noise etc. has arisen at a p-n junction constituting a MOS transistor or a BiP transistor formed in a silicon substrate, and it has formed the cause of such a problem as the destruction of a stored signal in an SRAM or a DRAM.

Such a phenomenon degrades the reliability of the semiconductor device and is unfavorable.

The present invention can prevent the phenomenon, is applicable to various products including MOS, BiP, CMOS, Bi-MOS and Bi-CMOS devices and is capable of enhancement in the reliability etc., so that it can be effectively utilized.

* C L M S *

REPLACEMENT SHEET
28 FEB 1997

WHAT IS CLAIMED IS:

1. In a semiconductor device which has sources and drains of insulated-gate field effect transistors or collectors, bases and emitters of bipolar transistors within a substrate and a plurality of isolation layers isolated in the substrate; a semiconductor device characterize in that a voltage outside a varying range of applied voltages to respective electrodes of said source and drain or said collector, base and emitter is applied to at least one of said substrate and said plurality of isolation layers.

2. In a semiconductor device which has sources and drains of insulated-gate field effect transistors or collectors, bases and emitters of bipolar transistors within a substrate and a plurality of isolation layers isolated in the substrate; a semiconductor device characterize in that at least two unequal isolation voltages are applied to said substrate and the isolation layers which have conductivity types identical to each other, or to the plurality of isolation layers which have conductivity types identical to each other.

3. A semiconductor device having a semiconductor body, a semiconductor element includign at least one p-n junction provided in the body, power source means for the semiconductor element, and power source means for the body; characterized in that said power source means for said body supplies a voltage so as to prevent said p-n junction from being forward-biased even when an input voltage opposite in polarity to an input voltage which is originally expected as an input to said semiconductor element has arrived.

4. A semiconductor device as defined in Claim 3, characterized in that said semiconductor body is made up of a semiconductor substrate, and an epitaxial grown layer formed on said substrate.

This Sheet Has Been Replaced
THIS SHEET HAS BEEN REPLACED

* C L M S *

REPLACEMENT SHEET
2 8 FEB 1997

5. A semiconductor device as defined in Claim 3, characterized in that said semiconductor body is a semiconduct layer provided on an insulating substrate.

6. A semiconductor device as defined in Claim 4, characterized in that said semiconductor element includes at least a MOS transistor.

7. A semiconductor device as defined in Claim 4, characterized in that said semiconductor element includes at least a bipolar transistor.

8. A semiconductor device as defined in Claim 4, characterized in that said semiconductor element includes at least a MOS transistor and a bipolar transistor.

9. A semiconductor device as defined in Claim 3, characterized in that said semiconductor element is a semiconductor element to which an external input is applied.

10. A semiconductor device as defined in Claim 3, characterized in that said semiconductor element forms a semiconductor memory, and that said semiconductor element having said p-n junction not forward-biased is a semiconductor element to which an external input is applied.

This Sheet Has Been Replaced



THIS SHEET HAS BEEN REPLACED

REPLACEMENT SHEET
28 FEB 1997

SEMICONDUCTOR DEVICE

ABSTRACT:

The injection of minority carriers into a substrate caused by potential fluctuations ascribable to noise etc. is prevented.

In a semiconductor device which has sources and drains of insulated-gate field effect transistors or collectors, bases and emitters of bipolar transistors within a substrate and/or a plurality of isolation layers isolated in the substrate, voltages having values outside a varying range of applied voltages to respective electrodes of the source and drain or to the collector, base and emitter are applied to the substrate and the isolation layers.

FIGURE 2

This Sheet Has Been Replaced

THIS SHEET HAS BEEN REPLACED

REPLACEMENT SHEET
28 FEB 1997

FIG. 1

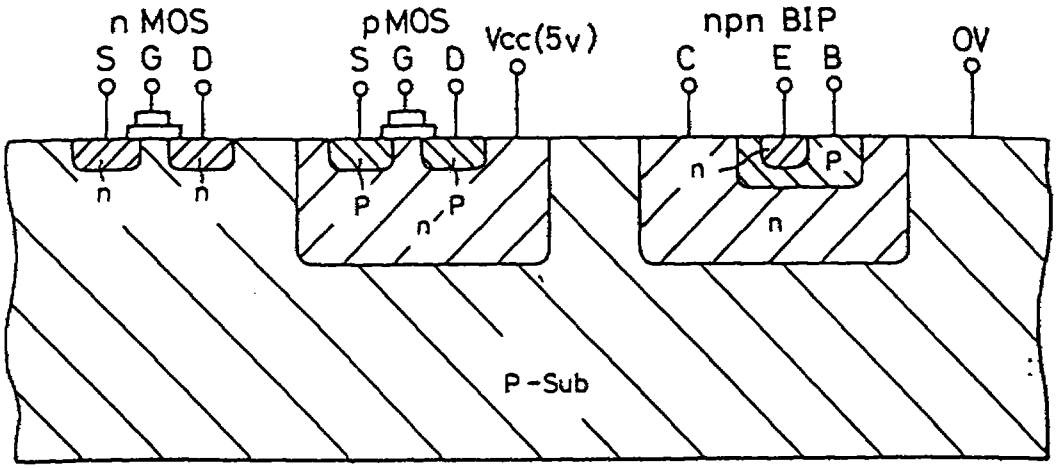
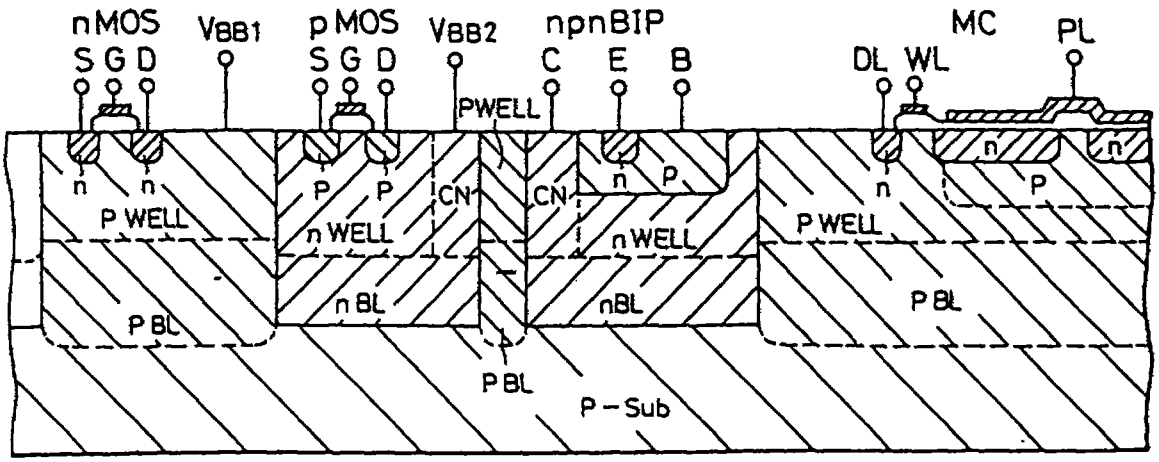


FIG. 2



REPLACEMENT SHEET
28 FEB 1997

FIG. 3

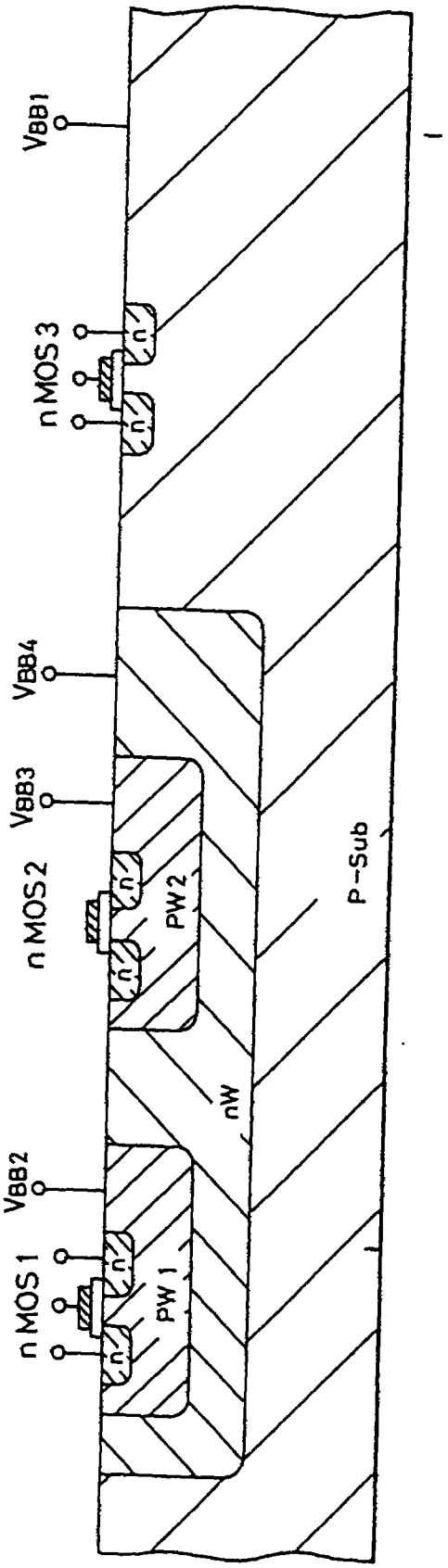
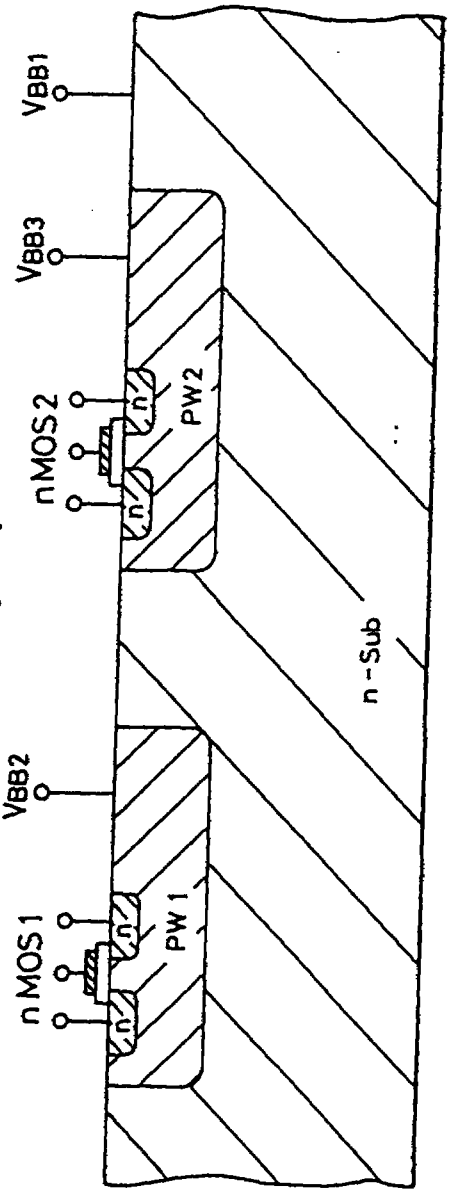
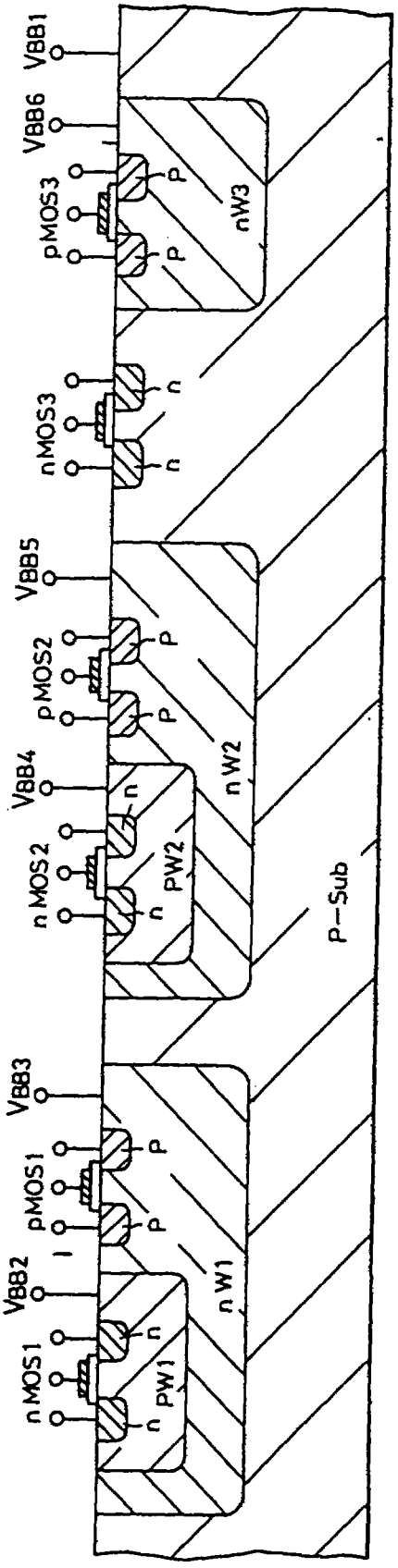


FIG. 4



REPLACEMENT SHEET
28 FEB 1997

FIG. 5



REPLACEMENT SHEET
28 FEB 1997

FIG. 6

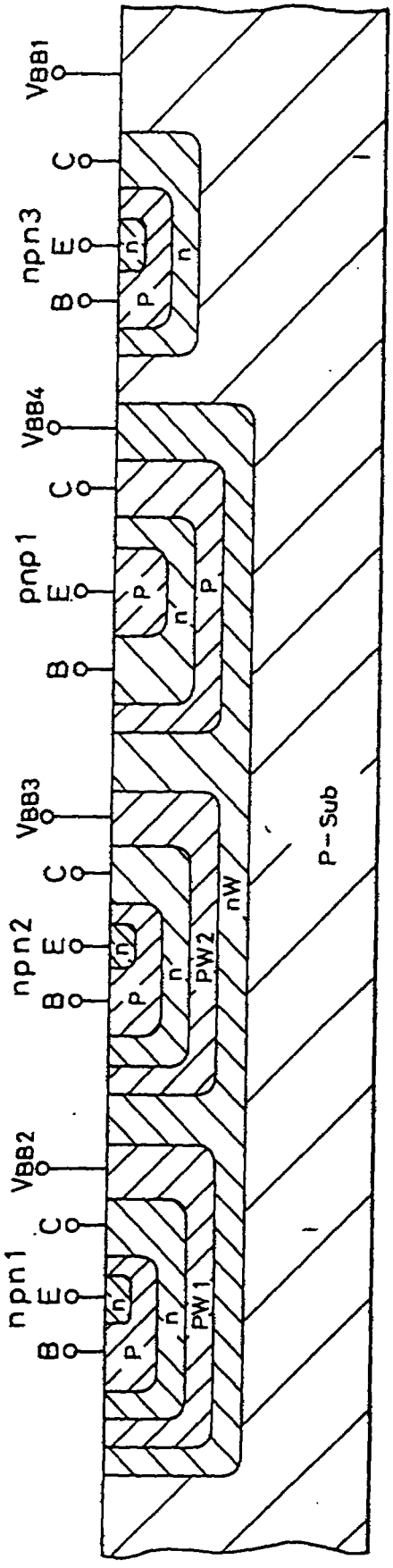
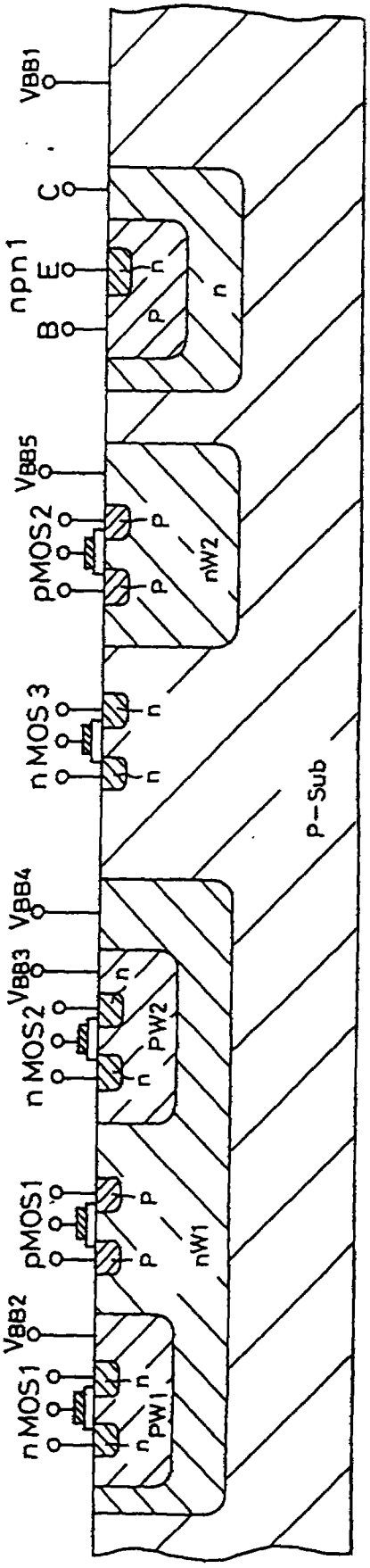


FIG. 7



REPLACEMENT SHEET
28 FEB 1997

FIG. 8

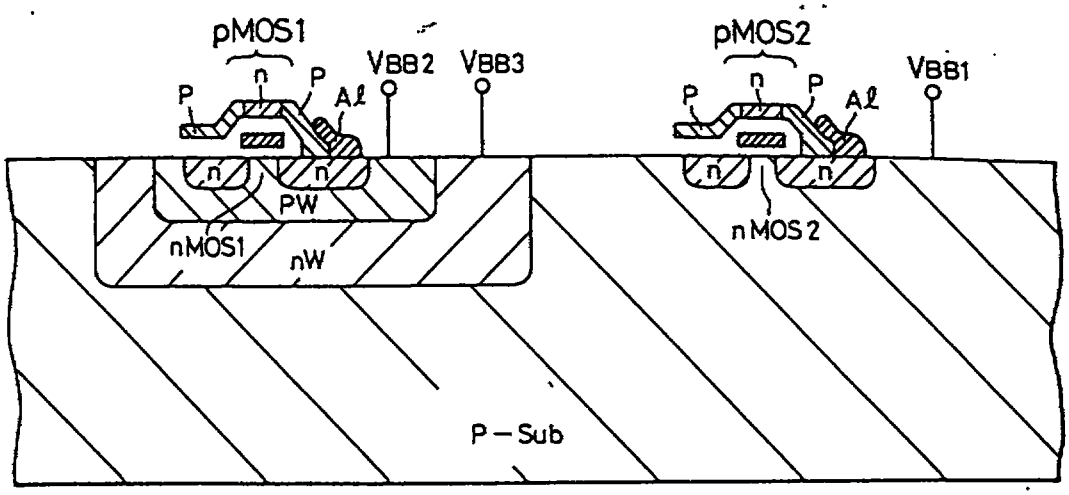
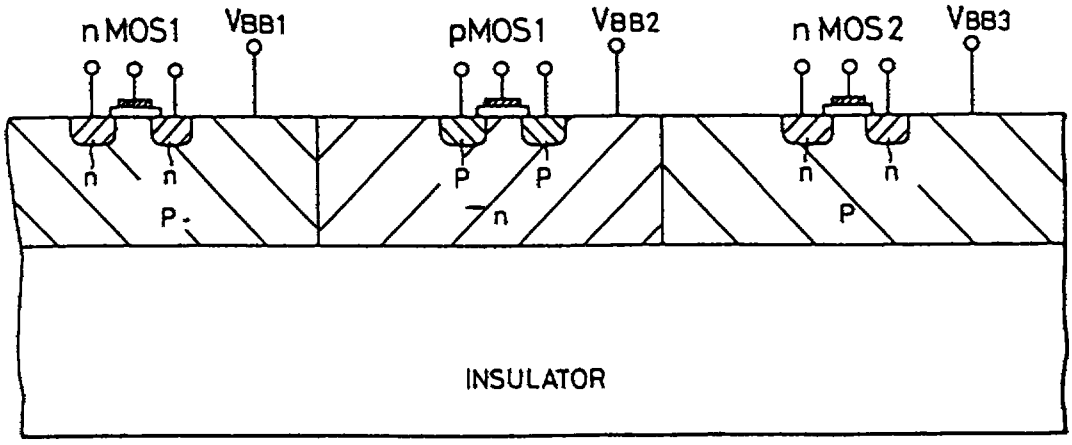


FIG. 9



REPLACEMENT SHEET
28 FEB 1997

FIG. 10

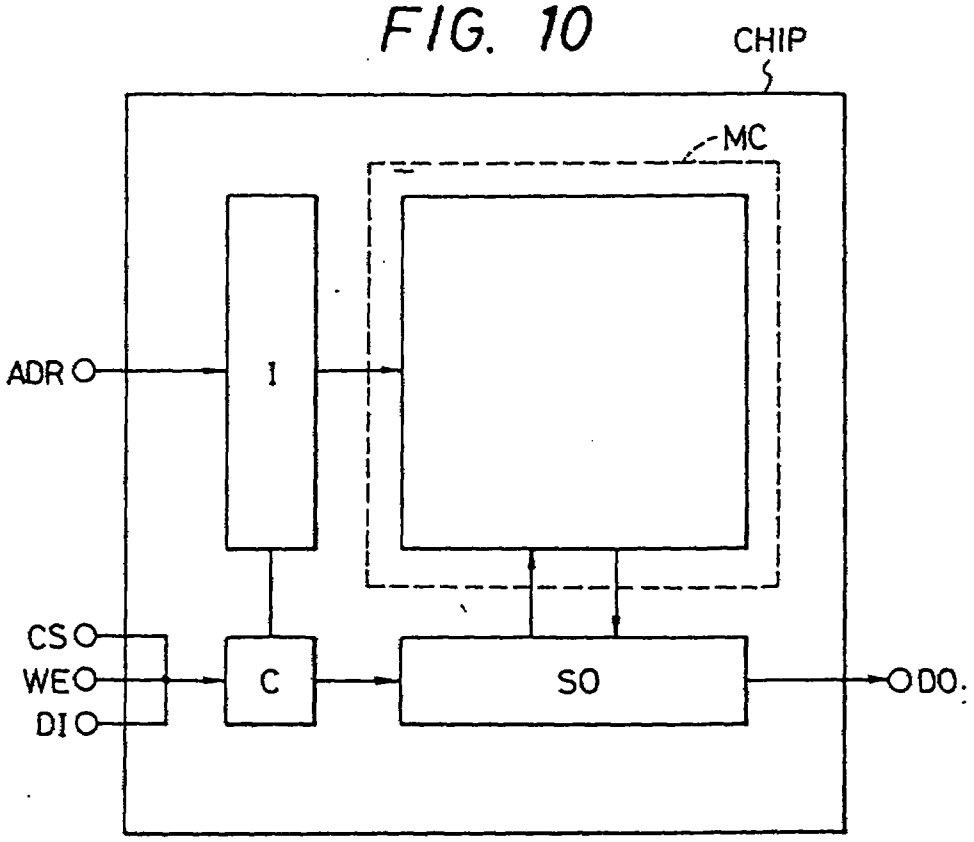
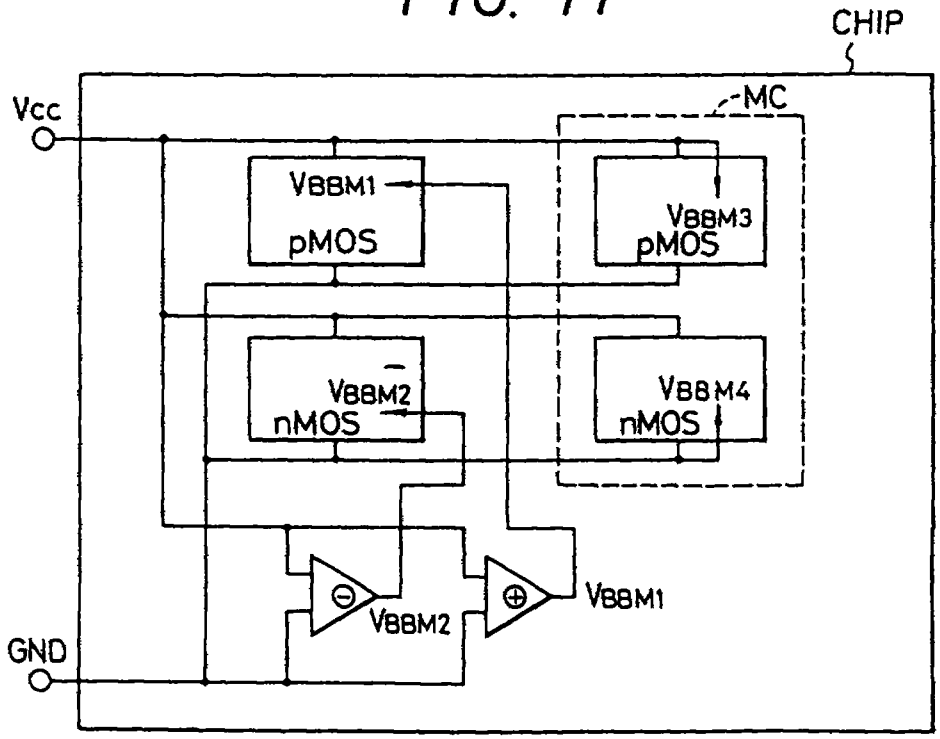


FIG. 11



REPLACEMENT SHEET
28 FEB 1997

FIG. 12

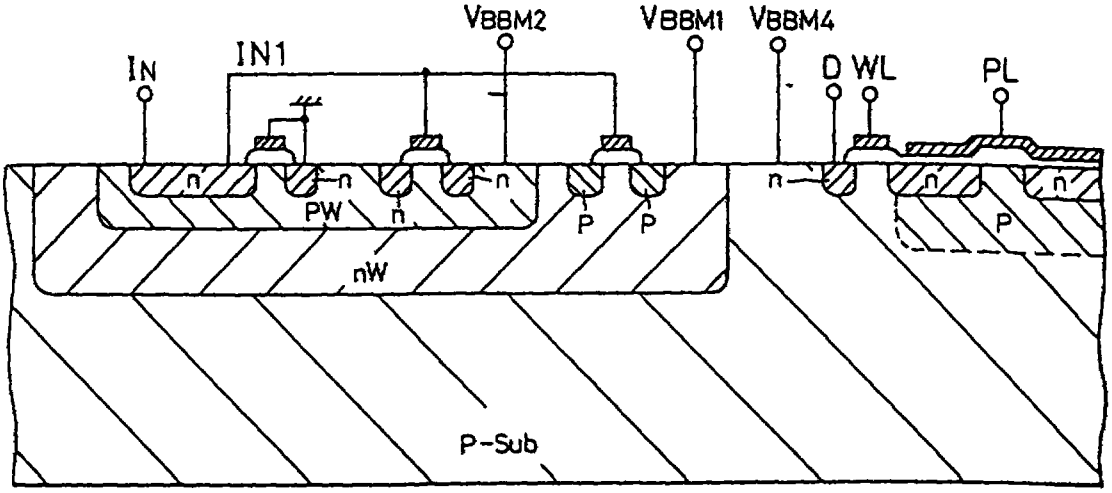


FIG. 13

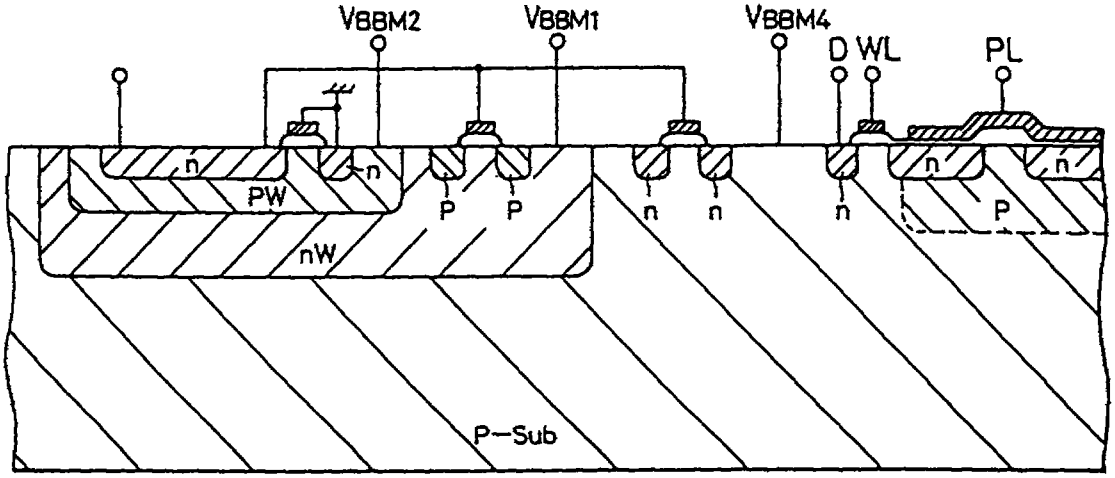
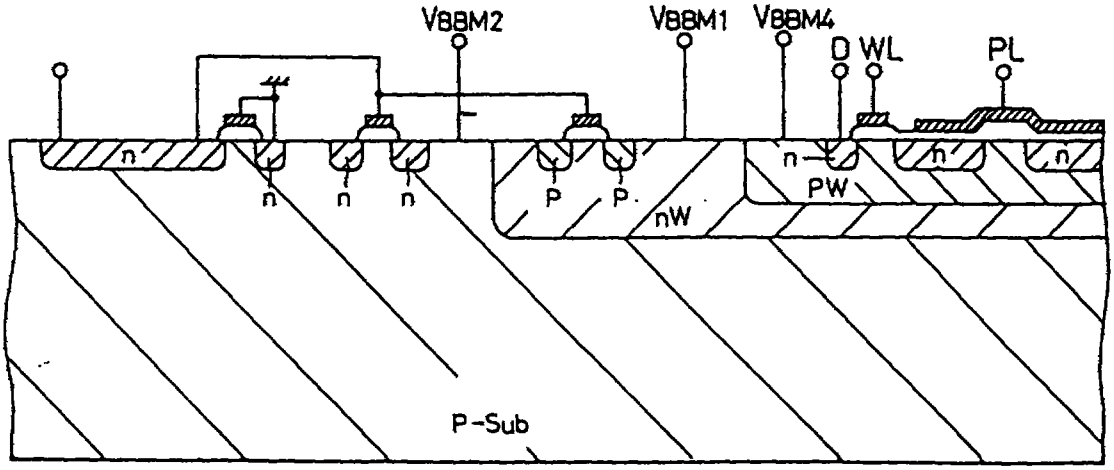


FIG. 14



REPLACEMENT SHEET
28 FEB 1997

FIG. 15

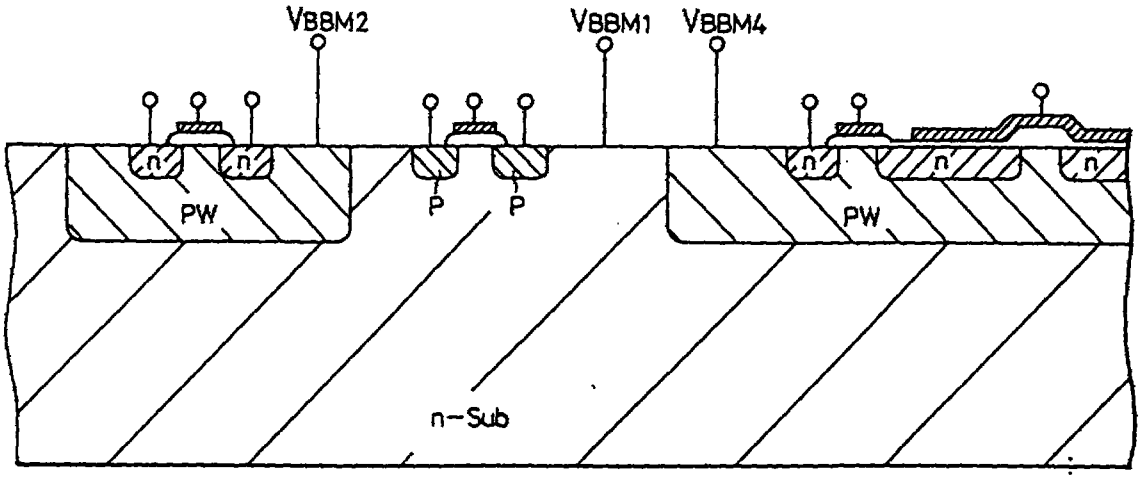
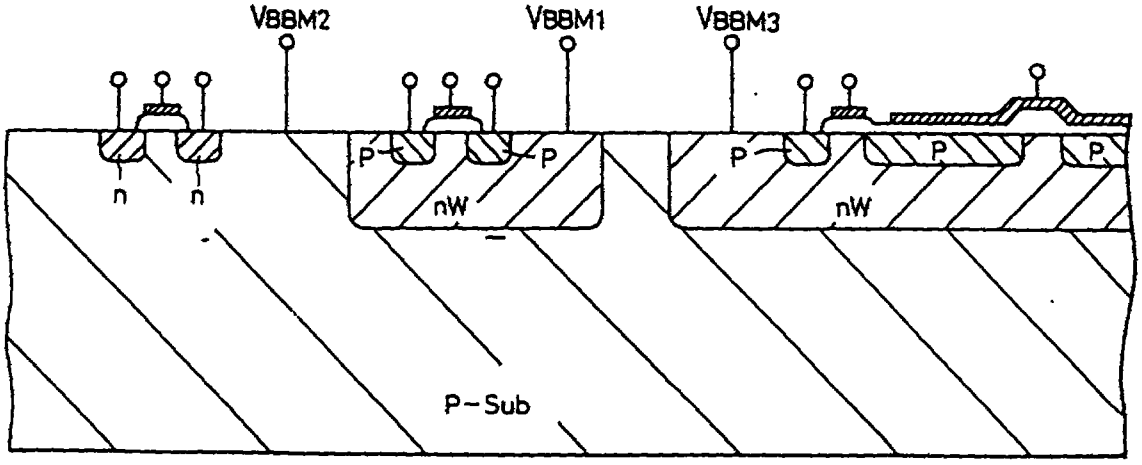


FIG. 16



REPLACEMENT SHEET
2 8 FEB 1997

FIG. 17

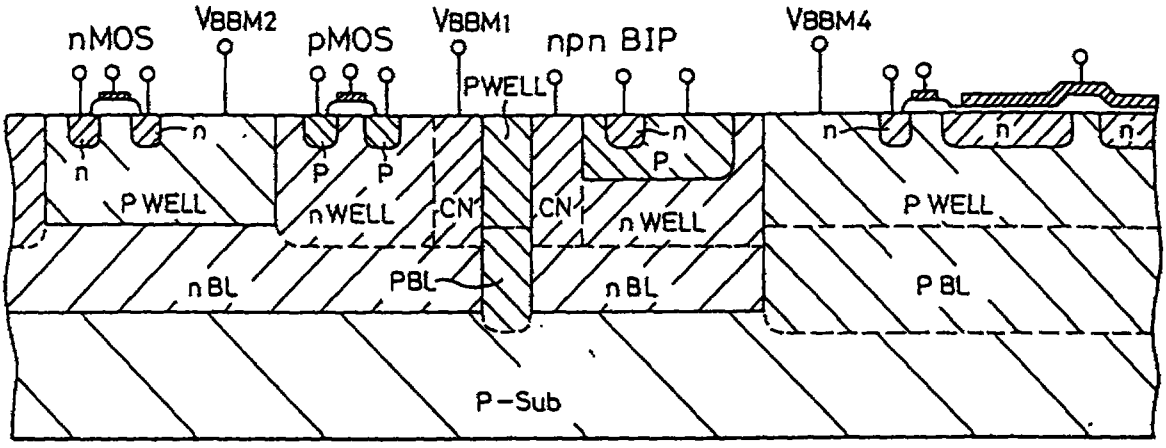
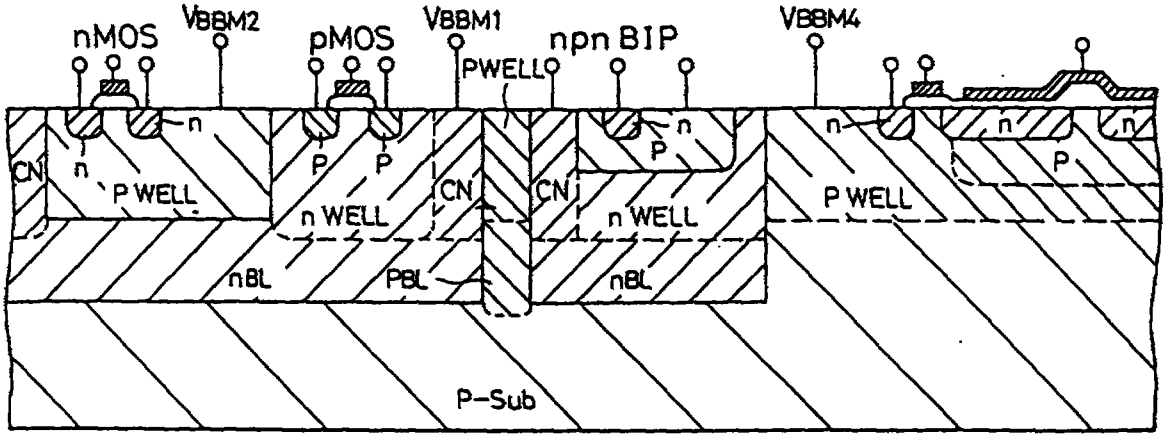
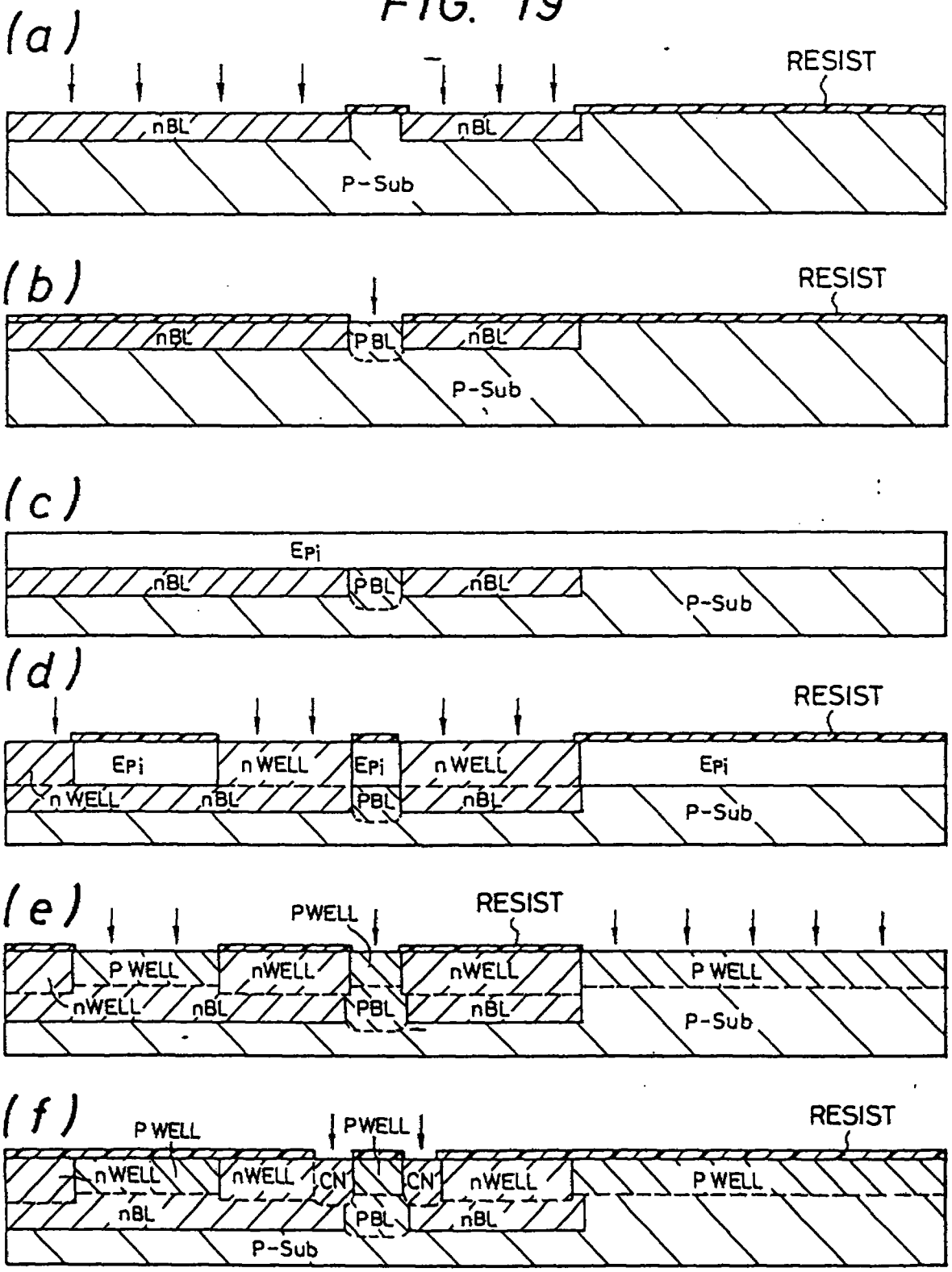


FIG. 18



REPLACEMENT SHEET
28 FEB 1997

FIG. 19



REPLACEMENT SHEET
28 FEB 1997

FIG. 20

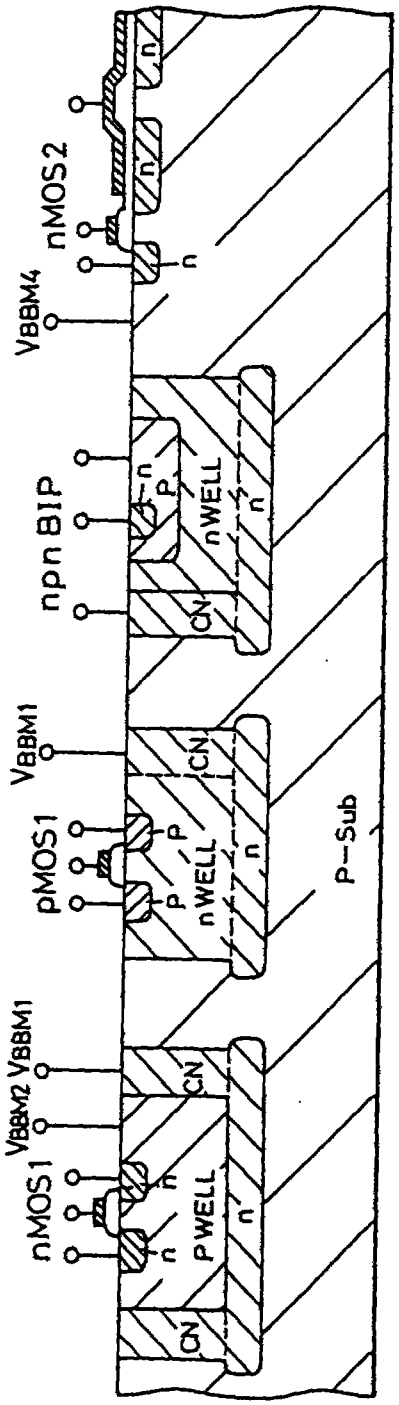
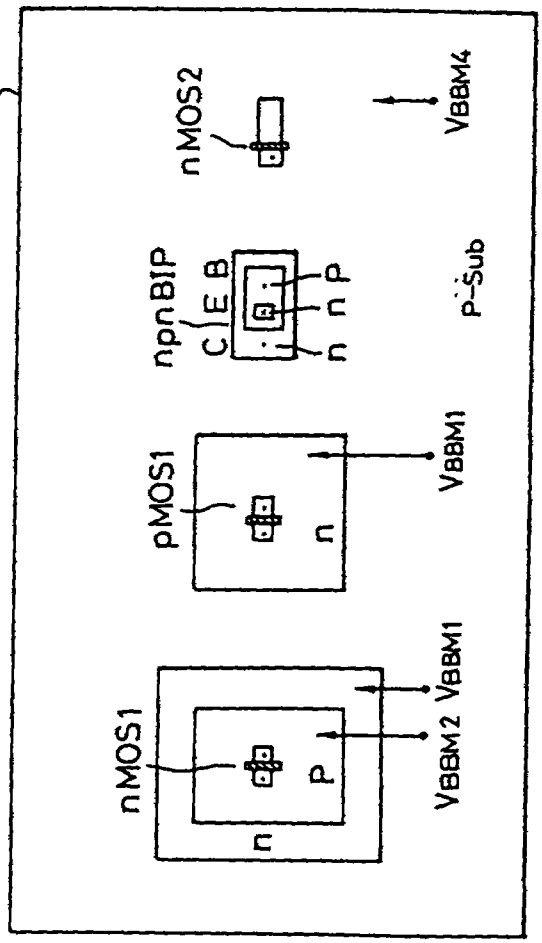
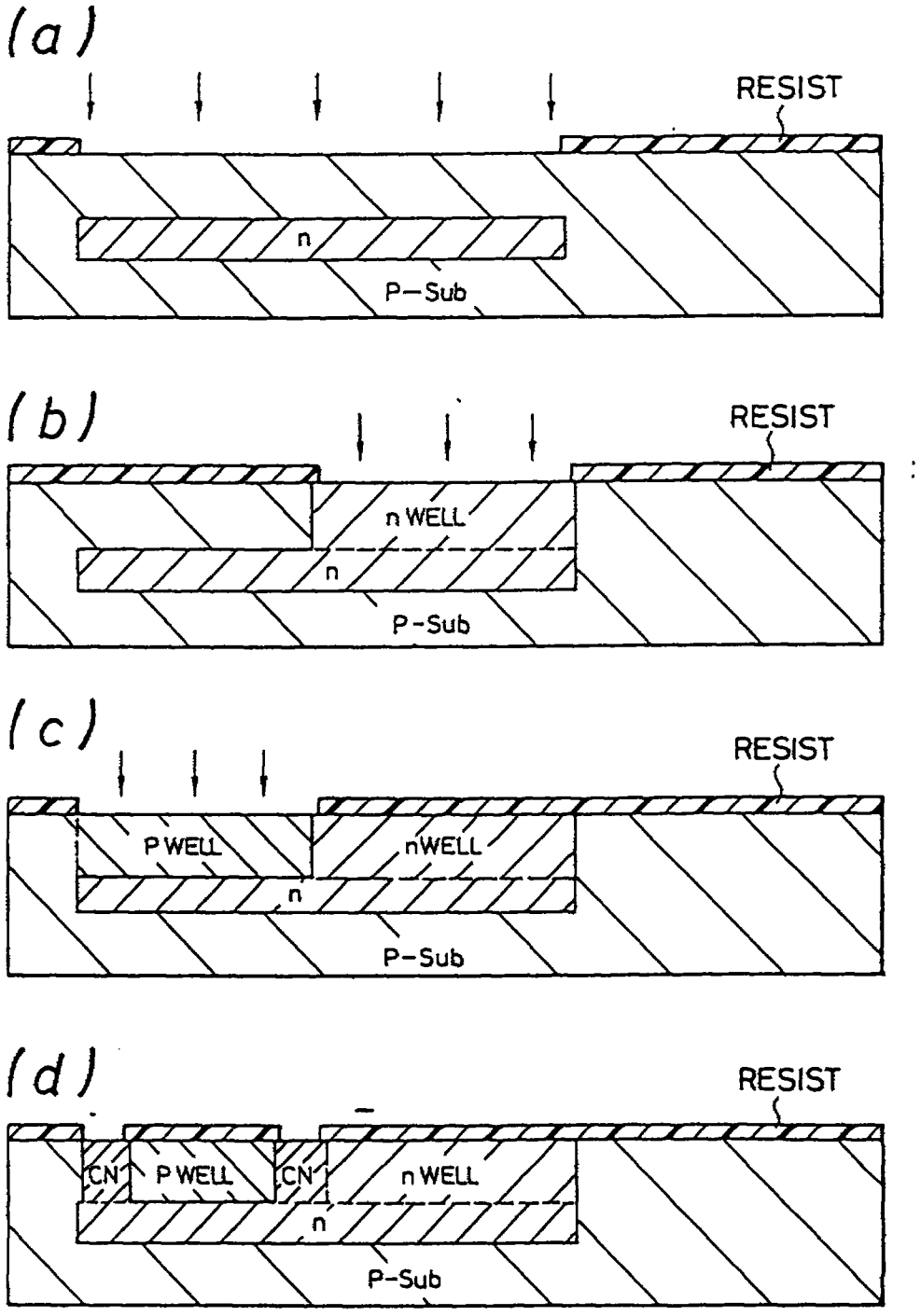


FIG. 21



REPLACEMENT SHEET
28 FEB 1997

FIG. 22



REPLACEMENT SHEET
06 MAR 1999

11. A semiconductor integrated circuit device comprising:

a semiconductor substrate having a main surface of a first conductivity type;

a first semiconductor region of a second conductivity type, opposite to said first conductivity type, extending to a first area of said main surface of said semiconductor substrate so as to form a first PN junction with said main surface of said semiconductor substrate;

a second semiconductor region of said first conductivity type in said first semiconductor region so as to form a second PN junction with said first semiconductor region, said second PN junction being surrounded by said first PN junction and being inside said
second first PN junction;

a third semiconductor region of said second conductivity type extending to a second area of said main surface of said semiconductor substrate so as to form a third PN junction with said main surface of said semiconductor substrate, said second area being a different area from said first area;

a fourth semiconductor region of said second conductivity type extending to a third area of said main surface of said semiconductor substrate so as to form a fourth PN junction with said main surface of said semiconductor substrate, said third area being a different area from said first area and said second area;

a first MISFET, having source and drain regions of said second conductivity type in a fourth area of said main surface of said semiconductor substrate, said fourth area being a different area from said first area , said second area and third area;

a memory cell, including a second MISFET having source and drain regions of said second conductivity type, said second MISFET being in said second semiconductor region;

a third MISFET, having source and drain regions of said first conductivity type in said third semiconductor region; and

a fourth MISFET, having source and drain regions of said first conductivity type in said fourth semiconductor region;

THIS SHEET HAS BEEN REPLACED

REPLACEMENT SHEET
06 MAR 1998

a bias voltage generator in said main surface of said semiconductor substrate,

wherein a first voltage is applied to said first semiconductor region, a second voltage is applied to said second semiconductor region, a third voltage is applied to said third semiconductor region, a fourth voltage is applied to said fourth semiconductor region and a fifth voltage is applied to said main surface of said semiconductor substrate, so that said first PN junction is reverse biased by said first and fifth voltages, said second PN junction is reverse biased by said first and second voltages, said third PN junction is reverse biased by said third and fifth voltages and said fourth PN junction is reverse biased by said fourth and fifth voltages,

wherein said second and fourth voltages are provided by said bias voltage generator, and

wherein a value of said second voltage is different from that of said fifth voltage, and a value of said third voltage is different from that of said fourth voltage.

12. A semiconductor integrated circuit device according to claim 11, further comprising a peripheral circuit in said main surface of said semiconductor substrate, wherein said peripheral circuit includes said first MISFET.

13. A semiconductor integrated circuit device according to claim 11, wherein said first conductivity type is p-type and said second conductivity type is n-type.

14. A semiconductor integrated circuit device according to claim 11, further comprising a capacitor element in said main surface of said semiconductor substrate, wherein said capacitor element is coupled to one of said source and drain regions of said second MISFET.

15. A semiconductor integrated circuit device comprising:

a semiconductor substrate having a main surface of a first

THIS SHEET HAS BEEN REPLACED

REPLACEMENT SHEET
06 MAR 1999

conductivity type;

a first semiconductor region of a second conductivity type, opposite to said first conductivity type, extending to a first area of said main surface of said semiconductor substrate so as to form a first PN junction with said main surface of said semiconductor substrate;

a second semiconductor region of said first conductivity type in said first semiconductor region so as to form a second PN junction with said first semiconductor region, said second PN junction being surrounded by said first PN junction and being inside said
second first PN junction;

a third semiconductor region of said second conductivity type extending to a second area of said main surface of said semiconductor substrate so as to form a third PN junction with said main surface of said semiconductor substrate, said second area being a different area from said first area;

a fourth semiconductor region of said second conductivity type extending to a third area of said main surface of said semiconductor substrate so as to form a fourth PN junction with said main surface of said semiconductor substrate, said third area being a different area from said first area and said second area;

a first MISFET, having source and drain regions of said second conductivity type in a fourth area of said main surface of said semiconductor substrate, said fourth area being a different area from said first area , said second area and third area;

a second MISFET having source and drain regions of said second conductivity type, said second MISFET being in said second semiconductor region;

a third MISFET, having source and drain regions of said first conductivity type in said third semiconductor region; and

a fourth MISFET, having source and drain regions of said first conductivity type in said fourth semiconductor region;

wherein a first voltage is applied to said first semiconductor region, a second voltage is applied to said second semiconductor region, a third voltage is applied to said third semiconductor region, a fourth voltage is applied to said fourth

THIS SHEET HAS BEEN REPLACED

REPLA... SHEET
0 6 MAR 1999

semiconductor region and a fifth voltage is applied to said main surface of said semiconductor substrate, so that said first PN junction is reverse biased by said first and fifth voltages, said second PN junction is reverse biased by said first and second voltages, said third PN junction is reverse biased by said third and fifth voltages and said fourth PN junction is reverse biased by said fourth and fifth voltages,

wherein a value of said second voltage is set so that said source and drain regions of said second MISFET and said second semiconductor region may not be forward biased and a value of said second voltage is set so that said source and drain regions of said fourth MISFET and said fourth semiconductor region may not be forward biased,

wherein a value of said second voltage is lower than that of said fifth voltage.

16 . A semiconductor integrated circuit device according to claim 15, wherein said first conductivity type is p-type and said second conductivity type is n-type.

17 . A semiconductor integrated circuit device according to claim 15, wherein a value of said third voltage is different from that of said fourth voltage.

THIS SHEET HAS BE... REPLACED

9609506-2

REPLACEMENT SHEET
25 SEP 1999

30

SEMICONDUCTOR DEVICE

ABSTRACT:

The injection of minority carriers into a substrate caused by potential fluctuations ascribable to noise etc. is prevented.

In a semiconductor device which has sources and drains of insulated-gate field effect transistors or collectors, bases and emitters of bipolar transistors within a substrate and/or a plurality of isolation layers isolated in the substrate, voltages having values outside a varying range of applied voltages to respective electrodes of the source and drain or to the collector, base and emitter are applied to the substrate and the isolation layers.

FIGURE 2

THIS SHEET HAS BEEN REPLACED

This Sheet Has Been Replaced

REPLACEMENT SHEET
14 OCT 1999

WHAT IS CLAIMED IS:

1. In a semiconductor device which has sources and drains of insulated-gate field effect transistors or collectors, bases and emitters of bipolar transistors within a substrate and a plurality of isolation layers isolated in the substrate; a semiconductor device characterized in that a voltage outside a varying range of applied voltages to respective electrodes of said source and drain or said collector, base and emitter is applied to at least one of said substrate and said plurality of isolation layers.

2. In a semiconductor device which has sources and drains of insulated-gate field effect transistors or collectors, bases and emitters of bipolar transistors within a substrate and a plurality of isolation layers isolated in the substrate; a semiconductor device characterized in that at least two unequal isolation voltages are applied to said substrate and the isolation layers which have conductivity types identical to each other, or to the plurality of isolation layers which have conductivity types identical to each other.

3. A semiconductor device having a semiconductor body, a semiconductor element includign at least one p-n junction provided in the body, power source means for the semiconductor element, and power source means for the body; characterized in that said power source means for said body supplies a voltage so as to prevent said p-n junction from being forward-biased even when an input voltage opposite in polarity to an input voltage which is originally expected as an input to said semiconductor element has arrived.

4. A semiconductor device as defined in Claim 3, characterized in that said semiconductor body is made up of a semiconductor substrate, and an epitaxial grown layer formed on said substrate.

REPLACEMENT SHEET
14 OCT 1999

* C L M S *

5. A semiconductor device as defined in Claim 3, characterized in that said semiconductor body is a semiconduct layer provided on an insulating substrate.

6. A semiconductor device as defined in Claim 4, characterized in that said semiconductor element includes at least a MOS transistor.

7. A semiconductor device as defined in Claim 4, characterized in that said semiconductor element includes at least a bipolar transistor.

8. A semiconductor device as defined in Claim 4, characterized in that said semiconductor element includes at least a MOS transistor and a bipolar transistor.

9. A semiconductor device as defined in Claim 3, characterized in that said semiconductor element is a semiconductor element to which an external input is applied.

10. A semiconductor device as defined in Claim 3, characterized in that said semiconductor element forms a semiconductor memory, and that said semiconductor element having said p-n junction not forward-biased is a semiconductor element to which an external input is applied.

* C L M S *

REPLACEMENT SHEET
14 OCT 1999

11. A semiconductor integrated circuit device comprising:

(1) a substrate having a main surface;

(2) a first semiconductor region of a first conductivity type formed in a first portion of said main surface of said substrate, a first voltage being provided to said first semiconductor region;

(3) a second semiconductor region of said first conductivity type formed in a second portion of said main surface of said substrate, said second portion being different from said first portion, a second voltage being provided to said second semiconductor region;

(4) a third semiconductor region of a second conductivity type formed in a third portion in a main surface of said substrate and within said first semiconductor region, said second conductivity type being different from said first conductivity type, a third voltage being provided to said third semiconductor region;

(5) a fourth semiconductor region of said second conductivity type formed in a fourth portion of said main surface of said substrate, said fourth portion being different from said first and second portions, a fourth voltage being provided to said fourth semiconductor region;

(6) a first MISFET of a second conductivity type channel formed in said first semiconductor region;

(7) a second MISFET of a second conductivity type channel formed in said second semiconductor region;

(8) a third MISFET of a first conductivity type channel formed in said third semiconductor region; and

(9) a fourth MISFET of said first conductivity type channel formed in said fourth semiconductor region;

wherein said first and second voltages are different from each other, and wherein said third and fourth voltages are different from each other.

12 A semiconductor integrated circuit according to **claim 11**, wherein a memory cell is formed in said third semiconductor region, and wherein said memory cell comprises said third MISFET.

* C L M S *

REPLACEMENT SHEET
14 OCT 1993

13. A semiconductor integrated circuit according to **claim 12**, wherein said memory cell includes a capacitor element which is coupled to one of source and drain regions of said third MISFET.

14. A semiconductor integrated circuit according to **claim 12**, wherein said substrate is a semiconductor substrate of said second conductivity type, and wherein said third semiconductor region is electrically isolated from said substrate by said first semiconductor region.

15 A semiconductor integrated circuit according to **claim 12**, wherein a peripheral circuit is formed on said main surface of said substrate, and wherein said peripheral circuit comprises said first, second and third MISFETs.

16. A semiconductor integrated circuit according to **claim 11**, wherein an input protective element is formed in said third semiconductor region, and wherein said input protective element comprises said third MISFET.

17. A semiconductor integrated circuit according to **claim 16**, wherein a drain region of said third MISFET is electrically connected to an external via a resistance element.

18. A semiconductor integrated circuit according to **claim 15**, wherein said substrate is a semiconductor substrate of said second conductivity type, and wherein said third semiconductor region is electrically isolated from said substrate by said first semiconductor region.

19. A semiconductor integrated circuit according to **claim 16**, wherein a memory cell is formed in said fourth semiconductor region, and wherein said memory cell comprises said fourth MISFET.

20. A semiconductor integrated circuit according to **claim 11**, wherein a memory cell is formed in said fourth semiconductor region, and wherein said memory cell comprises said fourth MISFET.

21. A semiconductor integrated circuit device comprising:

(1) a substrate having a main surface;

* C L M S *

REPLACEMENT SHEET
14 OCT 1999

(2) a first semiconductor region of a first conductivity type formed in a first portion of said main surface of said substrate, a first voltage being provided to said first semiconductor region;

(3) a second semiconductor region of said first conductivity type formed in a second portion of said main surface of said substrate, said second portion being different from said first portion, a second voltage being provided to said second semiconductor region;

(4) a third semiconductor region of a second conductivity type formed in a third portion within said first portion, said second conductivity type being different from said first conductivity type, a third voltage being provided to said third semiconductor region;

(5) a fourth semiconductor region of said second conductivity type formed in a fourth portion of said main surface of said substrate, said fourth portion being different from said first and second portions, a fourth voltage being provided to said fourth semiconductor region;

(6) a first MISFET of a second conductivity type channel formed in said first semiconductor region;

(7) a second MISFET of said second conductivity type channel formed in said second semiconductor region;

(8) a third MISFET of a first conductivity type channel formed in said third semiconductor region;

(9) a fourth MISFET of said first conductivity type channel formed in said fourth semiconductor region; and

(10) a memory cell formed in said fourth semiconductor region, said memory cell comprising said fourth MISFET,

wherein said first and second voltages are different from each other, and wherein said third and fourth voltages are different from each other.

22. A semiconductor integrated circuit device according to **claim 21**, wherein said memory cell includes a capacitor element which is connected to one of source and drain regions of said fourth MISFET.

23. A semiconductor integrated circuit device comprising:
a semiconductor substrate having a main surface of a first conductivity type;

* C L M S *

REPLACEMENT SHEET
14 OCT 1999

a first semiconductor region of a second conductivity type, opposite to said first conductivity type, formed in said main surface of said semiconductor substrate;

a second semiconductor region of said first conductivity type formed in said first semiconductor region;

a first MISFET of said second conductivity type formed in a first region of said main surface of said semiconductor substrate, said first region being different from said first semiconductor region; and

a second MISFET of said second conductivity type formed in a surface of said second semiconductor region;

wherein a first voltage is to be applied to said first semiconductor region, a second voltage is to be applied to said second semiconductor region, and a third voltage is to be applied to said main surface of said semiconductor substrate, such that said first voltage is to be applied to said first semiconductor region for electrically isolating said second semiconductor region from said main surface of said semiconductor substrate, and wherein a value of said second voltage is to be different from that of said third voltage.

24. A semiconductor integrated circuit device according to **claim 23**, further comprising a third MISFET of said first conductivity type formed in a second region of a surface of said first semiconductor region,

wherein said second region is different from said second semiconductor region.

25. A semiconductor integrated circuit device according to **claim 23**, further comprising voltage devices for applying said first voltage, said second voltage and said third voltage.

26. A semiconductor integrated circuit device according to **claim 25**, wherein said first conductivity type is p-type and said second conductivity type is n-type, and wherein a value of said first voltage is greater than that of said second voltage and that of said third voltage.

27. A semiconductor integrated circuit device according to **claim 25**, further comprising a memory cell formed in said surface of said second semiconductor

REPLACEMENT SHEET
14 OCT 1999

region and a peripheral circuit formed in said first region of said main surface of said semiconductor substrate, wherein said memory cell includes said second MISFET and said peripheral circuit includes said first MISFET.

28. A semiconductor integrated circuit device according to **claim 27**, wherein said first conductivity type is p-type and said second conductivity type is n-type, and wherein a value of said first voltage is greater than that of said second voltage and that of said third voltage.

29. A semiconductor integrated circuit device according to **claim 25**, wherein said value of said second voltage is lower than that of said third voltage.

30. A semiconductor integrated circuit device according to **claim 29**, further comprising a bias generator coupled between a first power supply voltage and a second power supply voltage and for providing a bias voltage, formed in said main surface of said semiconductor substrate, wherein said second power supply voltage is lower than that of said first power supply voltage, and said bias voltage is lower than that of said second power supply voltage, and wherein said second voltage applied to said second semiconductor region corresponds to said bias voltage provided by said bias generator.

31. A semiconductor integrated circuit device comprising:
a semiconductor substrate having a main surface of a first conductivity type;
a first semiconductor region of a second conductivity type, opposite to said first conductivity type, formed in said main surface of said semiconductor substrate;
a second semiconductor region of said first conductivity type formed in said first semiconductor region;
a first MISFET of said second conductivity type formed in a first region of said main surface of said semiconductor substrate, said first region being different from said first semiconductor region;
a second MISFET of said second conductivity type formed in a surface of said second semiconductor region;
a first voltage device to apply a first voltage to said first semiconductor region;
a second voltage device to apply a second voltage to said second

REPLACEMENT SHEET
14 OCT 1999

semiconductor region; and

a third voltage device to apply a third voltage to said main surface of said semiconductor substrate,

such that said first voltage is applied to said first semiconductor region for electrically isolating said second semiconductor region from said main surface of said semiconductor substrate and wherein a value of said second voltage is different from that of said third voltage.

32. A semiconductor integrated circuit device comprising:

a semiconductor substrate having a main surface of a first conductivity type;

a first semiconductor region of a second conductivity type, opposite to said first conductivity type, formed in said main surface of said semiconductor substrate so as to form a first PN junction between said first semiconductor region and said main surface of said semiconductor substrate;

a second semiconductor region of said first conductivity type formed in said first semiconductor region so as to form a second PN junction between said second semiconductor region and said first semiconductor region;

a first MISFET of said second conductivity type formed in a first region of said main surface of said semiconductor substrate, said first region being different from said first semiconductor region; and

a second MISFET of said second conductivity type formed in a surface of said second semiconductor region,

wherein a first voltage is to be applied to said first semiconductor region, a second voltage is to be applied to said second semiconductor region, and a third voltage is to be applied to said main surface of said semiconductor substrate, so that said second PN junction is reverse biased by said first and second voltages, and said first PN junction is reverse biased by said first and second voltages, and wherein a value of said second voltage is to be different from that of said third voltage.

33. A semiconductor integrated circuit device according to **claim 32**, further comprising voltage devices for applying said first voltage, said second voltage and said third voltage.

REPLACEMENT SHEET
14 OCT 1999

34. A method of operating a semiconductor integrated circuit device, the semiconductor integrated circuit device comprising a semiconductor substrate having a main surface of a first conductivity type; a first semiconductor region of a second conductivity type, opposite to said first conductivity type, formed in said main surface of said semiconductor substrate; a second semiconductor region of said first conductivity type, formed in said first semiconductor region: a first MISFET of said second conductivity type formed in a first region of said main surface of said semiconductor substrate, said first region being different from said first semiconductor region; and a second MISFET of said second conductivity type formed in a surface of said second semiconductor region, said method comprising the steps of:
applying a first voltage to said first semiconductor region;
applying a second voltage to said second semiconductor region; and
applying a third voltage to said main surface of said semiconductor substrate,
wherein said first voltage electrically isolates said second semiconductor region from said main surface of said semiconductor substrate, and
wherein a value of said second voltage is different from that of said third voltage.

35. A method according to **claim 34**, wherein said first conductivity type is p-type and said second conductivity type is n-type, and wherein a value of said first voltage is greater than that of said second voltage and that of said third voltage.

36. A method according to **claim 34**, wherein said value of said second voltage is lower than that of said third voltage.

37. A method of operating a semiconductor integrated circuit device, the semiconductor integrated circuit device comprising a semiconductor substrate having a main surface of a first conductivity type; a first semiconductor region of a second conductivity type, opposite to said first conductivity type, formed in said main surface of said semiconductor substrate so as to form a first PN junction between said first semiconductor region and said main surface of said semiconductor substrate; a second semiconductor region of said first conductivity type formed in said first semiconductor region so as to form a

* C L M S *

REPLACEMENT SHEET
14 OCT 1999

second PN junction between said second semiconductor region and said first semiconductor region; a first MISFET of said second conductivity type formed in a first region of said main surface of said semiconductor substrate, said first region being different from said first semiconductor region; and a second MISFET of said second conductivity type formed in a surface of said second semiconductor region, said method comprising the steps of:

applying a first voltage to said first semiconductor region;

applying a second voltage to said second semiconductor region; and

applying a third voltage to said main surface of said semiconductor substrate,

wherein said second PN junction is reverse biased by said first and second voltages, and said first PN junction is reverse biased by said first and second voltages, and wherein a value of said second voltage is different from that of said third voltage.

38. A semiconductor integrated circuit device comprising:

a semiconductor substrate having a main surface of a first conductivity type;

a first semiconductor region of a second conductivity type, opposite to said first conductivity type, extending to said main surface of said semiconductor substrate so as to form a first PN junction with said main surface of said semiconductor substrate;

a second semiconductor region of said first conductivity type, in said first semiconductor region so as to form a second PN junction with said first semiconductor region, said second PN junction being surrounded by said first PN junction and being inside said first PN junction;

a first MISFET, having source and drain regions of said second conductivity type in a first portion of said main surface of said semiconductor substrate, said first portion being outside of said first PN junction;

a second MISFET, having source and drain regions of said second conductivity type in said second semiconductor region; and

structure for applying a first voltage to said first semiconductor region, a second voltage to said second semiconductor region, and a third voltage to said main surface of said semiconductor substrate, so that said second PN junction is reverse biased by said first and second voltages, and said first PN junction is reverse biased by said first and third voltages, and a value of said second

* C L M S *

REPLACEMENT SHEET
14 OCT 1999

voltage is different from that of said third voltage.

39. A semiconductor integrated circuit device according to **claim 38**, further comprising a third MISFET, having source and drain regions of said first conductivity type in a second portion of said first semiconductor region, wherein said second portion is different from said second semiconductor region.

40. A semiconductor integrated circuit device according to **claim 38**, wherein said first conductivity type is p-type and said second conductivity type is n-type, and wherein a value of said first voltage is greater than that of said second voltage and that of said third voltage.

41. A semiconductor integrated circuit device according to **claim 38**, further comprising a memory cell in said second semiconductor region, and a peripheral circuit in said first portion of said main surface of said semiconductor substrate, wherein said memory cell includes said second MISFET and said peripheral circuit includes said first MISFET.

42. A semiconductor integrated circuit device according to **claim 41**, wherein said first conductivity type is p-type and said second conductivity type is n-type, wherein a value of said first voltage is greater than that of said second voltage and that of said third voltage, and wherein said value of said second voltage is lower than that of said third voltage.

43. A semiconductor integrated circuit device according to **claim 41**, wherein said memory cell includes said second MISFET and a capacitor element which is electrically connected with one of said source and drain regions of said second MISFET.

44. A semiconductor integrated circuit device according to **claim 38**, further comprising a bias generator, coupled between a first power supply voltage and a second power supply voltage and for providing a bias voltage, in said main surface of said semiconductor substrate, wherein said second power supply voltage provides a voltage lower than that of said first power supply voltage, and said bias voltage is lower than that of said second power supply voltage, and

* C L M S *

REPLACEMENT SHEET
14 OCT 1999

wherein said second voltage applied to said second semiconductor region corresponds to said bias voltage provided by said bias generator.

45. A semiconductor integrated circuit device according to **claim 38**, having said first voltage applied to said first semiconductor region, said second voltage applied to said second semiconductor region, and said third voltage applied to said main surface of said semiconductor substrate, the value of the second voltage being different from that of said third voltage.

46. A semiconductor integrated circuit device comprising:

a semiconductor substrate having a main surface of a first conductivity type;

a first semiconductor region of a second conductivity type, opposite to said first conductivity type, extending to said main surface of said semiconductor substrate so as to form a first PN junction with said main surface of said semiconductor substrate;

a second semiconductor region of said first conductivity type in said first semiconductor region so as to form a second PN junction with said first semiconductor region, said second PN junction being surrounded by said first PN junction and being inside said first PN junction;

a first MISFET, having source and drain regions of said second conductivity type in a first portion of said main surface of said semiconductor substrate, said first portion being outside of said first PN junction;

a second MISFET, having source and drain regions of said second conductivity type in said second semiconductor region;

a first voltage device to apply a first voltage to said first semiconductor region;

a second voltage device to apply a second voltage to said second semiconductor region; and

a third voltage device to apply a third voltage to said main surface of said semiconductor substrate,

wherein a first voltage is applied to said first semiconductor region, a second voltage is applied to said second semiconductor region, and a third voltage is applied to said main surface of said semiconductor substrate, so that said second PN junction is reverse biased by said first and second voltages, and said first PN junction is reverse biased by said first and third voltages,and

REPLACEMENT SHEET
14 OCT 1999

wherein a value of said second voltage is different from that of said third voltage.

47. A semiconductor integrated circuit device according to **claim 46**, further comprising a third MISFET, having source and drain regions of said first conductivity type in a second portion of said first semiconductor region, wherein said second portion is different from said second semiconductor region.

48. A semiconductor integrated circuit device according to **claim 46**, wherein said first conductivity type is p-type and said second conductivity type is n-type, and wherein a value of said first voltage is greater than that of said second voltage and that of said third voltage.

49. A semiconductor integrated circuit device according to **claim 46**, further comprising a memory cell in said second semiconductor region and a peripheral circuit in said first portion of said main surface of said semiconductor substrate, wherein said memory cell includes said second MISFET and said peripheral circuit includes said first MISFET.

50. A semiconductor integrated circuit device according to **claim 49**, wherein said first conductivity type is p-type and said second conductivity type is n-type, wherein a value of said first voltage is greater than that of said second voltage and that of said third voltage, and wherein the value of said second voltage is lower than that of said third voltage.

51. A semiconductor integrated circuit device according to **claim 49**, wherein said memory cell includes said second MISFET and a capacitor element which is electrically connected with one of said source and drain regions of said second MISFET.

52. A semiconductor integrated circuit device according to **claim 46**, further comprising a bias generator, coupled between a first power supply voltage and a second power supply voltage and for providing a bias voltage, in said main surface of said semiconductor substrate, wherein said second power supply voltage is lower than that of said first power supply voltage, and said bias

* C L M S *

REPLACEMENT SHEET
14 OCT 1999

voltage is lower than that of said second power supply voltage and wherein said second voltage applied to said second semiconductor region corresponds to said bias voltage provided by said bias generator.

53. A semiconductor integrated circuit device comprising:

a semiconductor substrate of a first conductivity type, said semiconductor substrate having a first area, a second area other than said first area and a third area in said first area;

a first semiconductor region of a second conductivity type, opposite to said first conductivity type, in said first area of said semiconductor substrate so as to form a first PN junction with said semiconductor substrate;

a second semiconductor region of said first conductivity type, in said third area so as to form a second PN junction with said first semiconductor region, said second PN junction being surrounded by said first PN junction and being inside said first PN junction;

a first MISFET, having source and drain regions of said second conductivity type in said second area of said semiconductor substrate;

a second MISFET, having source and drain regions of said second conductivity type in said third area of said semiconductor substrate; and

structure for applying a first voltage to said first semiconductor region, a second voltage to said second semiconductor region, and a third voltage to said main surface of said semiconductor substrate, so that said second PN junction is reverse biased by said first and second voltages, and said first PN junction is reverse biased by said first and third voltages, and wherein a value of said second voltage is different from that of said third voltage.

54. A semiconductor integrated circuit device according to **claim 46**, having said first voltage applied to said first semiconductor region, said second voltage applied to said second semiconductor region, and said third voltage applied to said main surface of said semiconductor substrate, the value of the second voltage being different from that of said third voltage.

REPLACEMENT SHEET
14 OCT 1999

55(new). A semiconductor integrated circuit device comprising:

a semiconductor substrate having a main surface of a first conductivity type;

a first semiconductor region of a second conductivity type, opposite to said first conductivity type, extending to a first area of said main surface of said semiconductor substrate so as to form a first PN junction with said main surface of said semiconductor substrate;

a second semiconductor region of said first conductivity type in said first semiconductor region so as to form a second PN junction with said first semiconductor region, said second PN junction being surrounded by said first PN junction and being inside said
second first PN junction;

a third semiconductor region of said second conductivity type extending to a second area of said main surface of said semiconductor substrate so as to form a third PN junction with said main surface of said semiconductor substrate, said second area being a different area from said first area;

a fourth semiconductor region of said second conductivity type extending to a third area of said main surface of said semiconductor substrate so as to form a fourth PN junction with said main surface of said semiconductor substrate, said third area being a different area from said first area and said second area;

a first MISFET, having source and drain regions of said second conductivity type in a fourth area of said main surface of said semiconductor substrate, said fourth area being a different area from said first area , said second area and third area;

a memory cell, including a second MISFET having source and drain regions of said second conductivity type, said second MISFET being in said second semiconductor region;

a third MISFET, having source and drain regions of said first conductivity type in said third semiconductor region; and

a fourth MISFET, having source and drain regions of said first conductivity type in said fourth semiconductor region;

REPLACED
14 OCT 1999

a bias voltage generator in said main surface of said semiconductor substrate,

wherein a first voltage is applied to said first semiconductor region, a second voltage is applied to said second semiconductor region, a third voltage is applied to said third semiconductor region, a fourth voltage is applied to said fourth semiconductor region and a fifth voltage is applied to said main surface of said semiconductor substrate, so that said first PN junction is reverse biased by said first and fifth voltages, said second PN junction is reverse biased by said first and second voltages, said third PN junction is reverse biased by said third and fifth voltages and said fourth PN junction is reverse biased by said fourth and fifth voltages,

wherein said second and fourth voltages are provided by said bias voltage generator, and

wherein a value of said second voltage is different from that of said fifth voltage, and a value of said third voltage is different from that of said fourth voltage.

56(new). A semiconductor integrated circuit device according to claim 55, further comprising a peripheral circuit in said main surface of said semiconductor substrate, wherein said peripheral circuit includes said first MISFET.

57(new). A semiconductor integrated circuit device according to claim 55, wherein said first conductivity type is p-type and said second conductivity type is n-type.

58(new). A semiconductor integrated circuit device according to claim 55, further comprising a capacitor element in said main surface of said semiconductor substrate, wherein said capacitor element is coupled to one of said source and drain regions of said second MISFET.

59 (new). A semiconductor integrated circuit device comprising:

a semiconductor substrate having a main surface of a first

REPLACEMENT SHEET
14 OCT 1999

conductivity type;

a first semiconductor region of a second conductivity type, opposite to said first conductivity type, extending to a first area of said main surface of said semiconductor substrate so as to form a first PN junction with said main surface of said semiconductor substrate;

a second semiconductor region of said first conductivity type in said first semiconductor region so as to form a second PN junction with said first semiconductor region, said second PN junction being surrounded by said first PN junction and being inside said
second first PN junction;

a third semiconductor region of said second conductivity type extending to a second area of said main surface of said semiconductor substrate so as to form a third PN junction with said main surface of said semiconductor substrate, said second area being a different area from said first area;

a fourth semiconductor region of said second conductivity type extending to a third area of said main surface of said semiconductor substrate so as to form a fourth PN junction with said main surface of said semiconductor substrate, said third area being a different area from said first area and said second area;

a first MISFET, having source and drain regions of said second conductivity type in a fourth area of said main surface of said semiconductor substrate, said fourth area being a different area from said first area , said second area and third area;

a second MISFET having source and drain regions of said second conductivity type, said second MISFET being in said second semiconductor region;

a third MISFET, having source and drain regions of said first conductivity type in said third semiconductor region; and

a fourth MISFET, having source and drain regions of said first conductivity type in said fourth semiconductor region;

wherein a first voltage is applied to said first semiconductor region, a second voltage is applied to said second semiconductor region, a third voltage is applied to said third semiconductor region, a fourth voltage is applied to said fourth

REPLACEMENT SHEET
14 OCT 1999

semiconductor region and a fifth voltage is applied to said main surface of said semiconductor substrate, so that said first PN junction is reverse biased by said first and fifth voltages, said second PN junction is reverse biased by said first and second voltages, said third PN junction is reverse biased by said third and fifth voltages and said fourth PN junction is reverse biased by said fourth and fifth voltages,

wherein a value of said second voltage is set so that said source and drain regions of said second MISFET and said second semiconductor region may not be forward biased and a value of said second voltage is set so that said source and drain regions of said fourth MISFET and said fourth semiconductor region may not be forward biased,

wherein a value of said second voltage is lower than that of said fifth voltage.

60(new). A semiconductor integrated circuit device according to claim 59, wherein said first conductivity type is p-type and said second conductivity type is n-type.

61(new). A semiconductor integrated circuit device according to claim 59, wherein a value of said third voltage is different from that of said fourth voltage.

* C L M S *

REPLACEMENT SHEET
14 OCT 1999

SEMICONDUCTOR DEVICE

ABSTRACT:

The injection of minority carriers into a substrate caused by potential fluctuations ascribable to noise etc. is prevented.

In a semiconductor device which has sources and drains of insulated-gate field effect transistors or collectors, bases and emitters of bipolar transistors within a substrate and/or a plurality of isolation layers isolated in the substrate, voltages having values outside a varying range of applied voltages to respective electrodes of the source and drain or to the collector, base and emitter are applied to the substrate and the isolation layers.

FIGURE 2

THIS SHEET HAS BEEN REPLACED

This Sheet Has Been Replaced



REPLACEMENT SHEET
04 AUG 2000



62 . . A semiconductor integrated circuit device comprising:

a semiconductor substrate, of a first conductivity type, having a main surface;

a first semiconductor region of a second conductivity type, opposite to said first conductivity type, extending to said main surface of said semiconductor substrate so as to form a first PN junction with said semiconductor substrate;

a second semiconductor region of said first conductivity type, in said first semiconductor region so as to form a second PN junction with said first semiconductor region, said second PN junction being surrounded by said first PN junction and being inside said first PN junction;

a first MISFET, having source and drain regions of said second conductivity type in a first portion of said main surface of said semiconductor substrate, said first portion being outside of said first PN junction;

a second MISFET, having source and drain regions of said second conductivity type in said second semiconductor region; and

structure for applying a first voltage to said first semiconductor region, a second voltage to said second semiconductor region, and a third voltage to said main surface of said semiconductor substrate, so that said second PN junction is reverse biased by said first and second voltages, and said first PN junction is reverse biased by said first and third voltages, and a value of said second voltage is different from that of said third voltage, wherein said second semiconductor region is junction-isolated from said semiconductor substrate by said first semiconductor region.

63 . . A semiconductor integrated circuit device according to claim 62, further comprising a third MISFET, having source and drain regions of said first conductivity type in a second portion of said first semiconductor region, wherein said second portion is

* C L M S *

REPLACEMENT SHEET
04 AUG 2000

different from said second semiconductor region.

64 . A semiconductor integrated circuit device according to claim 62, wherein said first conductivity type is p-type and said second conductivity type is n-type, and wherein a value of said first voltage is greater than that of said second voltage and that of said third voltage.

65 . A semiconductor integrated circuit device according to claim 62, further comprising a memory cell in said second semiconductor region, and a peripheral circuit in said first portion of said main surface of said semiconductor substrate, and wherein said memory cell includes said second MISFET and said peripheral circuit includes said first MISFET.

66 . A semiconductor integrated circuit device according to claim 65, wherein said first conductivity type is p-type and said second conductivity type is n-type, wherein a value of said first voltage is greater than that of said second voltage and that of said third voltage, and wherein said value of said second voltage is lower than that of said third voltage.

67 . A semiconductor integrated circuit device according to claim 65, wherein said memory cell includes said second MISFET and a capacitor element which is electrically connected to one of said source and drain regions of said second MISFET.

68 . A semiconductor integrated circuit device according to claim 62, further comprising a bias generator circuit formed in said main surface of said semiconductor substrate and having a voltage input and a ground input thereto, said bias generator circuit providing said second voltage applied to said second semiconductor region, wherein ground potential of said ground input is lower than a voltage inputted by said voltage input, and wherein said second voltage applied to said second semiconductor region is lower than the ground potential.

REPLACEMENT SHEET
04 AUG 2000

69 . A semiconductor integrated circuit device according to claim 62, wherein said semiconductor substrate includes a semiconductor epitaxial layer of said first conductivity type on a semiconductor body of said first conductivity type.

70 . A semiconductor integrated circuit device according to claim 62, wherein said second PN junction is completely surrounded by said first PN junction both in plane view and in cross-sectional view.

71 . A semiconductor integrated circuit device comprising:

a semiconductor substrate, of a first conductivity type, having a main surface;

a first semiconductor region of a second conductivity type, opposite to said first conductivity type, extending to said main surface of said semiconductor substrate so as to form a first PN junction with said semiconductor substrate;

a second semiconductor region of said first conductivity type, in said first semiconductor region so as to form a second PN junction with said first semiconductor region, said second PN junction being surrounded by said first PN junction and being inside said first PN junction;

a first MISFET, having source and drain regions of said second conductivity type in a first portion of said main surface of said semiconductor substrate, said first portion being outside of said first PN junction;

a second MISFET, having source and drain regions of said second conductivity type in said second semiconductor region; and

a first voltage device to apply a first voltage to said first semiconductor region;

a second voltage device to apply a second voltage to said second semiconductor region; and

a third voltage device to apply a third voltage to said main surface of said semiconductor substrate, so that said second PN junction is reverse biased by said first and second voltages, and said first PN junction is reverse biased by said first and third voltages, wherein a value of said second voltage is different from

* C L M S *

REPLACEMENT SHEET
04 AUG 2000

that of said third voltage, and wherein said second semiconductor region is junction-isolated from said semiconductor substrate by said first semiconductor region.

72 . A semiconductor integrated circuit device according to claim 71, further comprising a third MISFET, having source and drain regions of said first conductivity type in a second portion of said first semiconductor region, wherein said second portion is different from said second semiconductor region.

73 . A semiconductor integrated circuit device according to claim 71, wherein said first conductivity type is p-type and said second conductivity type is n-type, and wherein a value of said first voltage is greater than that of said second voltage and that of said third voltage.

74 . A semiconductor integrated circuit device according to claim 71, further comprising a memory cell in said second semiconductor region, and a peripheral circuit in said first portion of said main surface of said semiconductor substrate, and wherein said memory cell includes said second MISFET and said peripheral circuit includes said first MISFET.

75 . A semiconductor integrated circuit device according to claim 74, wherein said first conductivity type is p-type and said second conductivity type is n-type, wherein a value of said first voltage is greater than that of said second voltage and that of said third voltage, and wherein said value of said second voltage is lower than that of said third voltage.

76 . A semiconductor integrated circuit device according to claim 74, wherein said memory cell includes said second MISFET and a capacitor element which is electrically connected to one of said source and drain regions of said second MISFET.

77 . A semiconductor integrated circuit device according to claim 71, further comprising a bias generator circuit formed in

REPLACEMENT SHEE
04 AUG 2000

said main surface of said semiconductor substrate and having a voltage input and a ground input thereto, said bias generator circuit providing said second voltage applied to said second semiconductor region, wherein ground potential of said ground input is lower than a voltage inputted by said voltage input, and wherein said second voltage applied to said second semiconductor region is lower than the ground potential.

78 . A semiconductor integrated circuit device according to claim 71, wherein said semiconductor substrate includes a semiconductor epitaxial layer of said first conductivity type on a semiconductor body of said first conductivity type.

79 . A semiconductor integrated circuit device according to claim 71, wherein said second PN junction is completely surrounded by said first PN junction both in plane view and in cross-sectional view.

80 . A semiconductor integrated circuit device comprising:

a semiconductor substrate of a first conductivity type, said semiconductor substrate having a first area, a second area other than said first area and a third area in said first area;

a first semiconductor region of a second conductivity type, opposite to said first conductivity type, in said first area of said semiconductor substrate so as to form a first PN junction with said semiconductor substrate;

a second semiconductor region of said first conductivity type, in said third area so as to form a second PN junction with said first semiconductor region, said second PN junction being surrounded by said first PN junction and being inside said first PN junction;

a first MISFET, having source and drain regions of said second conductivity type in said second area of said semiconductor substrate;

a second MISFET, having source and drain regions of said second conductivity type in said third area of said semiconductor substrate; and

REPLACEMENT SHEET
04 AUG 2000

structure for applying a first voltage device to said first semiconductor region, a second voltage to said second semiconductor region, and a third voltage to said semiconductor substrate, so that said second PN junction is reverse biased by said first and second voltages, and said first PN junction is reverse biased by said first and third voltages, wherein a value of said second voltage is different from that of said third voltage, and wherein said second semiconductor region is junction-isolated from said semiconductor substrate by said first semiconductor region.

81 A semiconductor integrated circuit device comprising:

a semiconductor substrate, of a first conductivity type, having a main surface;

a first semiconductor region of a second conductivity type, opposite to said first conductivity type, extending to said main surface of said semiconductor substrate so as to form a first PN junction with said semiconductor substrate;

a second semiconductor region of said first conductivity type, in said first semiconductor region so as to form a second PN junction with said first semiconductor region, said second PN junction being surrounded by said first PN junction and being inside said first PN junction;

a third semiconductor region of said first conductivity type extending to a first portion of said main surface of said semiconductor substrate, said first portion being outside of said first PN junction;

a first MISFET, having source and drain regions of said second conductivity type in said first portion of said main surface of said semiconductor substrate; and

a second MISFET, having source and drain regions of said second conductivity type in said second semiconductor region,

wherein a first voltage is applied to said first semiconductor region, a second voltage is applied to said second semiconductor region, and a third voltage is applied to said third semiconductor region,

wherein said first PN junction is reverse biased, and said

REPLACEMENT SHEET
04 AUG 2000

second PN junction is reverse biased,

wherein a value of said second voltage is different from that of said third voltage, and

wherein said second semiconductor region is junction-isolated from said semiconductor substrate by said first semiconductor region.

82 . A semiconductor integrated circuit device according to claim 81, further comprising a peripheral circuit in said main surface of said semiconductor substrate, wherein said peripheral circuit includes said first MISFET.

83 . A semiconductor integrated circuit device according to claim 81, wherein said first conductivity type is p-type and said second conductivity type is n-type.

84 . A semiconductor integrated circuit device according to claim 71, further comprising a capacitor element in said main surface of said semiconductor substrate, wherein said capacitor element is coupled to one of said source and drain regions of said second MISFET.

85 . A semiconductor integrated circuit device according to claim 81, wherein said semiconductor substrate includes a semiconductor epitaxial layer of said first conductivity type on a semiconductor body of said first conductivity type.

86 . A semiconductor integrated circuit device according to claim 81, wherein said second PN junction is completely surrounded by said first PN junction both in plane view and in cross-sectional view.

87 . A semiconductor integrated circuit device according to claim 81, wherein said first MISFET is in said third semiconductor region.

88 . A semiconductor integrated circuit device according to

REPLACEMENT SHEET
04 AUG 2000

claim 87, wherein said second semiconductor region is junction-isolated from said third semiconductor region by said first semiconductor region.

89 . A semiconductor integrated circuit device comprising:

a semiconductor substrate, of a first conductivity type, having a main surface;

a first semiconductor region of a second conductivity type, opposite to said first conductivity type, extending to said main surface of said semiconductor substrate so as to form a first PN junction with said semiconductor substrate;

a second semiconductor region of said first conductivity type, in said first semiconductor region so as to form a second PN junction with said first semiconductor region, said second PN junction being surrounded by said first PN junction and being inside said first PN junction;

said semiconductor substrate having a first portion, outside of said first PN junction, extending to said main surface of said semiconductor substrate, said first portion having higher impurity concentration than, and being of the same conductivity type as, a remaining portion of said semiconductor substrate;

a first MISFET, having source and drain regions of said second conductivity type in said first portion of said semiconductor substrate; and

a second MISFET, having source and drain regions of said second conductivity type in said second semiconductor region,

wherein a first voltage is applied to said first semiconductor region, a second voltage is applied to said second semiconductor region, and a third voltage is applied to said first portion of said semiconductor substrate,

wherein said first PN junction is reverse biased, and said second PN junction is reverse biased,

wherein a value of said second voltage is different from that of said third voltage, and

wherein said second semiconductor region is junction-isolated from said semiconductor substrate by said first semiconductor region.

* C L M S *

REPLACEMENT SHEET
04 AUG 2000

90 . A semiconductor integrated circuit device according to claim 89, further comprising a peripheral circuit in said main surface of said semiconductor substrate, wherein said peripheral circuit includes said first MISFET.

91 . A semiconductor integrated circuit device according to claim 89, wherein said first conductivity type is p-type and said second conductivity type is n-type.

92 . A semiconductor integrated circuit device according to claim 89, further comprising a capacitor element in said main surface of said semiconductor substrate, wherein said capacitor element is coupled to one of said source and drain regions of said second MISFET.

93 . A semiconductor integrated circuit device according to claim 89, wherein said second semiconductor region is junction-isolated from said third semiconductor region by said first semiconductor region.

REPLACEMENT SHEET
04 AUG 2000

SEMICONDUCTOR DEVICE

ABSTRACT:

The injection of minority carriers into a substrate caused by potential fluctuations ascribable to noise etc. is prevented.

In a semiconductor device which has sources and drains of insulated-gate field effect transistors or collectors, bases and emitters of bipolar transistors within a substrate and/or a plurality of isolation layers isolated in the substrate, voltages having values outside a varying range of applied voltages to respective electrodes of the source and drain or to the collector, base and emitter are applied to the substrate and the isolation layers.

FIGURE 2