

CLAIMS

What is claimed is:

1. A method of dicing a semiconductor wafer comprising a plurality of integrated circuits, the
5 method comprising:
 - forming a mask above the semiconductor wafer;
 - patterning the mask and the semiconductor wafer with a first laser process;
 - patterning the mask and the semiconductor wafer with a second laser process, wherein
the second laser process is different than the first laser process; and
 - 10 etching the semiconductor wafer with a plasma etching process to singulate the integrated
circuits.
2. The method of claim 1, wherein the first laser process has a first intensity and the second laser
process has a second intensity, and wherein the second intensity is greater than the first intensity.
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3. The method of claim 2, wherein a ratio of the second intensity to the first intensity is
approximately 3:1 or greater.
4. The method of claim 2, wherein the second intensity is approximately 6μJ or greater, and
20 wherein the first intensity is approximately 3μJ or smaller.
5. The method of claim 1, wherein there is substantially no recession at an interface between the
mask and the semiconductor wafer after the first laser process.
- 25 6. The method of claim 1, wherein the first laser process and the second laser process form a first
opening through the mask and a second opening through a device layer of the semiconductor
wafer.
7. The method of claim 6, wherein the first opening is substantially aligned with the second
30 opening.
8. The method of claim 6, wherein a maximum width of the second opening is smaller than a
minimum width of the first opening.

9. The method of claim 1, wherein the first laser process forms an opening through the mask and into a device layer of the semiconductor wafer, and wherein the second laser process extends the opening through the device layer.
- 5 10. The method of claim 1, further comprising:
a plasma cleaning operation between the second laser process and the plasma etching process.
11. The method of claim 1, wherein the laser has a pulse width between 10 femtoseconds and
10 100 picoseconds.
12. A method of dicing a semiconductor wafer comprising a plurality of integrated circuits, comprising:
forming a mask over the semiconductor wafer;
15 performing a first laser process to form an opening through the mask and into a device layer of the semiconductor wafer; and
performing a second laser process to singulate the plurality of integrated circuits.
13. The method of claim 12, wherein the first laser process has a first intensity and the second
20 laser process has a second intensity, wherein the second intensity is greater than the first intensity.
14. The method of claim 13, wherein a ratio of the second intensity to the first intensity is approximately 3:1 or greater.
- 25 15. The method of claim 13, wherein the second intensity is approximately 6 μ J or greater, and wherein the first intensity is approximately 3 μ J or smaller.
16. The method of claim 13, wherein there is substantially no recession of the mask at an
30 interface between the mask and the semiconductor wafer after the first laser process.
17. The method of claim 16, wherein there is a recession of the mask at the interface between the mask and the semiconductor wafer after the second laser process.

18. The method of claim 17, wherein a maximum width of an opening through the semiconductor wafer is smaller than a minimum width through the mask.

19. A system for dicing a semiconductor wafer comprising a plurality of integrated circuits, the
5 system comprising:

a factory interface;

a laser scribe apparatus coupled with the factory interface and comprising a laser
assembly configured to provide a first laser process and a second laser process; and

a plasma etch chamber coupled with the factory interface.

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20. The system of claim 19, wherein the first laser process has a first intensity and the second
laser process has a second intensity, wherein the second intensity is greater than the first
intensity.