

ABSTRACT

Provided herein may be a memory device. The memory device may include a memory block configured to include a first selection line, word lines, a second selection line, a channel layer, first select transistors, second select
5 transistors, and memory cells; a voltage generator configured to generate a turn-on voltage and a turn-off voltage to be applied to the first and second selection lines, and generate a program voltage and a pass voltage to be applied to word lines; a source line driver configured to generate a precharge voltage to be applied to the source line; a page buffer group
10 configured to apply a program-enable voltage and a program-inhibit voltage to bit lines; and a control circuit configured to determine a reference position and control the voltage generator, the source line driver, and the page buffer group to adjust time required to precharge the channel layer.

15 FIG. 7