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Abstract

FeRAM memory device

A FeRAM memory chip comprises an array 5 of non-volatile ferrocapacitor memory cells for storing data. Input pins receive data to be stored, and address data indicating where in the array of memory cells the data should be stored. The FeRAM memory chip further has a reset unit 7 for recognising an externally applied reset signal. The reset unit 7, upon recognition of the reset signal, initiates a reset operation in which at least a portion of the data stored in the memory cells is set to predetermined values.

10 [Fig. 2]