

PATENT SPECIFICATION

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DRAWINGS ATTACHED.

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COMPLETE SPECIFICATION.

Process for Packaging Multilead Semiconductor Devices and Resulting Product.

We, TEXAS INSTRUMENTS INCORPORATED, a Corporation organised according to the laws of the State of Delaware, United States of America, of 13500 North Central Expressway, Dallas, Texas, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates generally to semiconductor devices, and more particularly relates to semiconductor devices having a large number of external leads.

In an integrated circuit, a number of active semiconductor devices are formed on a chip of silicon and interconnected in place by thin film leads to form a complete circuit. Logic gates and flip-flop circuits having ten to fourteen leads have been extensively manufactured and sold. As integrated circuit technology has advanced over the past several years, yields have increased to the point that large arrays of the logic circuits can be produced on a single semiconductor slice nominally one and one-eighth inches in diameter. Second and third level interconnections can then be used to interconnect the individual circuits as desired and provide bonding pads at the edge of the slice. However, these circuit arrays usually require a large number of external connections, typically about one hundred and fifty. Conventional multilead packaging methods and devices are definitely limited as to the number of external leads practical both during fabrication of the devices and during

subsequent use of the devices by the ultimate consumer. For example, the standard flat pack generally has from ten to twenty leads, which are commonly referred to as pins, and the packages which utilize a ceramic substrate upon which a number of individual integrated circuit chips are mounted is usually limited to twenty or thirty pins, with forty being a maximum as a practical matter. In addition, the standard packaging techniques require ball bonded lead wires to interconnect the bonding pads formed on the surface of the monolithic semiconductor body. This is not only an expensive procedure, but results in two impedance discontinuities which degrade high speed performance.

According to the present invention there is provided a multilead package for a multilead semiconductor device, comprising a support member including an opening formed therein and a multilead semiconductor device positioned at least partly within the opening, spaced electrically conductive strips secured to one surface of the support member, the conductive strips each having one end that overlaps the periphery of the said opening, engaging and electrically connecting with a contact on one surface of the semiconductor device to provide electrical access thereto from a distal end of that conductive strip, the said conductive strips extending away from the said opening to distal ends at respective locations at or closely within the periphery of the support member, and in which the distance between the centres of the distal ends of any two adja-

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SEE ERRATA SLIP ATTACHED

cent ones of the conductive strips is not less than the distance between the centres of those conductive strips at the said one ends thereof.

- 5 More specifically, the support may comprise a sheet of insulating material, such as standard insulating circuit board, having an opening therethrough. A thin continuous sheet of metal is bonded to the front
10 side of the sheet of insulating material such that the sheet extends over the opening. Both sides of the metal sheet are protected by photo-resist, and the photo-resist is then patterned on one side and the metal sheet
15 etched, such as by conventional photolithographic and etching techniques, to form the lead strips. The integrated circuit chip or slice is then inserted into the opening from the backside and the bonding pads on the
20 surface of the semiconductor body aligned with and bonded to the overhanging lead strips.

- The lead strips formed on the surface of the insulating sheet may extend to predetermined spaced positions along the edge of the insulating sheet such that the edge of the insulating sheet may be inserted in a
25 standard printed circuit board connector. Or, the lead strips formed on the surface of the insulating sheet may extend to pins disposed perpendicular to the insulating sheet, the pins being adapted to plug into mating
30 receptacles or sockets. Any one of the structures presently described may be encapsulated in whole or in part in a suitable potting plastics or other potting material to provide protection from the ambient and to
35 provide mechanical stability.

- The sheet of insulation may be substantially the same thickness as the semiconductor device so that a stiffening sheet may be bonded to the backside of both the semiconductor device and the insulating sheet
40 to lend further structural rigidity and stability. The stiffening sheet may be metal and a good thermal conductor to serve as a heat sink for the semiconductor device, and if desired, to serve as an electrical ground plane or other electrical function.
45

- The invention may best be understood by reference to the following detailed description of illustrative embodiments, when read in conjunction with the accompanying drawings, wherein:
50

- 55 Figure 1 is a sectional view illustrating an intermediate step in the process of the present invention;

- 60 Figure 2 is a plan view illustrating another intermediate step in the process of the present invention;

- 65 Figure 3 is a sectional view similar to Figure 1 illustrating still another step in the process of the present invention and a package constructed in accordance with this invention;

Figure 4 is a plan view of another package fabricated in accordance with the process of the present invention at an intermediate stage of fabrication;

Figure 5 is a sectional view taken substantially on lines 5—5 of Figure 4;

Figure 6 is a side view, partially broken away, of still another package fabricated in accordance with the present invention;

Figure 7 is a sectional view taken substantially on lines 7—7 of Figure 6;

Figure 8 is a plan view of still another package constructed in accordance with the present invention, the device being shown at an intermediate stage of fabrication;

Figure 9 is a sectional view taken substantially on lines 9—9 of Figure 8, but after completion of the package;

Figures 10 and 11 illustrate the method of the present invention as applied to the packaging of a slice having circuits formed on both faces; and

Figures 12 and 13 are sectional views illustrating an alternative method for packaging a slice having circuits formed on both faces.

The present invention can best be understood in connection with Figures 1, 2 and 3. The starting material is a dielectric sheet 10 having surfaces 12 and 14. The dielectric sheet 10 may be formed from substantially any material commonly used for printing circuits, such as epoxy impregnated fiber glass fabric, phenolic printed circuit board, etc. or, if desired, may be a metal sheet with an insulated coating thereon. A cavity is formed in the surface 12 of the dielectric sheet 10 for receiving an integrated circuit device which will presently be described. The cavity is preferably formed by an opening 16 which extends completely through the sheet 10 and which may be formed by punching or any other suitable process.

Next, a continuous conductive sheet 18 is bonded to the surface 12 and extends over the opening 16. The conductive sheet 18 may be any suitable metal, such as copper, and may be bonded to the dielectric sheet 10 using any conventional process such as, for example, the process as used to fabricate printed circuit board stock. The conductive sheet 18 may be coextensive with one or more edges of the dielectric sheet 10, or may terminate short of one or more edges, depending upon the package to be fabricated as will hereafter be described.

The conductive layer 18 is then patterned to form a plurality of lead strips 20, such as illustrated in Figures 2 and 3. This may be accomplished by coating both the upper and lower surfaces 18a and 18b of the sheet 18 with photo resist material. Only the photo resist on the upper surface 18a need be exposed to the pattern. When the photo resist is developed, the upper surface 18a

of the metal layer 18 will then be protected in areas where the metal sheet is to be retained to form strip leads, and is exposed in all areas where it is to be removed. Then the entire assembly is immersed in a suitable selective etchant for the particular metal forming the sheet 18 and the metal is removed in all areas except where protected by the photo resist on the upper surface 18a. The photo resist on the lower surface 18b limits the etching process to the upper surface. As will be noted in Figure 2, the lead strips are formed such that the ends 20a extend over the edge of the cavity formed by the opening 16. The other ends 20b preferably extend to and terminate at one straight edge 22 of the dielectric sheet 10. Note that the spacing between the ends 20b is at least as large as the spacing between the ends 20a.

Next, a semiconductor slice 24 is inserted in the opening 16 from the underside of the dielectric sheet 10 so as not to disturb the ends 20a of the strip leads. The semiconductor device 24 may be an entire semiconductor slice, which is nominally about one and one-eighth inches in diameter and about 0.010 inch thick on which an array of many logic circuits may be formed. At this point it should be noted that the drawings are not necessarily to scale, but are merely illustrative of the process of the ultimate package. It should be understood that the number of strip leads 20 may be increased substantially as required. The large number of components such as diodes, transistors, resistors, and capacitors formed in the semiconductor slice are interconnected into circuits and arrays of circuits by one or more layers of conductors fabricated using conventional thin film techniques. However, for each connection that is to be made to a circuit externally of the device 24, a bonding pad is formed on the surface of the device, and the bonding pads are arranged on the slice so that all can be simultaneously aligned with and positioned under the overhanging ends 20a of the lead strips 20. After the device 24 is so aligned, the ends 20a of the lead strips are then bonded to the bonding pad using conventional ultrasonic welding or thermocompression welding techniques.

The entire structure is then preferably encapsulated in a suitable potting compound 26 as represented by the dotted outline in Figures 2 and 3 to produce a completed package 30. It will be noted that the lower edge of the dielectric sheet 10 and the ends 20b of the lead strips remain exposed for connection to external circuitry either by soldering, welding, or by a conventional printed circuit board connector which fits over the edge of the printed circuit board

and provides a pressure contact between the ends 20b and a mating lead.

A package constructed in accordance with another example of the present invention is indicated generally by the reference numeral 40 in Figures 4 and 5. The package 40 has a dielectric sheet 42 with a rectangular opening 44 formed therein. A plurality of tapered strip conductors 46 have narrow ends 46a which overhang the opening 44 and are bonded to bonding pads on the surface of an integrated circuit chip 48 disposed within the opening 44. A conductive pin 50 extends perpendicularly through the wider ends 46b of each of the conductor strips 46, through the dielectric sheet 42, and protrudes from the lower face of the package 40. The ends 46b are, in general, spaced apart by distances greater than the distances between the corresponding ends 46a. The pins 50 are so sized and spaced as to be plugged into a mating female receptacle. The conductor strips 46, chip 48 and dielectric sheet 42 may then be encapsulated in a suitable potting plastics material 52. The package 40 may be fabricated using the same process as that described in connection with fabrication of the package 30 illustrated in Figure 3, except of course for the pins 50. The dielectric sheet 42 may typically comprise a thin ceramic sheet into which the pins 50 are inserted using conventional techniques.

Another package constructed in accordance with the present invention is indicated generally by the reference numeral 60 in Figures 6 and 7. The package 60 is quite similar to the package 30 illustrated in Figures 2 and 3 and includes a dielectric sheet 62. A plurality of strip conductors 64 are formed on the upper surface of sheet 62, and the ends 64a overhang an opening 66 formed in the dielectric sheet 62. The ends 64a are bonded to bonding pads on a semiconductor device 68 disposed in the opening 66. However, in the package 60 the dielectric sheet 62 is the same thickness as the semiconductor slice 68, and a stiffening sheet 70 is bonded to the backside of the dielectric sheet 62 and to the backside of the semiconductor slice 68 by a suitable adhesive. The backing sheet 70 lends structural rigidity and stability to the package 60, and is preferably fabricated from metal or other material having good thermal conductivity so as to transfer heat from the semiconductor device 68. Both the strip conductors 64 and the backing sheet 70 may extend to the edge 62a of the dielectric sheet 62. The edge 62a may then be inserted in a suitable connector adapted to provide both electrical and thermal transfer to the lead strips 64 and the backing sheet 70. The entire device may then be encapsulated in a suitable potting plastics material 72 except

4 along the edge 62a so as to seal the active
portions of the device from the ambient
while still permitting electrical and thermal
contact to be made through the conductor
5 strip 64 and the backing sheet 70. The
backing sheet 70 may be either electrically
insulated from or in electrical contact with
the semiconductor device 68, as desired, de-
pending upon the type of bonding agent used.

10 Another package constructed in accord-
ance with the present invention is indicated
generally by the reference numeral 80 in
Figures 8 and 9. The package 80 comprises
15 a dielectric sheet 82 with an aperture 84
formed therein. A large number of tapered
lead strips 86 extend from the four edges
of the dielectric sheet 82 radially inwardly so
that the narrow ends 86a of the strips ex-
20 tend over the opening 84 and over a semi-
conductor slice 88 disposed within the open-
ing 84. The dielectric sheet 82 and the
slice 88 are preferably of substantially the
same thickness, and a backing sheet 90 is
25 bonded to the faces of the dielectric sheet
82 and semiconductor slice 88 opposite from
the strip leads 86. The backing plate 90
serves to stiffen the structure, and may also
be used as a heat transfer media to a heat
30 sink upon which the device is positioned, as
well as a ground plane or ground terminal
if desired. A suitable potting material 92,
such as plastics material, is then placed over
and around the semiconductor slice 88 by
35 applying the potting material in paste form
to the slice 88 and then curing the potting
material. Thus, no mold is required in
order to encapsulate the slice 88. It should
be pointed out that the packages 30, 40 and
40 60 may also be potted in the same manner
without the use of a mold if desired. It
will be evident that the package 80 can be
fabricated using the process heretofore de-
scribed.

45 It will be appreciated by those skilled in
the art that although the positions of the
circuits on the slice 88, and therefore the
positions of the various bonding pads which
must be mated with the ends 86a of the
lead strips 86, are arranged in a precisely
50 predetermined pattern, the pattern itself is
somewhat randomly oriented with respect to
the edge of the slice 88. For this reason,
the aperture 84 is made somewhat larger
than the slice 88 so that the slice 88 may
55 be moved about within the aperture until
the bonding pads register with the ends 86a
of the strip leads.

60 In accordance with another important
aspect of the invention, a slice of semi-
conductor material having circuit arrays
formed on both faces may be packaged
using the method illustrated in Figures 10
and 11. A semiconductor slice 120 has
65 circuits formed in the upper and lower faces
120a and 120b. Expanded contact pads,

represented at 122a and 122b, are exposed
on the faces 120a and 120b, respectively,
and are preferably aligned in predetermined
relationship. The slice 120 is sandwiched
between a pair of package halves indicated
generally by the reference numerals 124 and
126. The package half 124 is substantially
identical to the packaging devices hereto-
fore described and comprises an insulating
sheet frame 128, which may be a conven-
75 tional printed circuit board, having an ap-
erture 130 for receiving the slice 120, and a
large number of radially extending leads 132
cantilevered over the opening 130. The
frame 128 preferably has a thickness equal
80 to about one-half the thickness of the slice
120. The package half 126 is identical to the
package half 124 and is comprised of an in-
sulating frame sheet 134 having an opening
136 and radially extending cantilevered
85 leads 138.

To assemble the package, the slice 120 is
placed between the package halves 124 and
126, substantially as illustrated in Figure
10. It will be noted that the package halves
90 are oriented such that the insulating sheets
128 and 134 are facing the slice 120, with
the leads 132 and 138 facing away from the
slice. Then the package halves 124 and 126
are brought together as illustrated in Figure
95 11 and aligned so that the leads 132 and
138 will be in the same predetermined rela-
tionship as the expanded contact pads 122a
and 122b on the slice 120. The package
halves may then be bonded together along
100 the abutting faces by a bonding agent re-
presented at 150. The slice 120 can then be
manipulated between the leads 132 and 138,
such as by a vacuum tool 152 indicated in
dotted outline in Figure 11, until the con-
105 tact pads 122a are aligned with the ends of
the leads 132. The contact pads 122b will
then be aligned with the leads 138. The
leads 132 and 138 can then be welded to
the expanded contact pads 122a and 122b,
110 respectively, using the techniques heretofore
described. The slice can then be encap-
sulated in a suitable epoxy or other material,
as represented by the dotted outline 154.

115 An alternative method for assembling the
package is to first mate the package half 124
to the slice 120 by aligning and welding the
leads 132 to the contact pads 122a. Then
the package half 126 is mated with the slice
120 by aligning and welding the leads 138
120 to the contact pads 122b. As before, the
slice may then be encapsulated in a suitable
epoxy or other material as represented by
the dotted outline 154.

125 An alternative method for packaging the
slice 120 is illustrated in Figures 12 and 13.
Again, an insulating sheet 160 has an open-
ing 162 therein so that the sheet forms an
insulating frame adapted to receive the slice
120. The sheet 160 is preferably as thick as,
130

or slightly thicker than, the slice 120, substantially as illustrated in the drawings. A lead pattern 164, identical to the lead pattern 132, for example, is formed on one surface of the insulating sheet 160, and the same lead pattern 166 is formed on the other surface, except that the leads of the pattern 166 do not extend over the opening 162. This structure may be fabricated by first bonding a metal sheet to the underside of the insulating sheet 160 and patterning the sheet to form the leads 166, then bonding a sheet to the topside of the insulating sheets 160 and patterning the sheet to form the leads 164. Then the leads 164 are again mated with and welded to the contact pads 122a as illustrated in Figure 12. The assembly may then be inverted and whisker lead wires 168 ball bonded between the contact pads 122b and 166. The device may then be encapsulated in epoxy 170, or other suitable material to complete the device.

From the above detailed description, it will be appreciated by those skilled in the art that a highly useful process has been described for packaging integrated circuit arrays and other semiconductor devices requiring a large number of leads. The process is relatively simple and inexpensive and is amenable to use on a mass production basis. The process eliminates the use of ball bonded lead wire connections, thus simplifying and economizing the process. The number of connections internally of the package is also reduced to one, rather than two as is the case when the bonding pads of the semiconductor device are connected to the external leads by very fine ball bonded jumper wires, thus reducing the number of impedance discontinuities and improving high frequency performance. The devices resulting from the process can be fabricated so as to be compatible with standard printed circuit connectors, with standard multisolet connectors, or with standard flat pack connectors. The number of leads may be very large, one hundred fifty leads being readily obtainable. The devices may be fabricated so as to have a good thermal transfer path to remove heat dissipated in the semiconductor device.

Although preferred embodiments of the invention have been described in detail, it is to be understood that various changes, substitutions and alterations can be made therein without departing from the scope of the invention as defined by the appended claims.

WHAT WE CLAIM IS:—

1. A multilead package for a multilead semiconductor device, comprising a support member including an opening formed therein and a multilead semiconductor device positioned at least partly within the open-

ing, spaced electrically conductive strips secured to one surface of the support member, the conductive strips each having one end that overlaps the periphery of the said opening engaging and electrically connecting with a contact on one surface of the semiconductor device to provide electrical access thereto from a distal end of that conductive strip, the said conductive strips extending away from the said opening to distal ends at respective locations at or closely within the periphery of the support member, and in which the distance between the centres of the distal ends of any two adjacent ones of the conductive strips is not less than the distance between the centres of those conductive strips at the said one ends thereof.

2. A multilead package as claimed in claim 1, in which the distance between the centres of the distal ends of any two adjacent ones of the conductive strips is greater than the distance between the centres of those conductive strips at the said one ends thereof.

3. A multilead package as claimed in claim 2, wherein the said distal ends of the said conductive strips are wider than the said one ends thereof.

4. A multilead package as claimed in claim 3, wherein the said distal ends are formed as enlarged area lands.

5. A multilead package as claimed in claim 4, and further including electrically conductive pins electrically connected to the said distal ends of the conductive strips and extending perpendicularly to the one surface of the support member.

6. A multilead package as claimed in any preceding claim, wherein the support member has at least one straight edge to which the said conductive strips extend.

7. A multilead package as claimed in claim 3, wherein the said conductive strips extend radially from the opening in the support member.

8. A multilead package as claimed in claim 7, in which the said conductive strips comprise the totality of the conductive strips secured to the support member, and in which the conductive strips terminate at peripheral edges of the support member.

9. A multilead package as claimed in any of claims 1, 2, 3, and 6, and further including a member of thermally conductive material attached to the surface of the support member opposite that to which the said conductive strips are secured and positioned in thermal transfer relation with the semiconductor device.

10. A multilead package as claimed in any of claims 1, 2, 3, and 6, and further including a second support member having an opening formed therein and a second plurality of electrically conductive strips

or slightly thicker than, the slice 120, substantially as illustrated in the drawings. A lead pattern 164, identical to the lead pattern 132, for example, is formed on one surface of the insulating sheet 160, and the same lead pattern 166 is formed on the other surface, except that the leads of the pattern 166 do not extend over the opening 162. This structure may be fabricated by first bonding a metal sheet to the underside of the insulating sheet 160 and patterning the sheet to form the leads 166, then bonding a sheet to the topside of the insulating sheets 160 and patterning the sheet to form the leads 164. Then the leads 164 are again mated with and welded to the contact pads 122a as illustrated in Figure 12. The assembly may then be inverted and whisker lead wires 168 ball bonded between the contact pads 122b and 166. The device may then be encapsulated in epoxy 170, or other suitable material to complete the device.

From the above detailed description, it will be appreciated by those skilled in the art that a highly useful process has been described for packaging integrated circuit arrays and other semiconductor devices requiring a large number of leads. The process is relatively simple and inexpensive and is amenable to use on a mass production basis. The process eliminates the use of ball bonded lead wire connections, thus simplifying and economizing the process. The number of connections internally of the package is also reduced to one, rather than two as is the case when the bonding pads of the semiconductor device are connected to the external leads by very fine ball bonded jumper wires, thus reducing the number of impedance discontinuities and improving high frequency performance. The devices resulting from the process can be fabricated so as to be compatible with standard printed circuit connectors, with standard multisolet connectors, or with standard flat pack connectors. The number of leads may be very large, one hundred fifty leads being readily obtainable. The devices may be fabricated so as to have a good thermal transfer path to remove heat dissipated in the semiconductor device.

Although preferred embodiments of the invention have been described in detail, it is to be understood that various changes, substitutions and alterations can be made therein without departing from the scope of the invention as defined by the appended claims.

WHAT WE CLAIM IS:—

1. A multilead package for a multilead semiconductor device, comprising a support member including an opening formed therein and a multilead semiconductor device positioned at least partly within the open-

ing, spaced electrically conductive strips secured to one surface of the support member, the conductive strips each having one end that overlaps the periphery of the said opening engaging and electrically connecting with a contact on one surface of the semiconductor device to provide electrical access thereto from a distal end of that conductive strip, the said conductive strips extending away from the said opening to distal ends at respective locations at or closely within the periphery of the support member, and in which the distance between the centres of the distal ends of any two adjacent ones of the conductive strips is not less than the distance between the centres of those conductive strips at the said one ends thereof.

2. A multilead package as claimed in claim 1, in which the distance between the centres of the distal ends of any two adjacent ones of the conductive strips is greater than the distance between the centres of those conductive strips at the said one ends thereof.

3. A multilead package as claimed in claim 2, wherein the said distal ends of the said conductive strips are wider than the said one ends thereof.

4. A multilead package as claimed in claim 3, wherein the said distal ends are formed as enlarged area lands.

5. A multilead package as claimed in claim 4, and further including electrically conductive pins electrically connected to the said distal ends of the conductive strips and extending perpendicularly to the one surface of the support member.

6. A multilead package as claimed in any preceding claim, wherein the support member has at least one straight edge to which the said conductive strips extend.

7. A multilead package as claimed in claim 3, wherein the said conductive strips extend radially from the opening in the support member.

8. A multilead package as claimed in claim 7, in which the said conductive strips comprise the totality of the conductive strips secured to the support member, and in which the conductive strips terminate at peripheral edges of the support member.

9. A multilead package as claimed in any of claims 1, 2, 3, and 6, and further including a member of thermally conductive material attached to the surface of the support member opposite that to which the said conductive strips are secured and positioned in thermal transfer relation with the semiconductor device.

10. A multilead package as claimed in any of claims 1, 2, 3, and 6, and further including a second support member having an opening formed therein and a second plurality of electrically conductive strips



- secured to one surface of the second support member, the second support member and the second plurality of conductive strips thereon being substantially identical in construction to the first mentioned support member and the conductive strips thereon, and wherein the semiconductor device is positioned partly within the said opening of the first mentioned support member and partly within the said opening of the second support member, the semiconductor device having contacts on opposite surfaces thereof, the contacts on one surface engaging and electrically connecting with the said conductive strips on the first mentioned support member and the contacts on the opposite surface electrically connecting with the said conducting strips on the second support member.
- 11: A multilead package according to any preceding claim wherein the semicon-

ductor device and at least a part of the said support member(s) and the conductive strips thereon are covered by a mass of potting compound.

12. A multilead package as claimed in claim 5, wherein the semiconductor device, the support member and the conductive strips thereon are wholly encapsulated and wherein the electrically conductive pins extend through the encapsulation.

13. A multilead package substantially as herein described with reference to Figures 1 to 3, 4 and 5, 6 and 7, 8 and 9 or 10 to 13 of the drawings.

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