FIG. 1

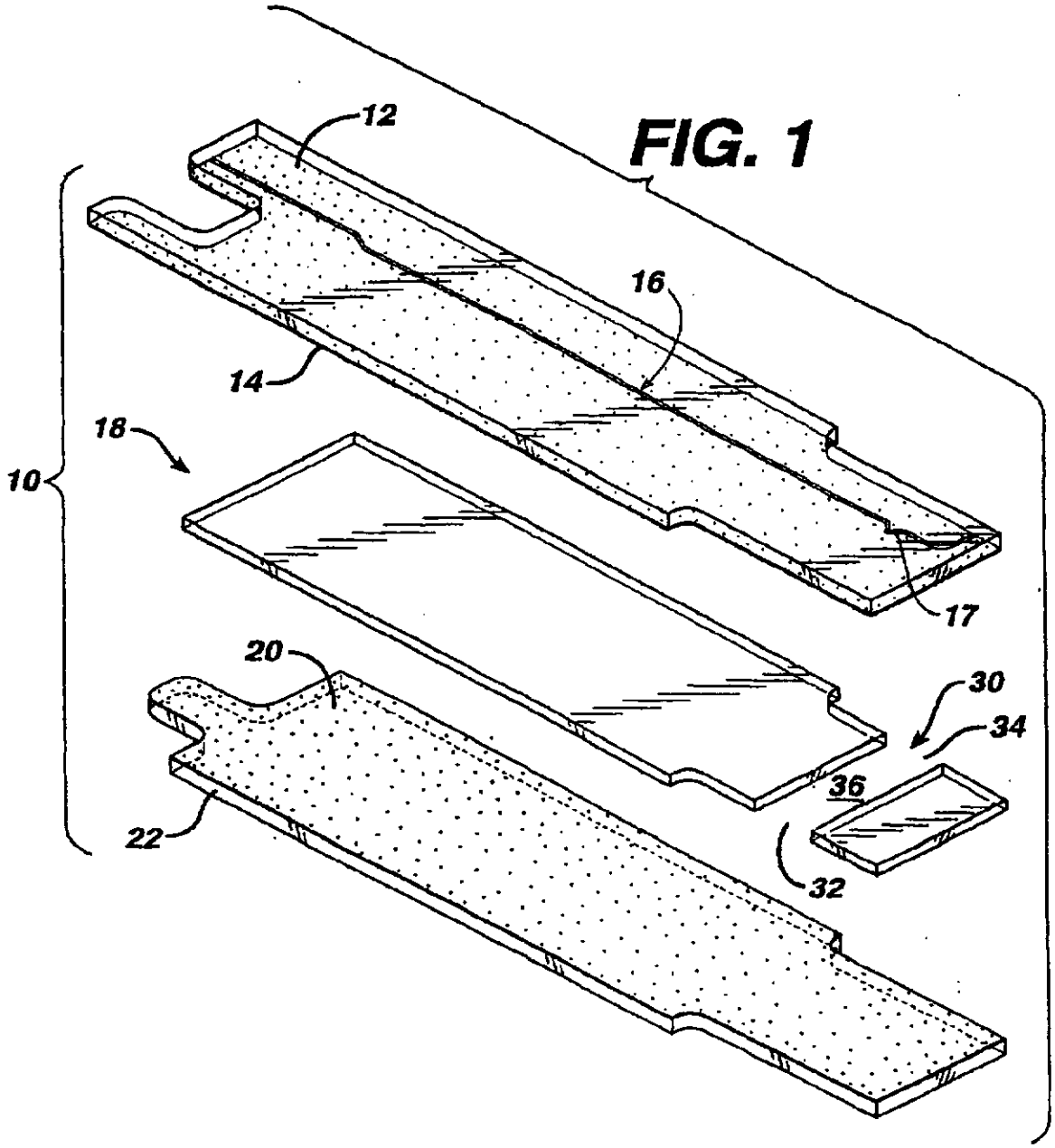


FIG. 2

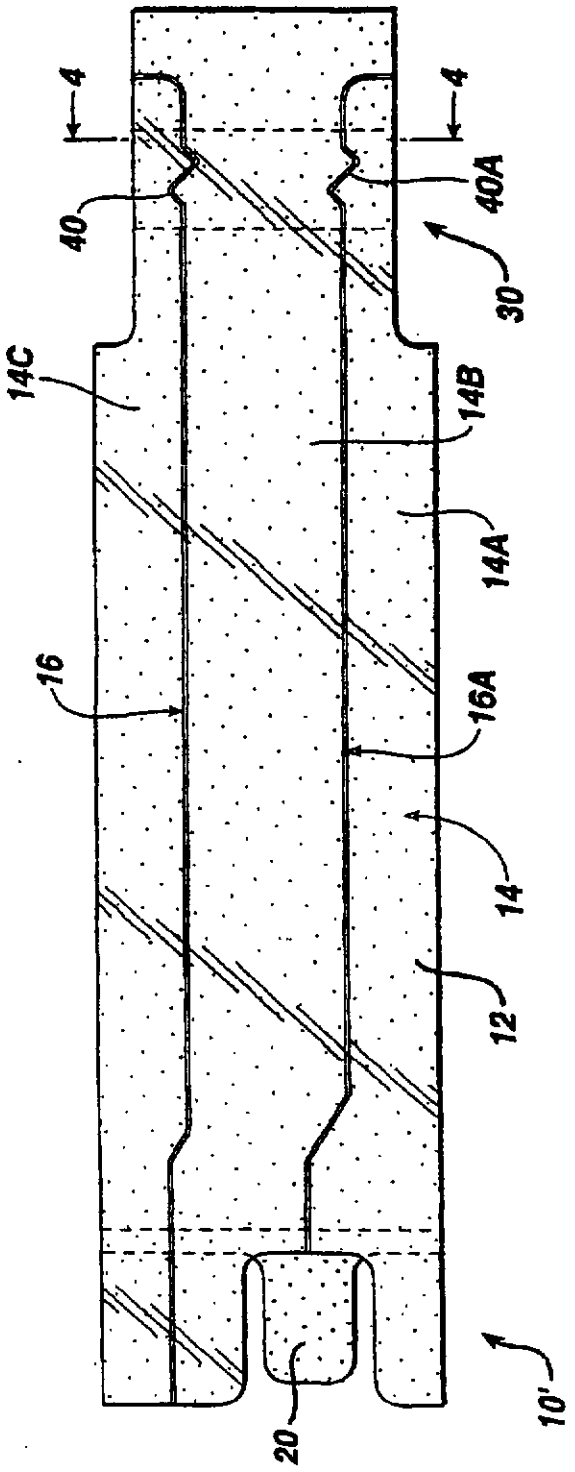


FIG. 3A

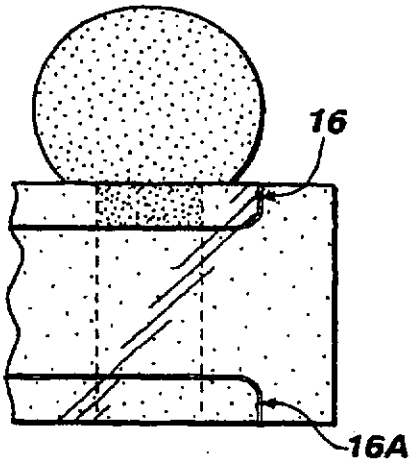


FIG. 3B

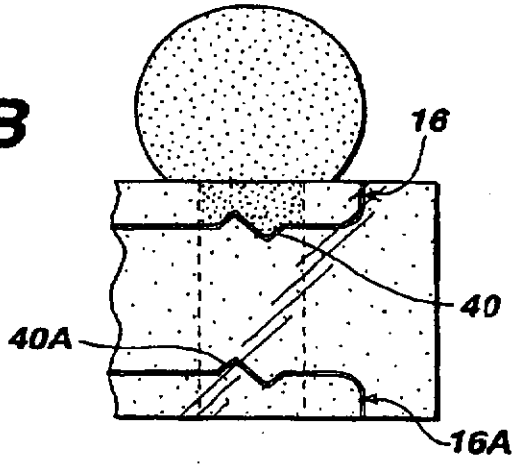


FIG. 3C

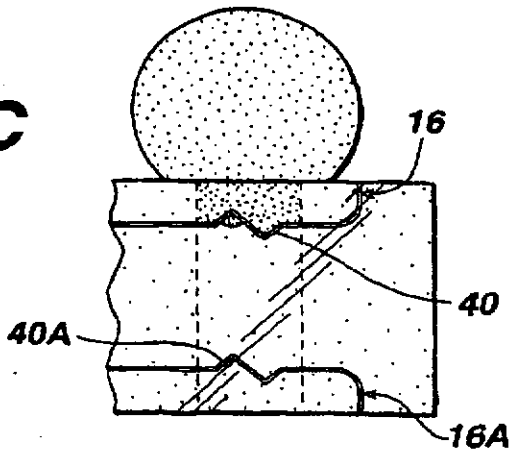


FIG. 4

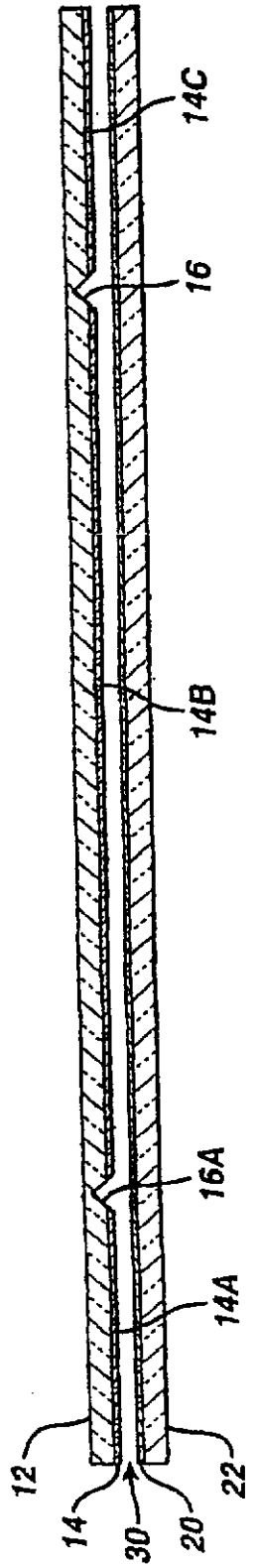


FIG. 5

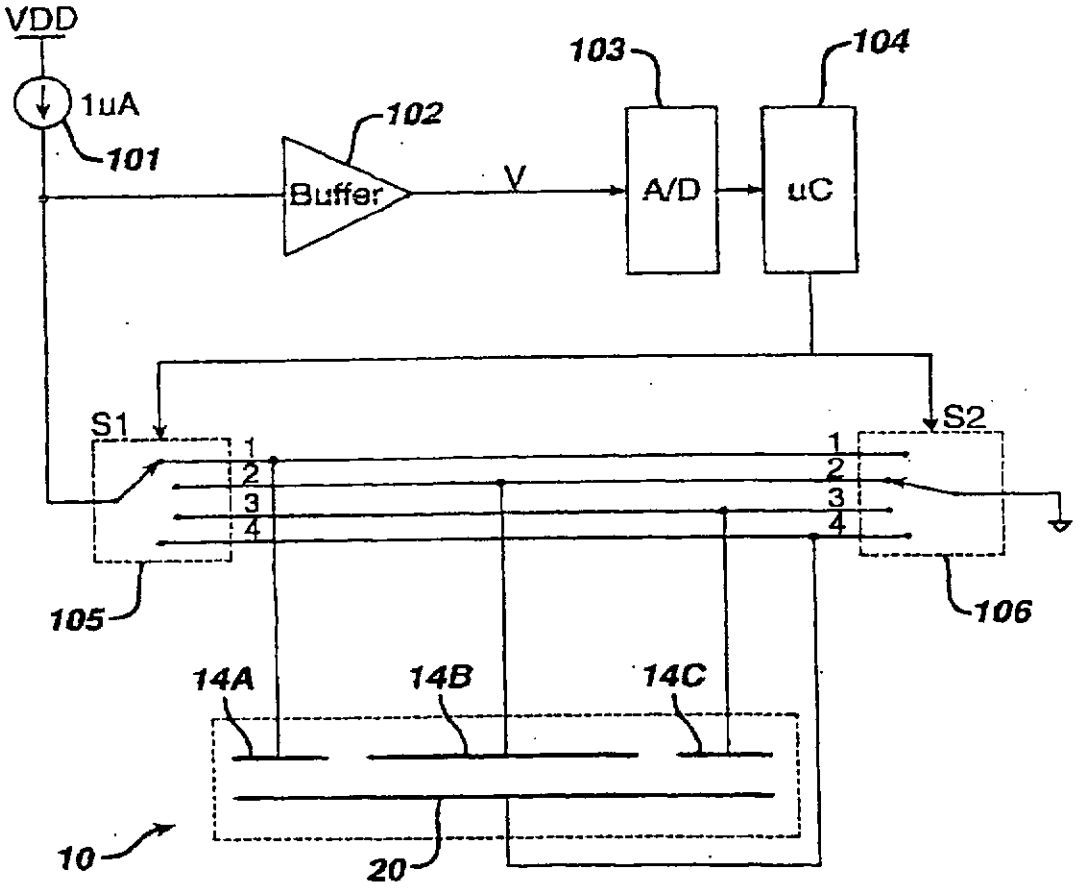

VDD
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102
Buffer
V
103
A/D
104
uC
S1
S2
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2
3
4
105
106
14A
14B
14C
10
20

FIG. 6

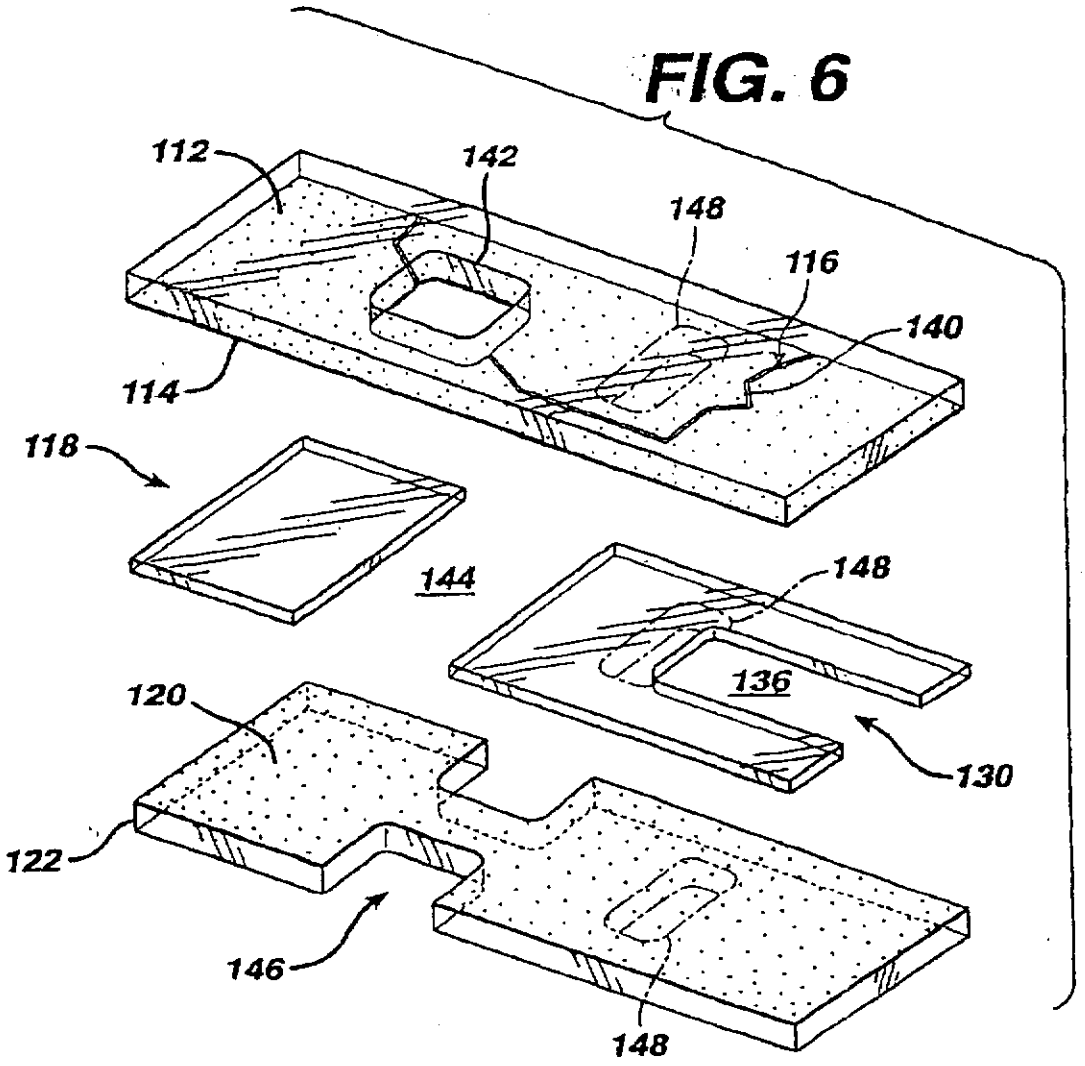


FIG. 7

