

CLAIMS

1. An apparatus comprising:
 - an electrode plane;
 - a memory material disposed through and coupled to the electrode plane;
 - a memory cell included in the memory material aligned in a same plane as the electrode plane, the memory cell configured to exhibit a first threshold voltage representative of a first logic state and a second threshold voltage representative of a second logic state, wherein the memory cell is further configured to act as a selector device and a memory element; and
 - a conductive pillar disposed through and coupled to the memory cell, wherein the conductive pillar and electrode plane are configured to provide a voltage across the memory cell to write a logic state to the memory cell;
 - wherein, responsive to biasing the memory cell between the conductive pillar and the electrode plane by the voltage between a first voltage coupled to the conductive pillar and a second voltage coupled to the electrode plane:
 - the first logic state is written to the memory cell when the first voltage is greater than the second voltage, or
 - the second logic state is written to the memory cell when the first voltage is less than the second voltage.
2. The apparatus of claim 1, further comprising an electrode cylinder disposed between the conductive pillar and the memory material.
3. The apparatus of claim 1, wherein the memory material and conductive pillar are formed as concentric cylinders.
4. The apparatus of claim 1, further comprising a second electrode plane parallel to the electrode plane, the memory material and conductive pillar extending through and coupled to the second electrode plane.
5. The apparatus of claim 4, wherein the memory material comprises a second memory cell associated with the second electrode plane.

6. The apparatus of claim 4, further comprising a dielectric material disposed between the electrode plane and the second electrode plane.

7. The apparatus of claim 1, further comprising a plurality of conductive pillars and corresponding memory material disposed through the electrode plane, wherein the plurality of conductive pillars and corresponding memory material form an array.

8. The apparatus of claim 1, wherein the electrode plane is coupled to a first memory access line and the conductive pillar is coupled to a second memory access line.

9. The apparatus of claim 1, wherein the conductive pillar and electrode plane are further configured to provide a second voltage across the memory cell to read the first logic state and the second logic state.

10. An apparatus, comprising:

a memory column including a ring-shaped memory cell, a conductive pillar, and an electrode material disposed between the ring-shaped memory cell and the conductive pillar, wherein the ring-shaped memory cell is configured to act as a selector device and a memory element;

a stack of alternating plurality of electrode planes and plurality of dielectric material, wherein the ring-shaped memory cell is aligned in an electrode plane of the plurality of electrode planes; and

an opening through the stack, wherein the memory column is disposed in the opening;

wherein, responsive to biasing the ring-shaped memory cell between the conductive pillar and the electrode plane by a voltage between a first voltage coupled to the conductive pillar and a second voltage coupled to the electrode plane:

a first logic state is written to the ring-shaped memory cell when the first voltage is greater than the second voltage, or

a second logic state is written to the ring-shaped memory cell when the first voltage is less than the second voltage.

11. The apparatus of claim 10 wherein the ring-shaped memory cell is included in a memory material extending a length of the memory column.
12. The apparatus of claim 10, wherein the plurality of electrode planes comprises a plurality of thin films.
13. The apparatus of claim 10, wherein the plurality of dielectric material comprises an oxide.
14. The apparatus of claim 11, wherein the memory material comprises a chalcogenide.
15. The apparatus of claim 10, wherein the electrode material comprises a barrier material.
16. An apparatus, comprising:
 - an electrode plane; and
 - a plurality of ring-shaped memory cells aligned in the electrode plane as a two-dimensional array, wherein the plurality of ring-shaped memory cells are configured to act as selector devices and memory elements;
 - wherein, responsive to biasing a respective ring-shaped memory cell in the plurality of ring-shaped memory cells between a corresponding conductive pillar and the electrode plane by coupling a first voltage to the corresponding conductive pillar and coupling a second voltage to the electrode plane:
 - a first logic state is written to the respective ring-shaped memory cell when the first voltage is greater than the second voltage, or
 - a second logic state is written to the respective ring-shaped memory cell when the first voltage is less than the second voltage.
17. The apparatus of claim 16, further comprising a plurality of conductive pillars within the plurality of ring-shaped memory cells.

18. The apparatus of claim 16, further comprising a plurality of ring-shaped electrode cylinders within the plurality of ring-shaped memory cells.

19. The apparatus of claim 16, further comprising:
a second electrode plane; and
a second plurality of ring-shaped memory cells aligned in the second electrode plane.

20. The apparatus of claim 19, wherein the second plurality of ring-shaped memory cells are vertically aligned with the plurality of ring-shaped memory cells.

21. The apparatus of claim 16, wherein the plurality of memory cells are configured to exhibit a first threshold voltage representative of a first logic state responsive to programming with a voltage having a first polarity and a second threshold voltage representative of a second logic state responsive to programming with a voltage having a second polarity.

22. An apparatus comprising:
an electrode plane;
an array of conductive pillars disposed through the electrode plane; and
an array of memory cells formed as concentric rings around the conductive pillars of the array of conductive pillars, wherein the array of memory cells are aligned in a same plane as the electrode plane, wherein the array of memory cells are configured to act as selector devices and memory elements;

wherein, responsive to biasing a respective memory cell in the array of memory cells between a corresponding conductive pillar and the electrode plane by a voltage between a first voltage coupled to the corresponding conductive pillar and a second voltage coupled to the electrode plane:

a first logic state is written to the respective memory cell when the first voltage is greater than the second voltage, or

a second logic state is written to the respective ring-shaped memory cell when the first voltage is less than the second voltage.

23. The apparatus of claim 22, wherein the memory cells of the array of memory cells are configured to act as two-terminal threshold switching devices.

24. The apparatus of claim 22, wherein the electrode plane, the array of conductive pillars, and the array of memory cells are included in a three-dimensional memory array.

25. The apparatus of claim 22, wherein the memory cells of the array of memory cells include a chalcogenide.

26. The apparatus of claim 22, wherein the memory cells of the array of memory cells have a thickness equal to a thickness of the electrode plane.

27. A method comprising:

receiving a first address corresponding to a conductive pillar in an array of conductive pillars;

receiving a second address corresponding to an electrode plane in a stack of electrode planes;

coupling the conductive pillar to a first voltage;

coupling the electrode plane to a second voltage; and

biasing a memory cell coupled between the conductive pillar and the electrode plane by a difference between the first voltage and the second voltage, wherein the memory cell is configured to act as a selector device and a memory element;

wherein the first voltage is greater than the second voltage and responsive to the biasing, a first logic state is written to the memory cell, or wherein the first voltage is less than the second voltage and responsive to the biasing, a second logic state is written to the memory cell.

28. The method of claim 27, further comprising coupling conductive pillars in the array of conductive pillars that do not correspond to the first address to a common voltage; and

coupling electrode planes in the stack of electrode planes that do not correspond to the second address to the common voltage.

29. The method of claim 27, wherein the memory cell exhibits a first threshold voltage when the difference between the first voltage and the second voltage is in a same polarity as a read voltage, and wherein the memory cell exhibits a second threshold voltage when the difference between the first voltage and the second voltage is in an opposite polarity as the read voltage.

30. The method of claim 27, wherein the first logic state corresponds to a first threshold voltage of the memory cell, and wherein the second logic state corresponds to a second threshold voltage of the memory cell.

31. The method of claim 30, further comprising:
coupling the conductive pillar to a third voltage;
coupling the electrode plane to a fourth voltage;
biasing the memory cell coupled between the conductive pillar and the electrode plane by a difference between the third voltage and the fourth voltage, wherein the third voltage is greater than the fourth voltage; and
responsive to the biasing, determining a logic state of the memory cell.

32. The method of claim 27, wherein the first address is received at a row address decoder and a column address decoder and the second address is received at an electrode plane address decoder.

33. A method comprising:
forming a stack of alternating electrode planes and dielectric layers;
forming an opening in the stack;
forming a conformal layer of memory material in the opening; and
filling the opening with a conductive pillar over the conformal layer to form a respective memory cell corresponding to an electrode plane in the stack of alternating electrode planes;
wherein, responsive to biasing the respective memory cell between the conductive pillar and the corresponding electrode plane by a voltage between a first voltage coupled to the conductive pillar and a second voltage coupled to the corresponding electrode plane:

a first logic state is written to the respective memory cell when the first voltage is greater than the second voltage, or

a second logic state is written to the respective memory cell when the first voltage is less than the second voltage.

34. The method of claim 33, further comprising forming a conformal layer of barrier material over the memory material prior to filling the opening with the conductive pillar.

35. The method of claim 33, wherein forming the opening comprises applying a mask and etching the opening in the stack.

36. The method of claim 33 further comprising:
coupling the electrode planes to a first plurality of corresponding memory access lines; and
coupling the conductive pillar to a second memory access line.

37. The method of claim 33, wherein forming the conformal layer of memory material in the opening comprises recessing the electrode planes and selectively forming memory material in recesses formed in the electrode planes.