What is claimed is:

1. A semiconductor memory device comprising:

a memory cell array including a normal cell region and a redundancy cell region, the normal cell region including a plurality of normal region groups, and redundancy cell region configured to replace failed memory cells of the normal cell region; and

a repair control circuit configured to,

determine a target normal region group from among the plurality of normal region groups based on an input address,

extract target fail addresses from among a plurality of fail addresses based on the target normal region group, and

control a repair operation based on the target fail addresses and the input address;

wherein each of the plurality of normal region groups includes a plurality of sub regions such that ones of the plurality of sub regions adjacent to each other are in different ones of the plurality of normal region groups, and

wherein, in each of the plurality of normal region groups, the plurality of sub regions, are arranged sequentially in a column direction according to a round-robin scheme.

2. The semiconductor memory device claim 1, wherein a number of bit of each of the plurality of the fail addresses is smaller than a number of bits of the input address.

3. The semiconductor memory device of claim 1 or claim 2, wherein

the plurality of normal region groups includes 2^M normal region groups,

a number of bits of the input address is N input bits, and

a number of bits of each of the plurality of fail addresses is N-M, N being a natural number, and M being a natural number smaller than N.

4. The semiconductor memory device of any one of claims 1 to 3, wherein the input address includes one or more group identity bits representing the target normal region group.

5. The semiconductor memory device of claim 4, wherein the repair control circuit includes:

a group selection circuit configured to generate a plurality of group selection signals based on the group identity bits, the plurality of group selection signals representing the target normal region group;

an address storage circuit configured to store the plurality of fail addresses, and to extract the target fail addresses from among the plurality of fail addresses based on the plurality of group selection signals; and

a comparison circuit configured to generate a repair control signal based on the input address and the target fail addresses.

6. The semiconductor memory device of claim 5, wherein the comparison circuit is shared by the plurality of normal region groups.

7. The semiconductor memory device of claim 5 or claim 6, wherein

the comparison circuit includes a plurality of comparators configured to compare the target fail addresses with the input address, and

wherein a number of the plurality of comparators is less than a number of the fail addresses storable in the address storage circuit.

8. The semiconductor memory device of claim 7, wherein,

the number of the plurality of comparators is P and a number of the plurality of normal region groups is Q, and

the number of the fail addresses storable in the address storage circuit is P*Q, P and Q being natural numbers.

9. The semiconductor memory device of claim 7 or claim 8, wherein

the input address includes the one or more group identity bits and other bits,

each of the plurality of comparators includes a plurality of logic gates configured to perform a bitwise comparison of bits of ones of the target fail addresses with the other bits of the input address, and

the plurality of normal region groups includes 2^M normal region groups, a number of bits of the input address is N input bits, and a number of the plurality of logic gates in each comparator is N-M, N being a natural number and M being a natural number smaller than N.

10. The semiconductor memory device of any one of claims 1 to 9, wherein the input address includes one or more group identity bits and one or more sub region identity bits, the one or more group identity bits representing the target normal region group and the one or more sub region identity bits representing a target sub region among the plurality of sub regions.

11. The semiconductor memory device of claim 10, wherein the group identity bits in the input address are less significant bits than the sub region identity bits in the input address.

12. The semiconductor memory device of any one of claims 1 to 11, wherein the semiconductor memory device is configured to perform a row repair operation to repair the failed memory cells by unit of a row, such that each of the plurality of sub regions corresponds to a plurality of word lines.

13. The semiconductor memory device of any one of claims 1 to 12, wherein the semiconductor memory device is configured to perform a column repair operation to repair the failed memory cells by unit of a column in each of a plurality of memory blocks such that the plurality of sub regions corresponds to the plurality of memory blocks, and word lines of the redundancy cell region are different from word lines of the normal cell region.

14. The semiconductor memory device of any one of claims 1 to 13, wherein the redundancy cell region includes a plurality of redundancy region groups, the plurality of the redundancy region groups configured replace the failed memory cells in corresponding normal region groups among the plurality of normal region groups.

15. The semiconductor memory device of any one of claims 1 to 14, wherein the redundancy cell region is shared by the plurality of normal region groups such that the redundancy cell region is configured to replace the failed memory cells in the plurality of normal region groups.

16. A semiconductor memory device comprising:

a normal cell region including a plurality of normal region groups, each of the normal region groups including a plurality of sub regions, the plurality of sub regions included in respective ones of the normal region groups arranged one by one sequentially in a column direction according to a round-robin scheme;

a redundancy cell region configured to replace failed memory cells of the normal cell region; and

a repair control circuit configured to,

determine a target normal region group from among the plurality of normal region groups based on an input address,

extract target fail addresses from among a plurality of fail addresses based on the target normal region group, and

control a repair operation based on the target fail addresses and the input address.

17. A method of operating a semiconductor memory device, the semiconductor memory device including a normal cell region and a redundancy cell region, the normal cell region divided into a plurality of normal region groups, and the redundancy cell region configured to replace failed memory cells of the normal cell region, the method comprising:

determining a target normal region group from among the plurality of normal region groups based on an input address;

extracting target fail addresses from among a plurality of fail addresses based on the target normal region group;

controlling a repair operation based on the target fail addresses and the input address;

dividing each of the plurality of normal region groups into a plurality of sub regions; and

arranging the sub regions included in the respective normal region groups one by one sequentially in a column direction according to a round-robin scheme.