

FIG. 1

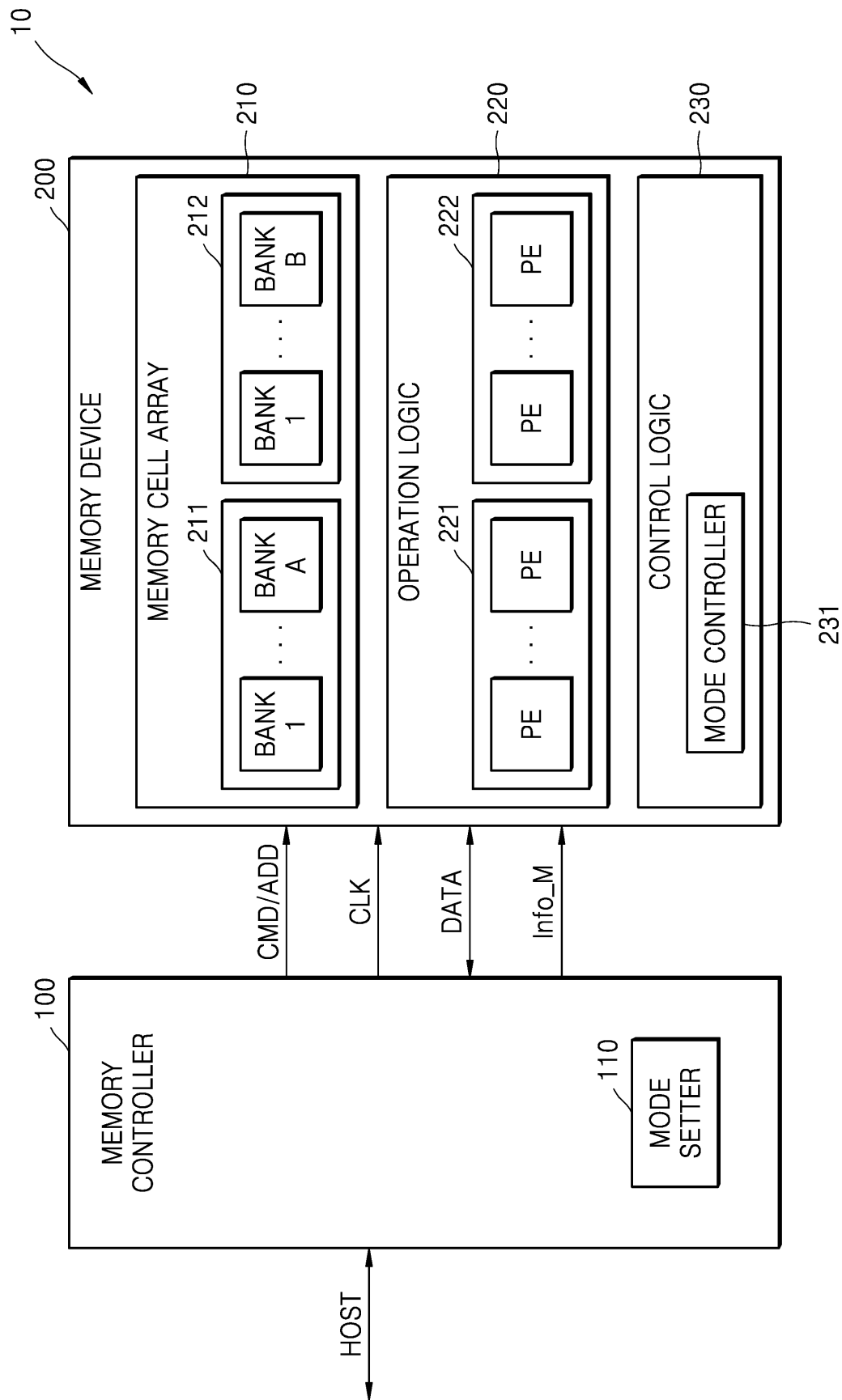


FIG. 2

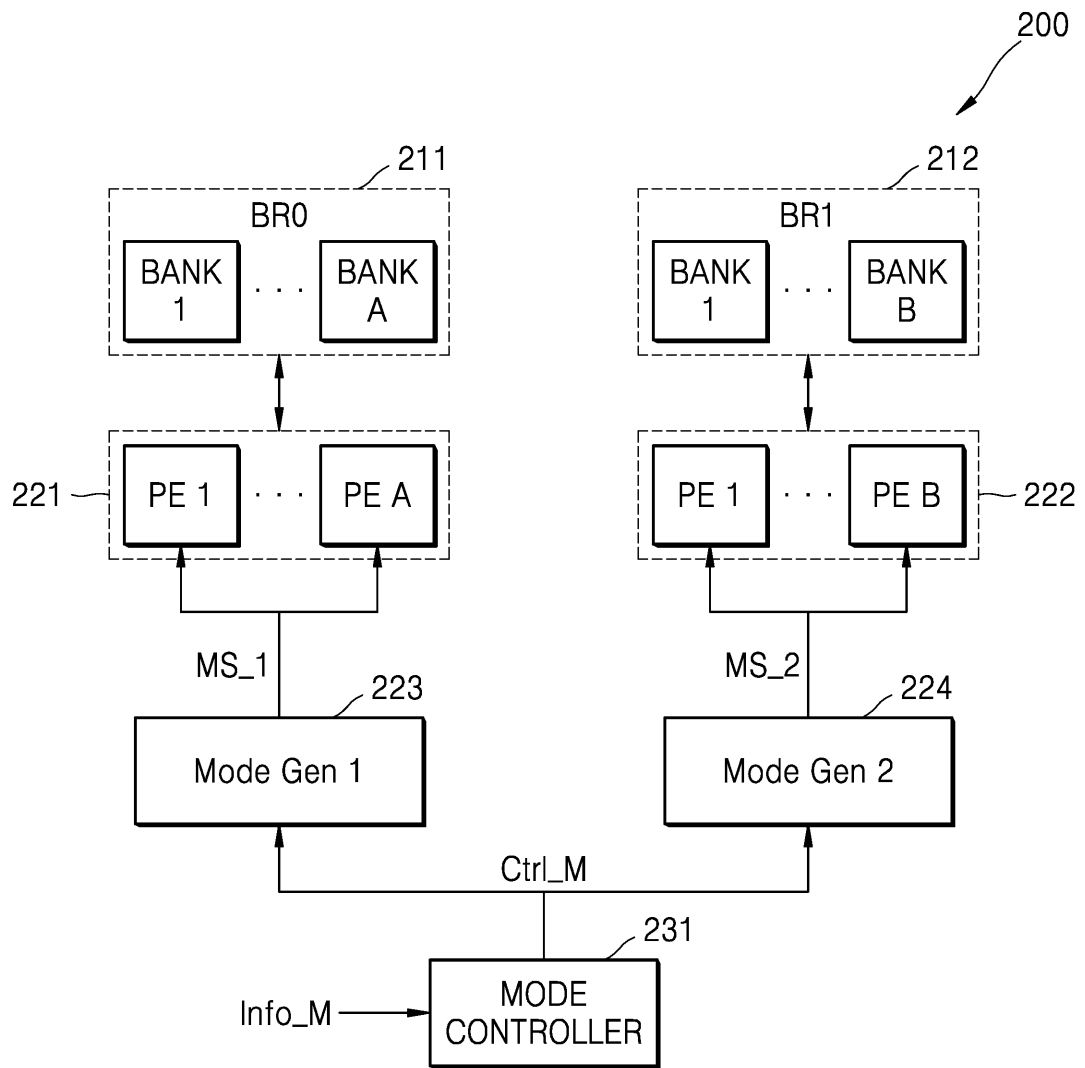


FIG. 3

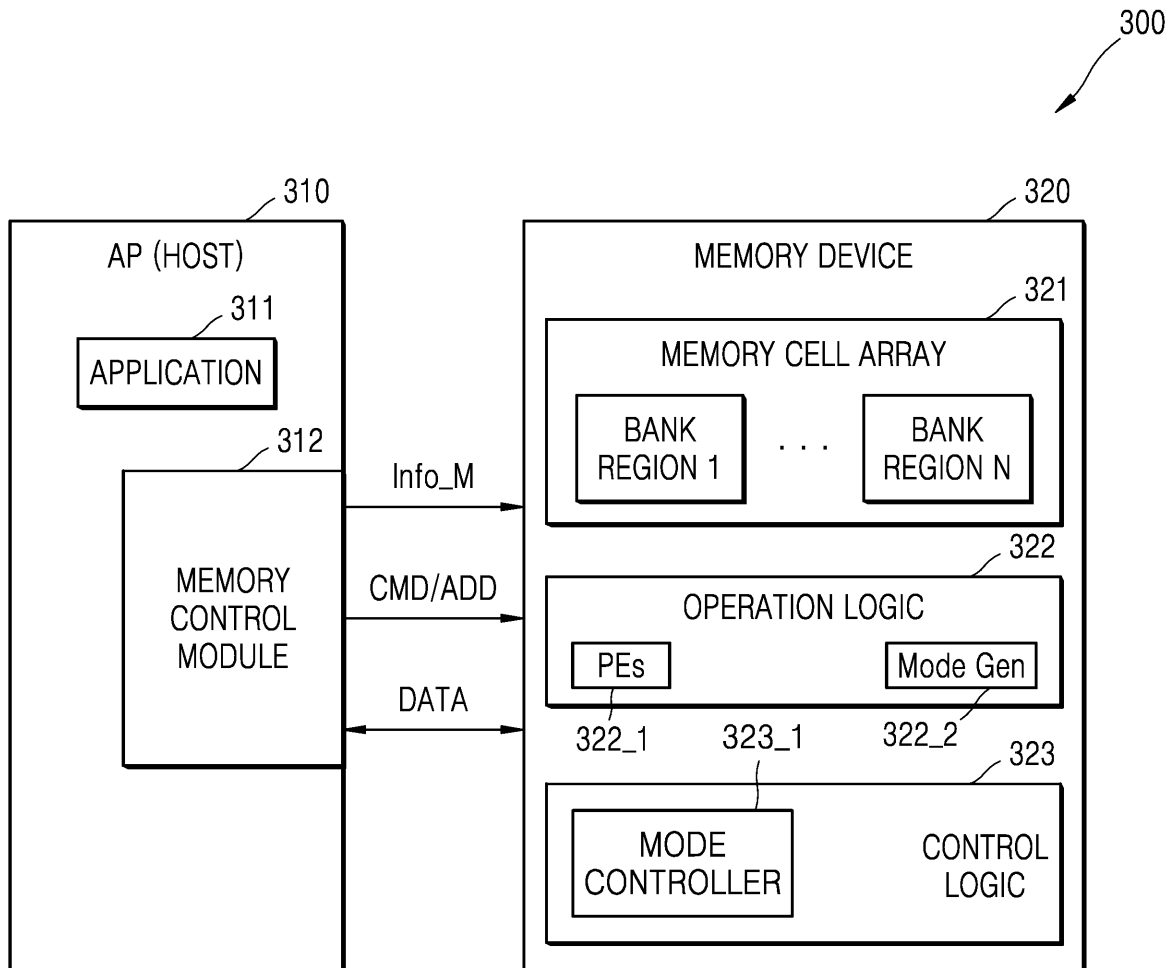


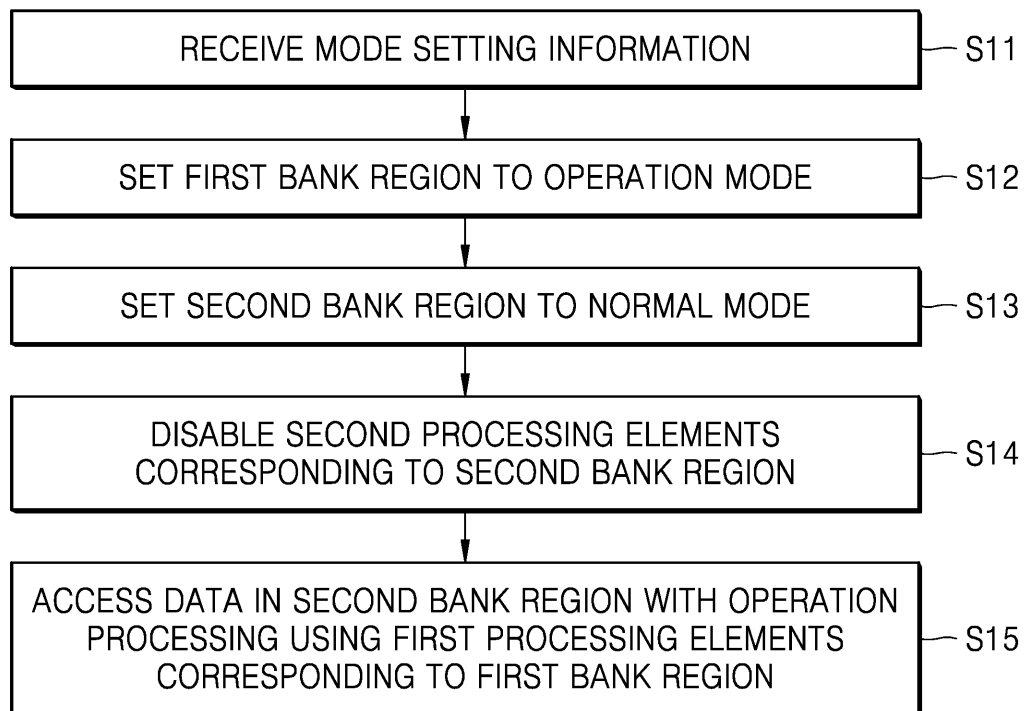
FIG. 4

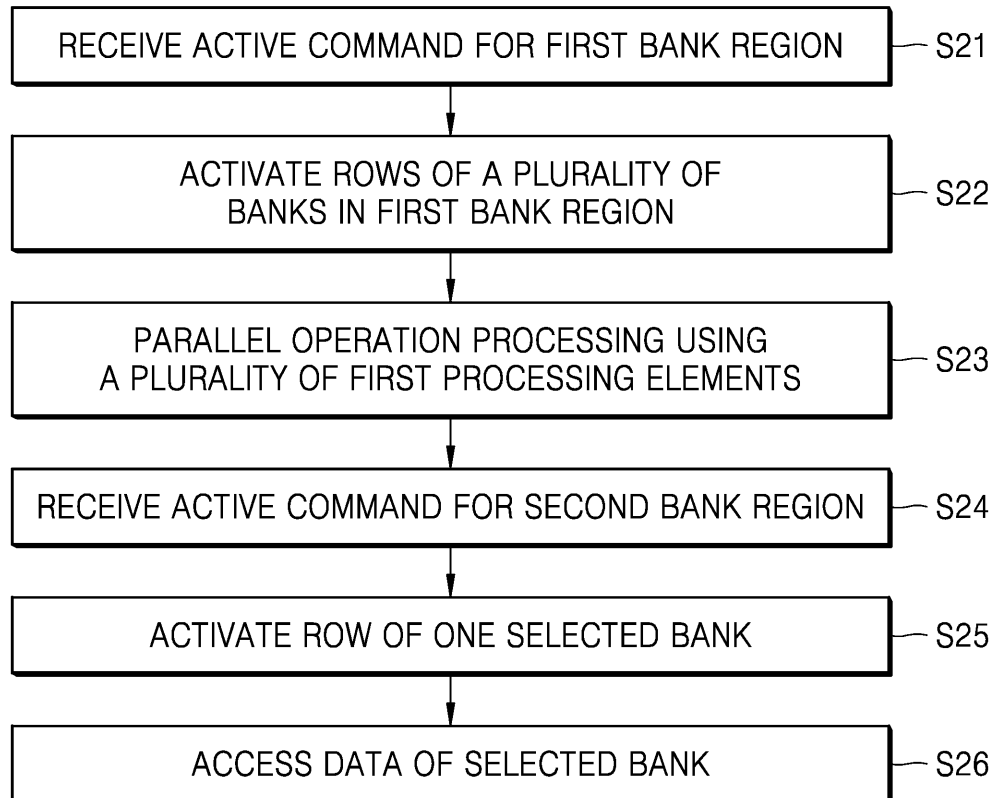
FIG. 5

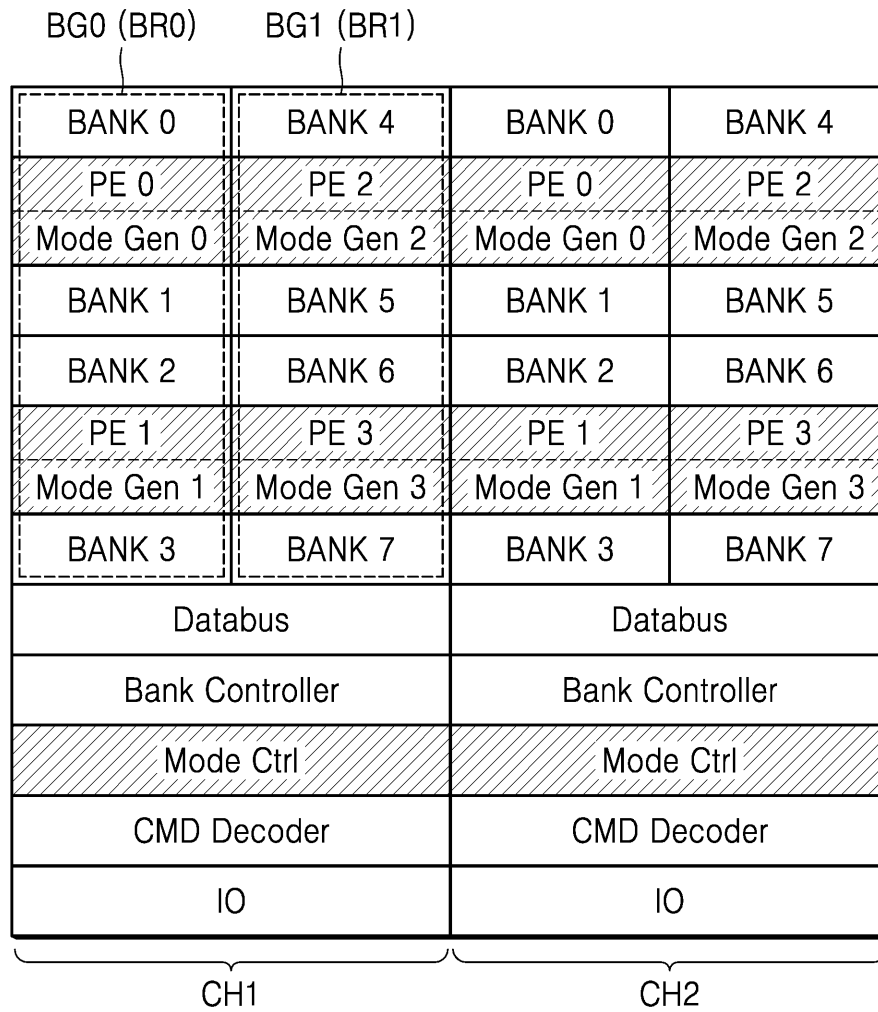
FIG. 6

FIG. 7

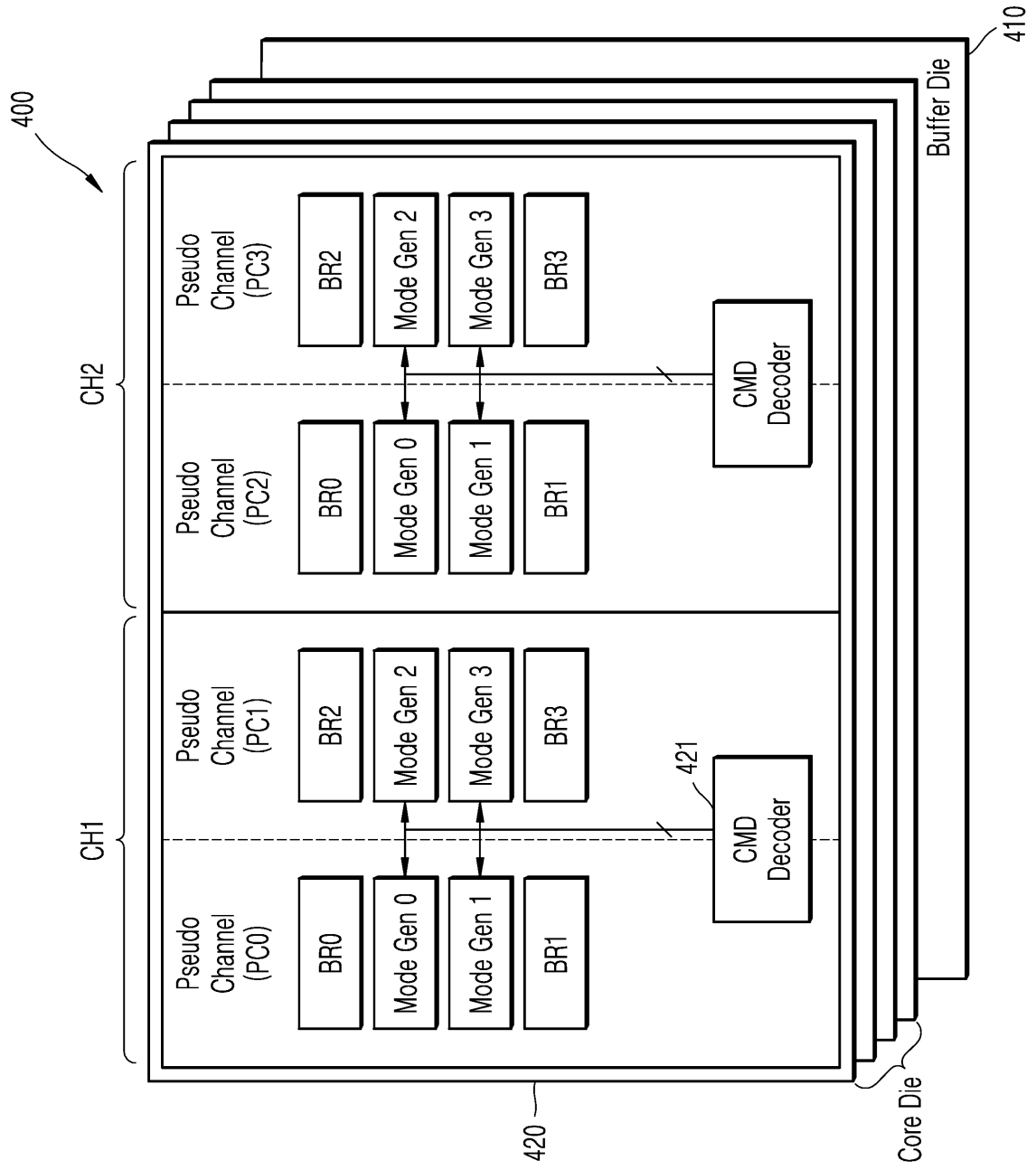


FIG. 8

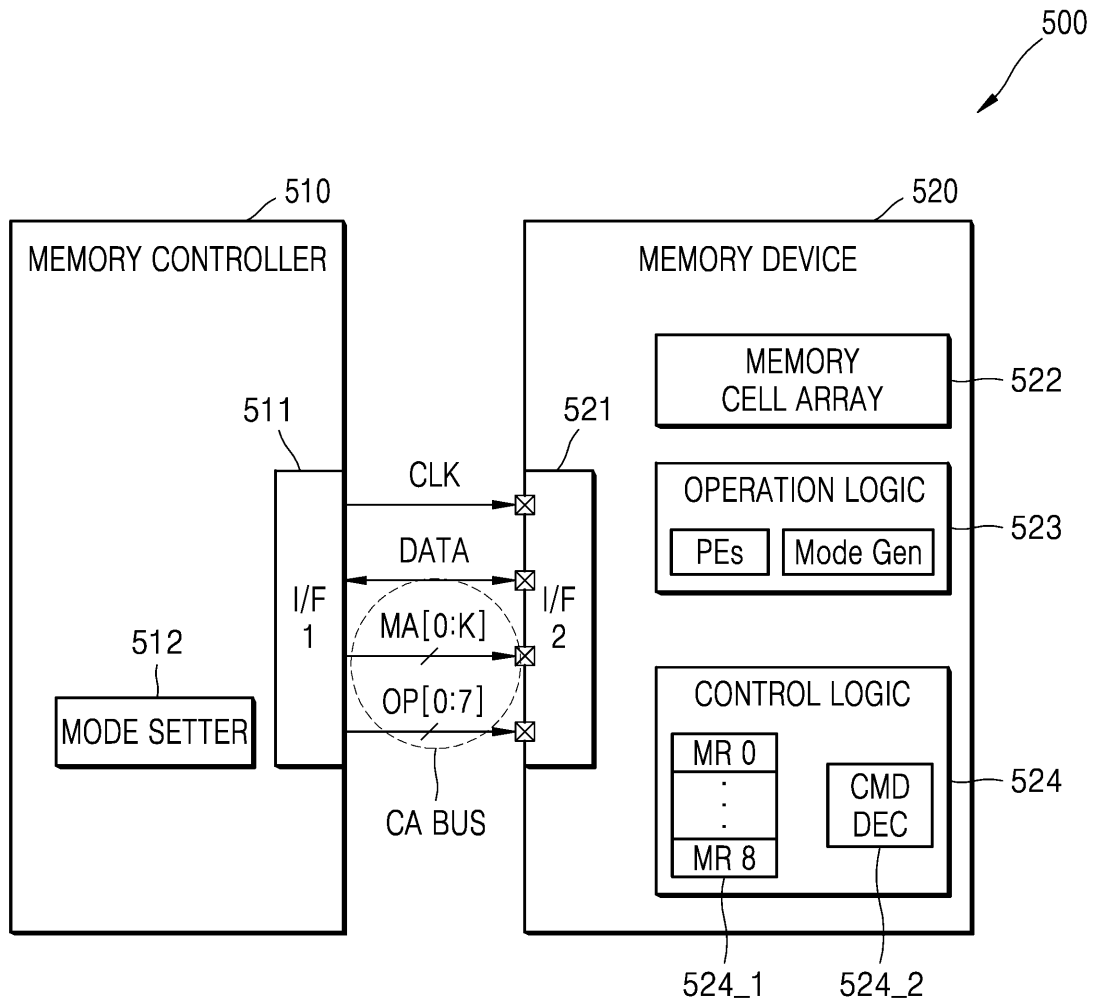


FIG. 9

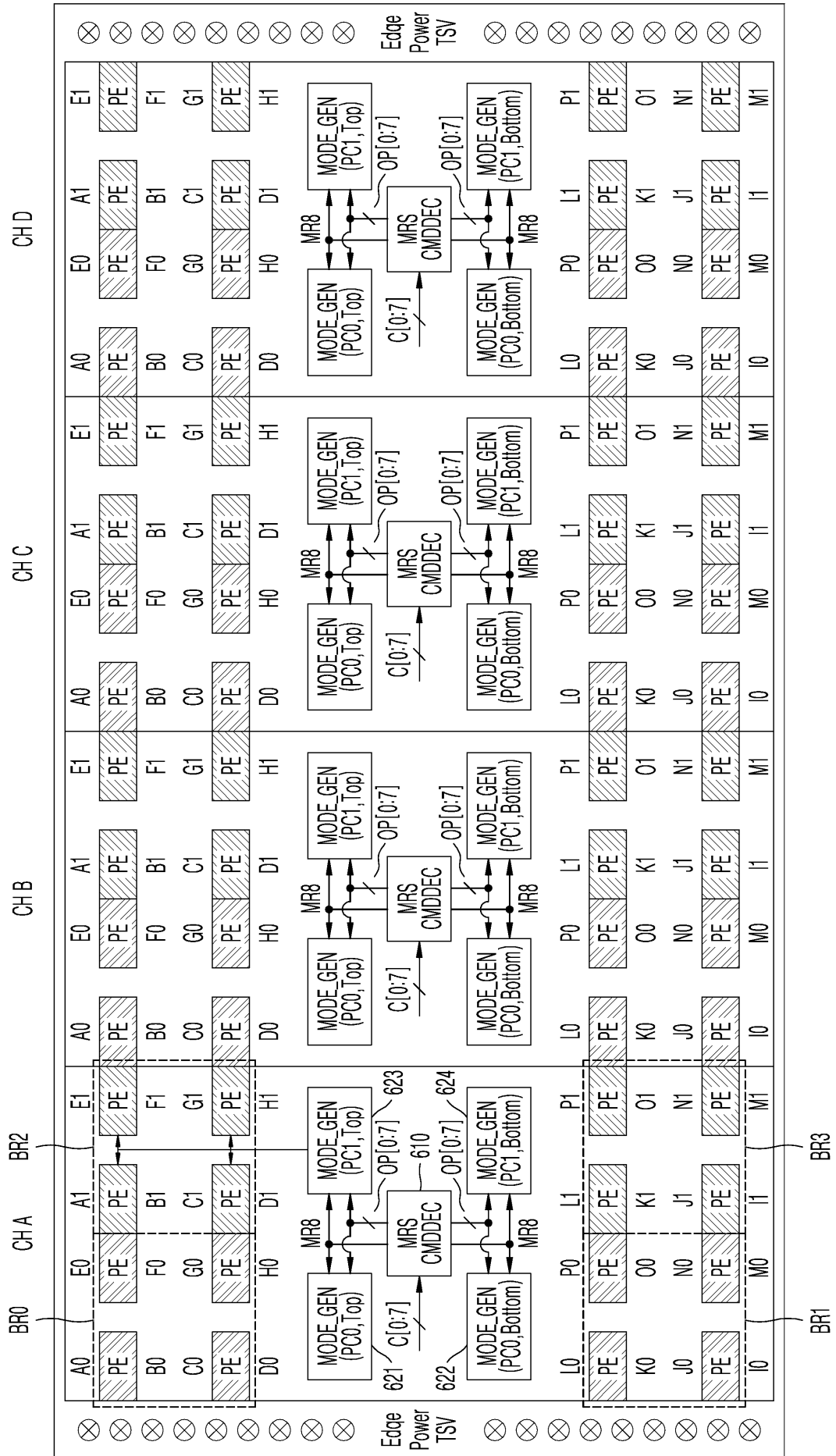


FIG. 10

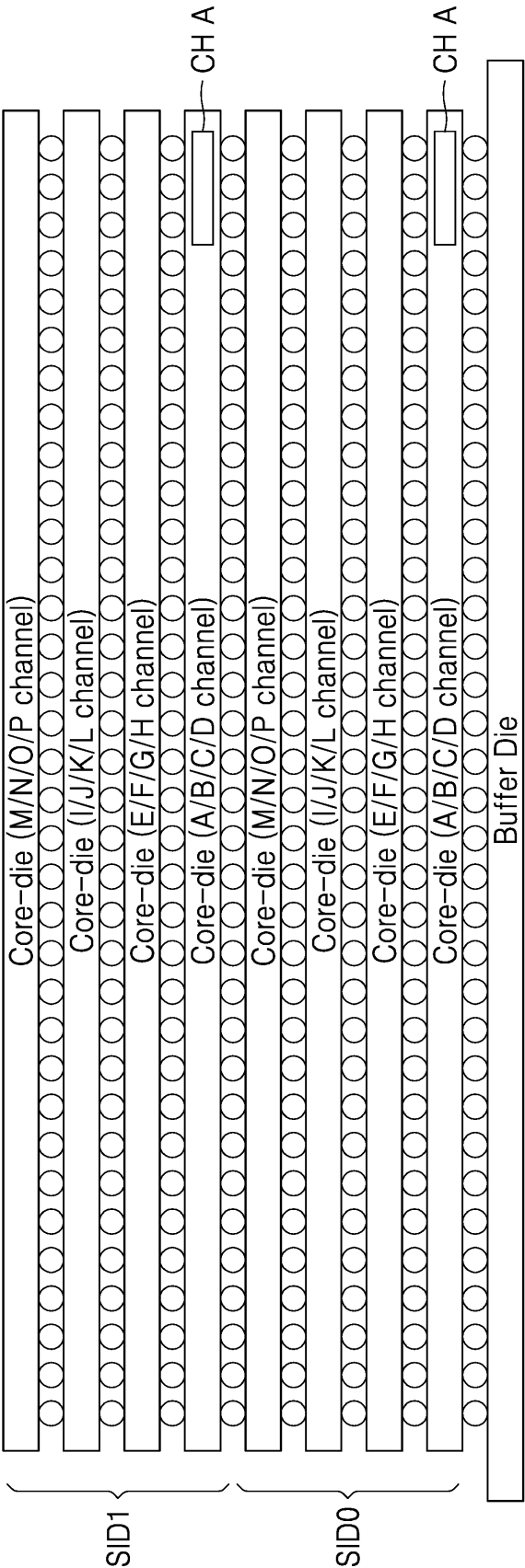


FIG. 11

	MA[0:4]	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
MR8	01000	BA3"H"	BA3"L"	PC1	PC0	SID1	SID0	Mode exit	Mode entry
(1) Default (normal mode)		0	0	0	0	0	0	0	0
(2) ALL BANKS OF SID0 AND PC0 ENTER PIM MODE		1	1	0	1	0	1	0	1
(3) ALL BANKS OF SID0 & SID1 AND PC0 ENTER PIM MODE		1	1	0	1	1	1	0	1
(4) ONLY BOTTOM REGION OF SID0, PC0 ENTER PIM MODE		1	0	0	1	0	1	0	1
(5) ONLY BOTTOM REGION OF SID0, PC0 & PC1 ENTER PIM MODE		1	0	1	1	0	1	0	1
(6) ALL BANKS OF SID0 AND PC0 EXIT FROM PIM MODE		1	1	0	1	0	1	1	0

FIG. 12

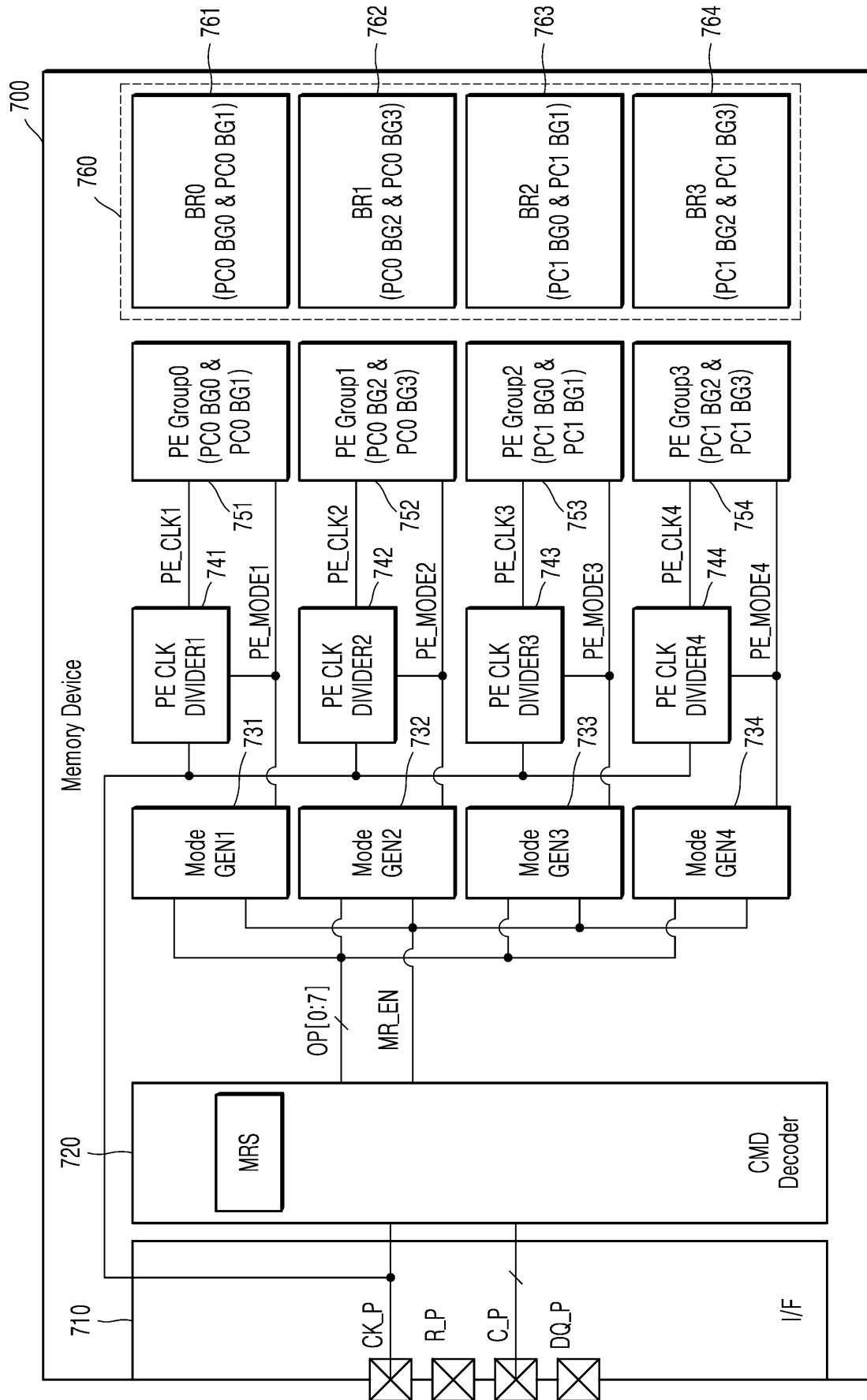


FIG. 13

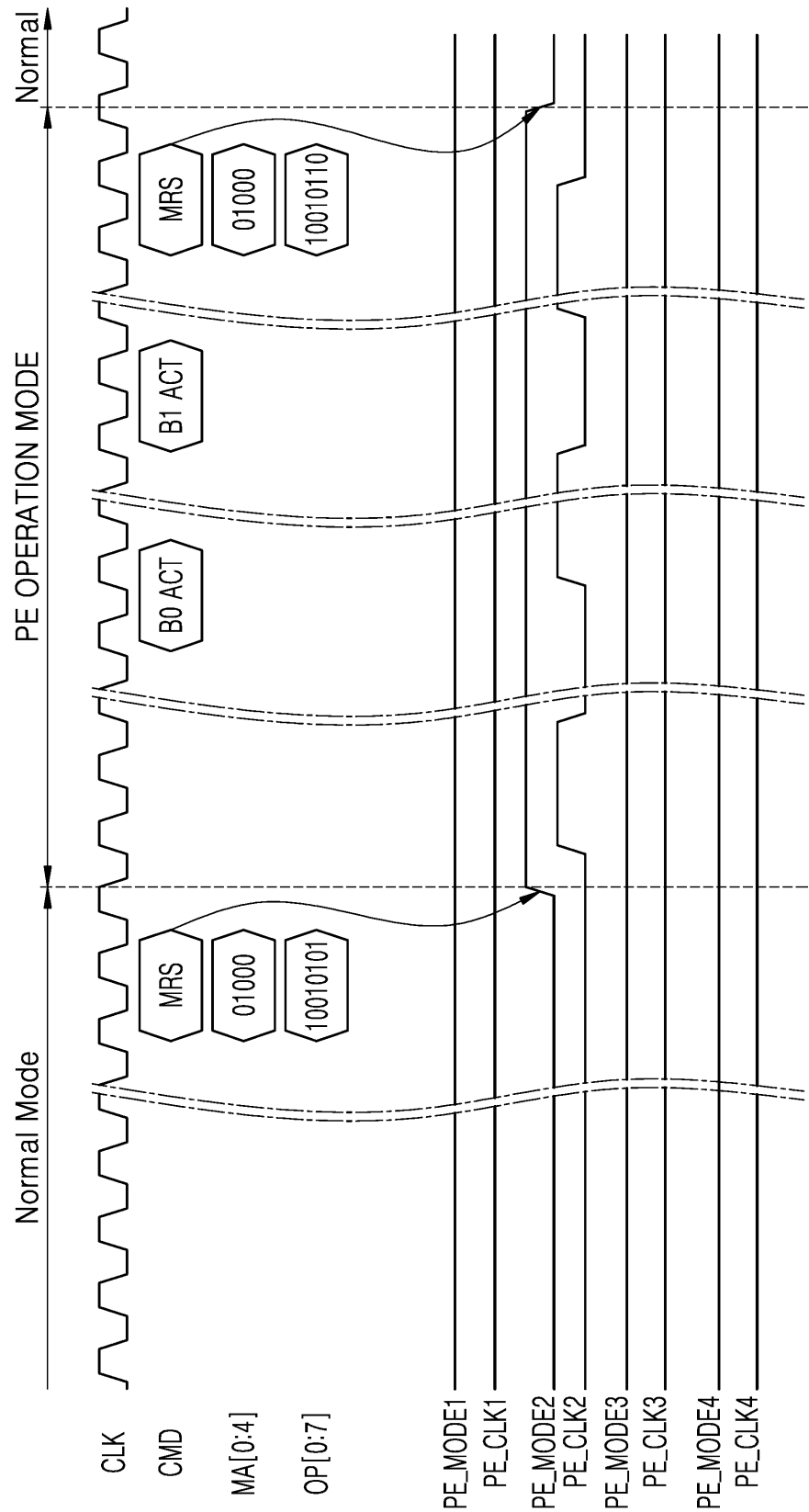


FIG. 14

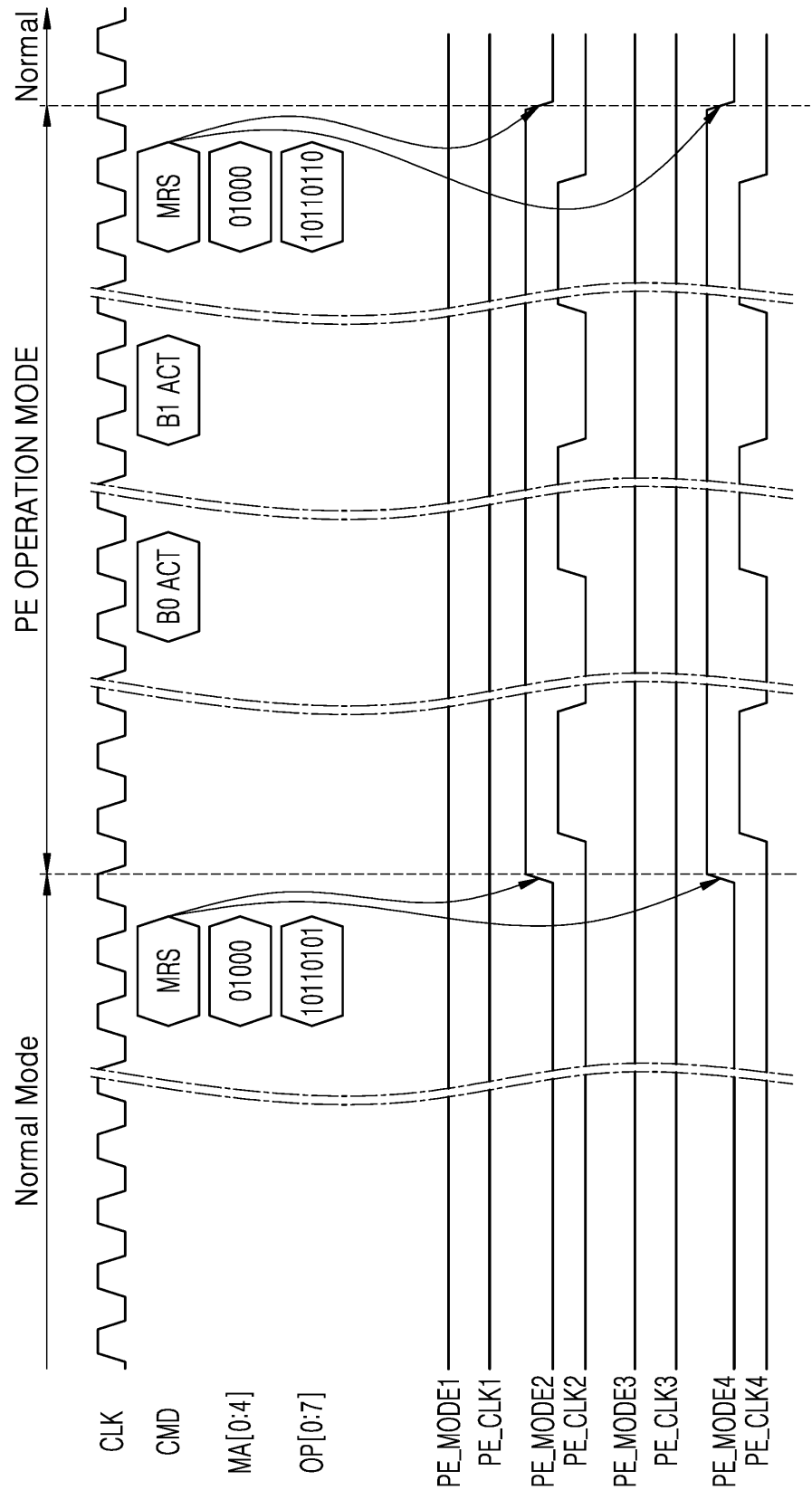


FIG. 15

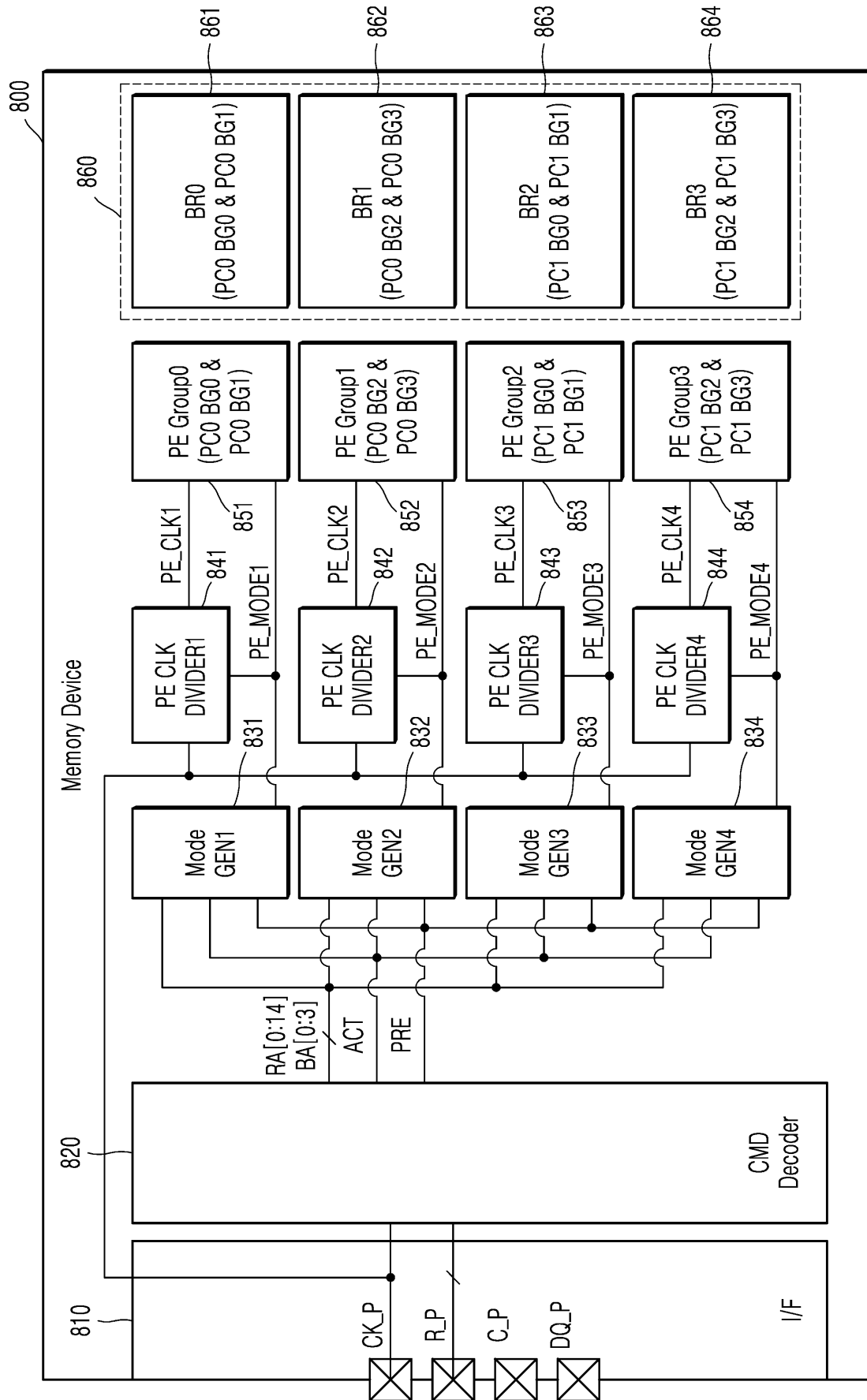


FIG. 16

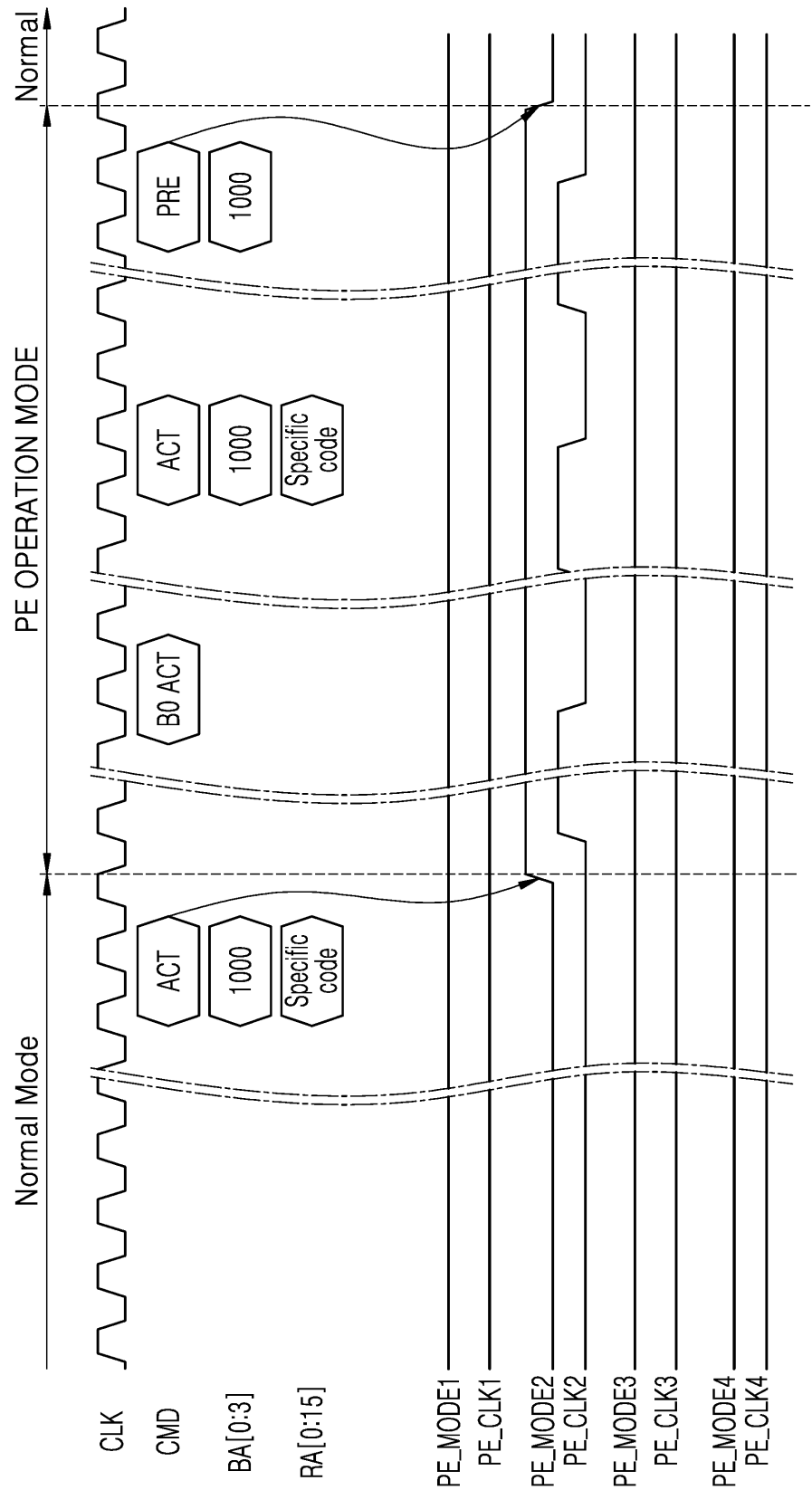


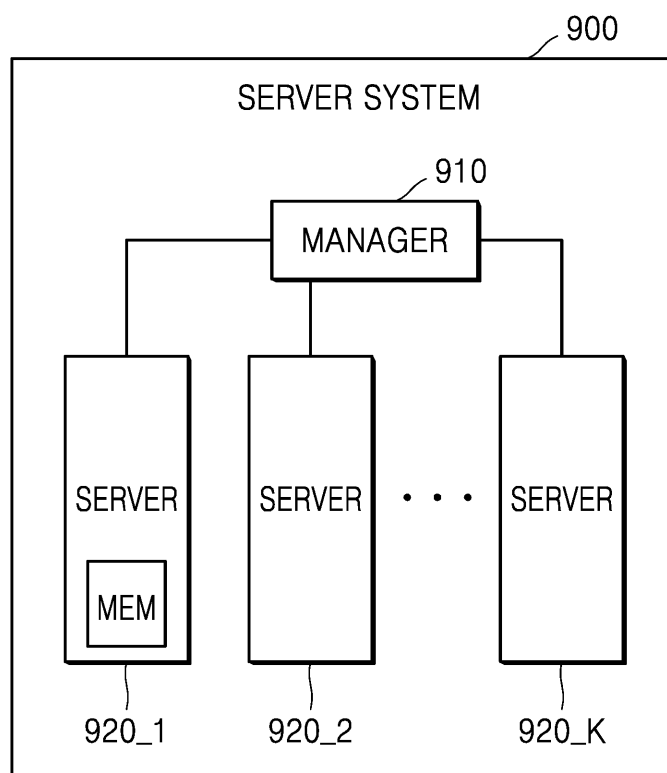
FIG. 17

FIG. 18

