

SPECIFICATION

A directional coupler

5 This invention relates to a directional coupler for duplex transmission, the coupler including a device for providing a correction signal and a compensation circuit to which the correction signal is applied for suppression of that part of the received signal which is caused by its own transmitted signal.

10 The known technique is illustrated in Figures 1-4 of the accompanying drawings.

A general block diagram as shown in Figure 1 illustrates duplex transmission on a single transmission channel, S, denoting transmitter, M denoting receiver and DK denoting directional coupler (traditionally a hybrid transformer). The connection between the two directional couplers is a simple transmission channel, e.g. a two-wire line.

20 With an ideal coupler one would obtain an equivalent diagram as shown in Figure 2, where H_1 and H_2 are the transfer functions of the line in the two directions.

However, in practice a portion of the signal from S, will in addition be partly transferred through the coupler and be partly reflected via the line to M, with a transfer function H_3 , and likewise from S₂ via a H_4 to M₂, as shown in Figure 3.

25 The unwanted transfer functions H_3 and H_4 are in general complex and in many applications variable with respect to time.

Known methods for eliminating the effect of H_3 and H_4 (echo-cancellation) consist in synthesizing a correction signal in the form of a copy of the signal provided by H_3 and H_4 respectively, and subtracting, and subtracting that from the incoming signal, as e.g. shown in Figure 4.

30 The circuit can be made adaptive by means of feedback if it may be assumed that transmitted and received signals are uncorrelated (statistically independent).

Known methods for synthesizing the transfer function $\hat{H}_3$ use:

a) Convolution integral: $y(t) = \int h(\tau) \cdot x(t-\tau) d\tau$
 45 where $h(\tau)$ is the impulse response of the line.

b) Transversal filter: $y(t) = \sum_{n=1}^N \alpha_n \cdot x(t-\tau)$

where α_n is the coefficients of the filter and where $x(t)$ and $y(t)$ are input and output signals of $\hat{H}_3$, respectively.

Both methods can be made adaptive by repeated measurement of the impulse response of the line and modifications of $h(\tau)$ and α_n , respectively, dependent therefrom. A great disadvantage of both methods is that they require complicated apparatus with great demand for computing capacity.

According to the present invention there is provided a directional coupler for duplex transmission for use with a transmitter/receiver unit, including a device for providing a correction signal and a compensation circuit to which the correction signal is applied to suppress that portion of the signal received by the receiver which is derived from the signal transmitted by the transmitter, wherein the

coupler includes a memory unit capable of storing values of the correction signal, the values being assigned to respective ones of the different possible variants within a selected period of time, of time functions coming from the transmitter and a decoder connected between the transmitter and the memory unit for detection of actual, transmitted signal variants, the decoder including means for selection in the memory unit of the values of the correction signal assigned to the actual signal variants and wherein the compensation circuit is connected to the memory unit for utilisation of the assigned values as correction signals.

The invention is illustrated by way of example, with reference to Figures 5 to 16 of the accompanying drawings, in which:

Figure 5 illustrates a step-response for H_3 .

Figure 6 is an example of a biphase signal.

Figure 7 illustrates the principle of the invention.

Figure 8 depicts a simple embodiment of a directional coupler according to the invention.

Figure 9 depicts a modification of the invention as it has been illustrated in Figure 7.

Figure 10 depicts an adaptive version of the directional coupler according to the invention.

Figure 11 depicts a digital integrator in the coupler of Figure 10.

Figure 12 depicts a simplified adaptive version of the coupler of Figure 10.

Figure 13 depicts an example of the biphase signal.

Figure 14 depicts a modification of the coupler of Figure 8.

Figure 15 depicts a modification of the coupler of Figure 12.

Figure 16 depicts an analogue embodiment of the coupler.

What makes H_3 complex is the output signal being dependent on the time function of the input signal over a certain time, see Figure 5.

In practice there is a finite memory time τ which is important.

If $x(t)$ within a period of time τ has a finite number of possible variants of time functions, it is possible to tabulate the corresponding variants of the value y and use the description the time function of $x(t)$ to choose a y -value.

Realisation becomes particularly simple if $x(t)$ is e.g. a digital biphase signal, since an array of e.g. three periods of a biphase signal can only appear in $2^3 = 8$ different ways, which are shown in Figure 6.

For practical lengths of lines τ may e.g. be approximately of the duration 2-4 biphase periods, i.e. the number of different antecedents (previously transmitted signals) is $2^2 = 2^4 = 4$ to 16, for a definite point of time during the biphase period. The number of points of time in the period necessary to observe/synthesize may be from 1 to 8 or more, dependent on synchronizing conditions and other system specifications. Thus, the number of different values of y at the sampling times is 4 to 128. Practical figures are: 3 periods antecedents and 8 samples per period, i.e. a total of $2^3 \times 8 = 64$ different values of y .

Figure 7 illustrates how according to the present invention one may provide a circuit for synthesizing

the signal which is to compensate for the effect of transfer functions H_2 , which, as explained above, is caused by reflections of the transmitted signal from S_1 and crosstalk due to non-ideal balancing of the line. In Figure 7, HUK is a memory unit and ADR is a detector detecting the actual variant of time function from the transmitter S_1 , and generating the memory address where the assigned value of the actual variant of the signal transmitted from S_1 is stored.

The array of assigned values coming from the memory unit yield the correction signal, which is subtracted from the received signal in a compensation circuit KK.

The memory must contain information about the actual transmission channel, so that the signal T , which the circuit H_3 provides, is equal to the incoming signal R when S_2 does not transmit. The difference signal S then becomes zero. When S_2 later starts to transmit, the circuit will subtract from the incoming signal R that portion which is caused by its own transmitted signal and the difference S will be the portion which is caused by transmitted signal from S_2 via the transfer function H_2 .

Figure 8 illustrates an embodiment where the memory unit HUK is a digital, read-only memory, and where the correction signal is converted to analogue form in a digital-to-analogue converter D/A. The compensation circuit is an analogue summing circuit Σ .

As a requirement for an adaptive version of the directional coupler the transmitted and received signals must be uncorrelated over a certain period of time (statistically independent), but they may be synchronous or asynchronous.

If one observes the instantaneous value of received signal S at M_1 , see Figure 7, for several occasions of a definite sequence of the transmitted signal from S_1 , corresponding to a definite memory address, the average value will be approximately zero as a result of the signals being uncorrelated. A change of the transfer function H_2 will however provide a systematic shift of the average value of the received signal.

A registration of said shift and a corresponding modification of the assigned value will bring the content of the memory in conformity with H_2 once more. In Figure 9 a general diagram of such an adaptive version of the directional coupler is shown.

Figure 10 illustrates an embodiment having a digital write/read memory and an analogue-to-digital converter and adder unit in the feed-back.

The averaging of the received signal takes place in that the analogue-to-digital converter, the adder unit and the memory for a definite address constitute a digital integrator, see Figure 11, defined by the following equation:

$$Y_i = Y_{i-1} + \alpha X_i \quad (1)$$

$$\text{The increment } \Delta Y = \alpha X_i \quad (2)$$

By numerical integration:

$$Y = -\sum_{T} X_i \Delta t \quad (3)$$

and

$$\Delta Y = \frac{\Delta t}{T} X \quad (4)$$

where Δt = step length, and

T = the time constant of the integrator

Comparing equation (2) and (4) yields:

$$\alpha = \frac{\Delta t}{T}$$

α is determined by the conversion constant of the analogue-to-digital converter and a possible rescaling upon connection to the adder unit and influences the transient time of the integrator. The longer the permissive transient time, the more accurate will be the synthesized signal T .

It has been proved that the analogue-to-digital converter in Figure 10, which is a comparatively large and complicated circuit, may be omitted by a coupling as shown in Figure 12, where the compensation circuit is a comparator K.

The circuit of Figure 10 uses the amount (with sign) of the deviation to modify the content in the memory.

The simplified adaptive circuit in Figure 12 uses only the sign of the deviation by adding +1, or possibly -1, to the content of the memory.

The difference between the two circuits is mainly that the first one adapts somewhat faster when turned on or upon a large and abrupt change of H_2 . Both circuits will however during normal operation be equally accurate.

An alternative method is as follows. An increased accuracy of the synthesized signal T requires that a longer portion of the antecedents of the biphase signal is considered, i.e. more of the previously transmitted signals. This yields a doubling of the size of the memory for an increase of one period of the antecedents of the biphase signal. For comparatively long lines and high bit-frequencies, it will be required that comparatively extensive antecedents are considered, and in order to save memory space it may be advantageous to provide a somewhat different device as described below.

Instead of letting the memory contain the actual figures which are to be applied to the digital-to-analogue converter, one may in the memory retain parts of the actual figures which have to be added with signs dependent of the antecedents of the transmitted signal in order to obtain the finite output value.

If one considers the biphase signal formed by an array of single pulses having a form shown in Figure 13, the instantaneous value of the synthesized signal may be said to consist of a contribution from a portion of the closest preceding single pulses which the biphase signal is composed of.

If the memory thus contains figures for the effect of a single pulse, for an array of moments after the commencement of the pulse (the pulse response of the line), the instantaneous value can be recreated by adding with sign the content of the memory spaces corresponding to complete biphase periods in time backwards from the sampling moment. The signs are determined from the transmitted biphase signal. Logic 1-pulse provides e.g. + and logic

O-pulse provides —. As many figures must be added as the number of periods of antecedents of the biphasic signal considered necessary.

- 5 For a system with e.g. 7 periods of antecedents and 8 samples per period the memory may be arranged in registers as follows:

10 $A_0 A_1 A_2 A_3 A_4 A_5 A_6 A_7$
 $B_0 B_1 B_2 B_3 B_4 B_5 B_6 B_7$
 $C_0 C_1 C_2 C_3 C_4 C_5 C_6 C_7$
 $D_0 D_1 D_2 D_3 D_4 D_5 D_6 D_7$
 $E_0 E_1 E_2 E_3 E_4 E_5 E_6 E_7$
 $F_0 F_1 F_2 F_3 F_4 F_5 F_6 F_7$
 $G_0 G_1 G_2 G_3 G_4 G_5 G_6 G_7$

- 15 where the subscript indicates sample number (0.7). Thus, the different registers (A, B, C etc.) contain figures for the effect of a logic pulse (see Figure 13) at the 1st, 2nd, 3rd etc. period after the pulse was transmitted. (It is assumed that the numerical value of the effect is equal for a logic 1-pulse and a logic 0-pulse). Figure 14 illustrates how such a circuit can be constructed. ADR denotes an address decoder and sign logic, F₁ sign selector, AKK accumulator register and ADD₁ adder unit.

The circuit may be made adaptive by updating the registers on the basis of the sign of the output signal S (see Figure 15).

- 30 In order to save computing time it may e.g. be sufficient that only one of the register spaces is updated for each sample. In the course of 56 samples all the spaces will have received an updating. In practice this has for a number of applications proved to be sufficiently frequent, even though the circuit in Figure 15 will then adapt slower than the circuit in Figure 12.

- The sign logic (included in the ADR unit) determines the sign of the actual periods of the antecedents and provides the sign for the register under treatment. The sign selector sets the correct sign on the figures arriving from the memory.

- 40 The unit F₂ in Figure 15 determines if a "1" is to be added or subtracted to or from the content of a register subjected to updating. This is determined by the sign of the register in question and the sign of the deviation S according to normal sign rules (— and + is —, — and — is +, etc.).

- The principle on which the circuit is based may also be considered used for other types of pulses, e.g. normal binary code, but one must then define more types of pulse elements (than those in Figure 13), and corresponding registers for the effect of these.

- 55 The number of memory spaces necessary in the system shown in Figure 15 becomes

$$N = n \cdot m$$

- 60 where n is the number of samples per period of the biphasic signal and m is equal to the number of periods of antecedents. In the previous described system (Figure 12) there is correspondingly obtained

65 $N = n \cdot 2^m$

This system will thus always require more memory spaces, but this is compensated by leaving the rest of the equipment much simpler and setting far less requirements with respect to speed and therefore power consumption. This in turn influences the package density and finally the price.

- 70 For many practical applications it is considered sufficient to consider 3-4 periods of the antecedents, and in that case the circuit of Figure 10 is preferred.

- 75 Figure 16 illustrates an adaptive version of the analogue embodiment of the coupler. In this example each memory location is embodied by a capacitor C and a switch B. The stored values are given by the charges on the capacitors. The coupler is made adaptive by means of introducing a resistor in the feed-back between the summation circuit and the memory HUK for modification of the values selected by the decoder ADR.

85 CLAIMS

1. A directional coupler for duplex transmission for use with a transmitter/receiver unit, including a device for providing a correction signal and a compensation circuit to which the correction signal is applied to suppress that portion of the signal received by the receiver which is derived from the signal transmitted by the transmitter, wherein the coupler includes a memory unit capable of storing values of the correction signal, the values being assigned to respective ones of the different possible variants within a selected period of time, of time functions coming from the transmitter, and a decoder connected between the transmitter and the memory unit for detection of actual, transmitted signal variants, the decoder including means for selection in the memory unit of the values of the correction signal assigned to the actual signal variants and wherein the compensation circuit is connected to the memory unit for utilisation of the assigned values as correction signals.

2. A directional coupler according to claim 1, and including a digital-to-analogue converter arranged between the memory unit and the compensation circuit, the memory unit being a digital read-only memory and the compensation circuit being an analogue summation circuit.

3. A directional coupler according to claim 1, where the signal transmitted from the transmitter is considered composed of a finite number of different elements, and wherein the memory unit is arranged to contain partial values of the correction signal corresponding to the effect of the different elements, and wherein an adder unit is connected between the memory unit and the compensation circuit whereby the correction signal is provided by addition of the actual elements as detected by the decoder and transmitted from the transmitter during a selected period of time.

4. A directional coupler according to claim 3, wherein the adder unit is an accumulating adder unit connected to the memory unit through a sign selector controlled by the decoder, and wherein a digital-to-analogue converter is provided between the adder unit and the compensation circuit, the memory unit being a digital read-only memory, and the



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3. A directional coupler according to claim 1, where the signal transmitted from the transmitter is considered composed of a finite number of different elements, and wherein the memory unit is arranged to contain partial values of the correction signal corresponding to the effect of the different elements, and wherein an adder unit is connected between the memory unit and the compensation circuit whereby the correction signal is provided by addition of the actual elements as detected by the decoder and transmitted from the transmitter during a selected period of time.

4. A directional coupler according to claim 3, wherein the adder unit is an accumulating adder unit connected to the memory unit through a sign selector controlled by the decoder, and wherein a digital-to-analogue converter is provided between the adder unit and the compensation circuit, the memory unit being a digital read-only memory, and the



compensation circuit being an analogue summation circuit.

5. A directional coupler according to claim 1, and provided with means providing feed-back from the output of the compensation circuit to the data input of the memory unit for modification of values of the correction signal selected by the decoder which thereby adapt themselves to changes in the transmission conditions in time, the memory unit being a write/read memory.

6. A directional coupler according to claim 5, wherein the means providing the feed-back includes an analogue-to-digital converter which, in series with an adder unit and the memory unit, provides a digital integrator for each selected value, the output of the memory unit partly being connected to the compensation circuit via a digital-to-analogue converter and partly being connected to the input of the adder unit, the compensation circuit being an analogue summation circuit.

7. A directional coupler according to claim 5, wherein the means providing feed-back includes an adder unit for adding of +1 or -1 to a selected value, the memory unit having its output partly connected to the compensation circuit via a digital-to-analogue converter and partly connected back to the input of the adder unit, the compensation circuit being constituted by a comparator.

8. A directional coupler according to claims 3 and 5, wherein the adder unit is an accumulating adder unit which is connected to the memory unit through a sign selector controlled by the decoder, wherein a digital-to-analogue converter is provided between the adder unit and the compensation circuit, the memory unit being a digital read-only memory and the compensation circuit being constituted by a comparator, and wherein a second adder unit and a second sign selector controlled by the decoder is introduced into the feed-back, the output of the memory unit being connected to the input of the second adder unit for modification of the values by adding +1 or -1.

9. A directional coupler according to claim 5, wherein the memory unit is arranged to store assigned values in analogue form.

10. A directional coupler according to claim 9, wherein the assigned values are represented by charges on capacitors, wherein the decoder selects the actual value of the correction signal by means of a switch for each capacitor, the switch connecting the actual capacitor to the input of the compensation circuit and wherein the feed-back takes place through a resistor.

11. A directional coupler according to claim 1 and substantially as hereinbefore described with reference to Figure 8 of the accompanying drawings.

12. A directional coupler according to claim 1 and substantially as hereinbefore described with reference to Figure 10 of the accompanying drawings.

13. A directional coupler according to claim 1 and substantially as hereinbefore described with reference to Figure 12 of the accompanying drawings.

14. A directional coupler according to claim 1

and substantially as hereinbefore described with reference to Figure 14 of the accompanying drawings.

15. A directional coupler according to claim 1 and substantially as hereinbefore described with reference to Figure 15 of the accompanying drawings.

16. A directional coupler according to claim 1 and substantially as hereinbefore described with reference to Figure 16 of the accompanying drawings.

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