

SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SEMICONDUCTOR DEVICE

CROSS-REFERENCE TO RELATED APPLICATION

5 **[0001]** This application claims priority under 35 U.S.C. §119 to Korean Patent Application No. 10-2024-0170566 filed on November 26, 2024, which is incorporated herein by reference in its entirety.

BACKGROUND

10 **1. Technical Field**

[0002] Embodiments of the present disclosure relate to an electronic device, and more particularly, to a semiconductor device and a manufacturing method of the semiconductor device.

15 **2. Related Art**

[0003] The degree of integration of a semiconductor device is primarily determined by an area occupied by a unit memory cell. Recently, as the integration of memory cells formed in a single layer on a substrate approaches its physical limits, a three-dimensional
20 semiconductor device that stacks memory cells vertically on a substrate has been proposed. Furthermore, in order to improve the operational reliability of such a semiconductor device, various structures and manufacturing methods have been developed.

SUMMARY

[0004] In an embodiment, a semiconductor device may include: channel pillars arranged along a first direction and a second direction intersecting the first direction, wherein the channel pillars are spaced
5 apart by a first interval in the first direction and a second interval in the second direction, the first interval being smaller than the second interval; a select line surrounding multiple channel pillars arranged in the first direction and extending in the first direction; word lines stacked above the select line in a third direction perpendicular to the
10 first and the second directions; and local bit lines extending through the word lines in the third direction and electrically connected to the channel pillars.

[0005] In an embodiment, a semiconductor device may include: local lines arranged in a first direction and a second direction that
15 intersects the first direction and extending in a third direction perpendicular to the first and the second directions; global lines extending in the second direction; and select transistors connected between the local lines and the global lines, each select transistors including a corresponding one of channel pillars, the channel pillars
20 being spaced apart by a first interval in the first direction and a second interval in the second direction, the first interval being different than the second interval.

[0006] In an embodiment, a manufacturing method of a semiconductor device may include: forming channel pillars arranged

in a first direction and a second direction that intersects the first direction; forming a select line surrounding multiple channel pillars and extending in the first direction; forming insulating pillars extending through the select line in a third direction perpendicular to the first and the second directions; and forming a contact plug electrically connected to the select line between two adjacent insulating pillars.

[0007] In an embodiment, a method of manufacturing a semiconductor device may include: forming global bit lines; forming channel pillars over the global bit lines in a third direction, the channel pillars being arranged in a first direction and a second direction intersecting the first direction and spaced apart by an interval in the first direction smaller than an interval in the second direction, the third direction being perpendicular to both the first and second directions; forming select lines, each configured to surround multiple channel pillars in the first direction and extending in the first direction; forming local bit lines on the select lines in the third direction, the local bit lines being connected to the channel pillars, respectively, and extending in the third direction; and forming word lines surrounding the local bit lines and stacked in the third direction.

[0008] In an embodiment, a semiconductor device includes first and second select lines extending in a first direction, the first and second select lines being offset from each other in a second direction

that is different from the first direction; first and second sets of channel pillars, the first set of channel pillars being associated with the first select line and the second set of channel pillars being associated with the second select line; word lines provided above the first and second select lines in a third direction that is different from the first direction and the second direction; and local bit lines extending through the word lines in the third direction and electrically coupled to the channel pillars.

[0009] The channel pillars in the first set are separated from adjacent channel pillars in the same set by a first interval in the first direction and separated from adjacent channel pillars in the second set by a second interval in the second direction, the first interval being smaller than the second interval.

[0010] The first select line surrounds the channel pillars in the first set, and the second select line surrounds the channel pillars in the second set. Each of the first direction, the second direction, and the third direction is substantially orthogonal to the other two directions.

BRIEF DESCRIPTION OF THE DRAWINGS

[0011] FIGS. 1A to 1D illustrate the structure of a semiconductor device in accordance with an embodiment.

[0012] FIGS. 2A to 2D illustrate the structure of a semiconductor device in accordance with an embodiment.

[0013] FIGS. 3A, 4A, 5A, 6A, 7A, 8A, 9A, and 10A, FIGS. 3B, 4B, 5B, 6B, 7B, 8B, 9B, and 10B, and FIGS. 3C, 4C, 5C, 6C, and 7C describe a manufacturing method of a semiconductor device in accordance with an embodiment.

5 **[0014]** FIGS. 11A and 11B illustrate the structure of a semiconductor device in accordance with an embodiment.

[0015] FIG. 12 is a circuit diagram illustrating a cell array of a semiconductor device in accordance with an embodiment.

[0016] FIG. 13 is a flowchart for describing a manufacturing method
10 of a semiconductor device in accordance with an embodiment.

[0017] FIGS. 14A to 14F describe a manufacturing method of a semiconductor device in accordance with an embodiment.

[0018] FIGS. 15A, 16A, and 17A and FIGS. 15B, 16B, and 17B describe a manufacturing method of a semiconductor device in
15 accordance with an embodiment.

[0019] FIG. 18 is a cross-sectional view illustrating the structure of a semiconductor device in accordance with an embodiment.

[0020] FIG. 19 is a configuration diagram of a semiconductor device in accordance with an embodiment.

20 **[0021]** FIG. 20 is a configuration diagram of a semiconductor device in accordance with an embodiment.

DETAILED DESCRIPTION

[0022] Various embodiments are directed to a semiconductor device

having a stable structure and improved characteristics and a manufacturing method of the semiconductor device.

[0023] By stacking memory cells in three dimensions, it is possible to improve the degree of integration of a semiconductor device. It is
5 also possible to provide a semiconductor device having a stable structure and improved reliability.

[0024] Hereafter, embodiments in accordance with the technical spirit of the present disclosure will be described with reference to the accompanying drawings.

10 **[0025]** FIGS. 1A to 1D illustrate the structure of a semiconductor device in accordance with an embodiment. FIG. 1A is a plan view, FIG. 1B is a cross-sectional view taken along line A-A' of FIG. 1A, FIG. 1C is a cross-sectional view taken along line B-B' of FIG. 1A, and FIG. 1D is a circuit diagram.

15 **[0026]** Referring to FIGS. 1A to 1C, the semiconductor device may include channel pillars 12, a select line 13, and a local line 17. The semiconductor device may further include one or more of a global line 11, a gap-fill insulating layer 14, an interlayer insulating layer 15, a gate insulating layer 16, a contact plug 18, and insulating pillars 19.
20 Here, the global line 11 may be a global bit line, and the local line 17 may be a local bit line.

[0027] In a plan view, the channel pillars 12 may be arranged in (e.g., a matrix form along) a first direction I and a second direction II, where the second direction II intersects the first direction I. The

channel pillars 12 have a first interval W1 in the first direction I and a second interval W2 in the second direction II. The first interval W1 and the second interval W2 may be different from each other. In an implementation, the first interval W1 may be smaller than the second interval W2.

[0028] Each channel pillar 12 may include a first semiconductor layer 12A, a second semiconductor layer 12B, and a third semiconductor layer 12C. The first semiconductor layer 12A, the second semiconductor layer 12B, and the third semiconductor layer 12C may be stacked in a third direction III. The third direction III may be perpendicular to the first direction I and the second direction II. In an embodiment, the channel pillar 12 extends orthogonal to the first and second directions I and II and has a dimension in the third direction III that is greater than its dimension in the first direction I or the second direction II. The second semiconductor layer 12B may be located between the first semiconductor layer 12A and the third semiconductor layer 12C.

[0029] The first semiconductor layer 12A and the third semiconductor layer 12C may function as junctions, and the second semiconductor layer 12B may serve as a channel region. The first semiconductor layer 12A, the second semiconductor layer 12B, and the third semiconductor layer 12C may each include N-type impurities, P-type impurities, or be formed as intrinsic semiconductors. For example, the first semiconductor layer 12A may include N-type impurities, the

second semiconductor layer 12B may include P-type impurities, and the third semiconductor layer 12C may include N-type impurities. Alternatively, the first semiconductor layer 12A may include P-type impurities, the second semiconductor layer 12B may include N-type impurities, and the third semiconductor layer 12C may include P-type impurities. In another configuration, the first semiconductor layer 12A may include N-type impurities, the second semiconductor layer 12B may be formed as an intrinsic semiconductor, and the third semiconductor layer 12C may include N-type impurities. Additionally, the first semiconductor layer 12A may include P-type impurities, the second semiconductor layer 12B may be formed as an intrinsic semiconductor, and the third semiconductor layer 12C may include P-type impurities.

[0030] The select line 13 extends in the first direction I and is associated with a group of channel pillars 12 arranged in the first direction I. In an embodiment, each of the select lines 13 is associated with a group or set of channel pillars, with the select line 13 surrounding or substantially surrounding the corresponding group of channel pillars. The multiple channel pillars 12 arranged in the first direction I may share the select line 13. For example, the select line 13 may surround the second semiconductor layer 12B of the channel pillar 12, while not surrounding the first semiconductor layer 12A and the third semiconductor layer 12C.

[0031] The select line 13 may extend in the first direction I. The

select line 13 may include two parallel first portions 13A extending along the first direction I and second portions 13B, each connecting the two parallel first portions 13A. The second portions 13B may be located between the multiple channel pillars 12, between insulating pillars 19, and between a channel pillar 12 and an insulating pillar 19, along the first direction I.

[0032] The gate insulating layers 16 may surround sidewalls of the channel pillars 12, and may be interposed between the channel pillars 12 and the select line 13.

10 **[0033]** The global lines 11 may extend in the second direction II. The channel pillars 12 may be located on the global lines 11 in the third direction III. The global line 11 may be connected to a plurality of channel pillars 12 arranged in the second direction II. The first semiconductor layer 12A and the global line 11 may be connected to each other.

15 **[0034]** The local lines 17 may be arranged in a matrix form along the first direction I and the second direction II, and may be located to correspond to the channel pillars 12, respectively. The local lines 17 may each have a pillar shape. The local lines 17 may extend in the third direction III, for example, in a vertical direction. The local lines 20 17 may be located on the channel pillars 12 in the third direction III. The third semiconductor layer 12C and the local line 17 may be connected to each other. For example, the channel pillar 12 may be connected between the global bit line and the local bit line.

[0035] Select transistors ST may be located in regions where the global lines 11 intersects the select lines 13. Each select transistor ST may include a channel pillar 12, and the channel pillar 12 may include a first semiconductor layer 12A, a second semiconductor layer 12B, and a third semiconductor layer 12C. Here, the first semiconductor layer 12A may be a first junction, the third semiconductor layer 12C may be a second junction, and the second semiconductor layer 12B may be a channel region. The select line 13 may surround the channel region.

[0036] The gap-fill insulating layers 14 may be located between the global lines 11 in the first direction I. The gap-fill insulating layers 14 may also be located between the first semiconductor layers 12A along the first direction I and the second direction II. The interlayer insulating layer 15 may be located to cover the select line 13. The local lines 17 may penetrate through the interlayer insulating layer 15 and be connected to the channel pillars 12.

[0037] The insulating pillars 19 may penetrate through the select lines 13, and may be located on the global lines 11. The insulating pillars 19 may be arranged in a matrix form along the first direction I and the second direction II. The insulating pillars 19 may be formed by filling regions vacated by the removal of the channel pillars 12 with an insulating material. The insulating pillars 19 may be integrally connected to the interlayer insulating layer 15.

[0038] The contact plug 18 may penetrate through the interlayer

insulating layer 15, and may be electrically connected to the select line 13. The contact plug 18 may be connected to the second portion 13B of the select line 13 between the insulating pillars 19 adjacent to each other in the first direction I. The contact plug 18 may surround
5 an upper surface and sidewalls of the second portion 13B. A select signal may be applied to the select line 13 through the contact plug 18, enabling the select transistor ST to be turned on or off in response to the select signal.

[0039] Referring to FIG. 1D, the semiconductor device may include
10 select lines SL0 to SLm, global lines GL0 to GLk, local lines LL00 to LLkm, select transistors ST, a global line decoder GL decoder, and a select line decoder SL decoder. The select transistors ST may be connected between the global lines GL0 to GLk and the local lines LL00 to LLkm. Here, the global lines GL0 to GLk may be global bit
15 lines, and the local lines LL00 to LL33 may be local bit lines. The global line decoder GL decoder may be a global bit line decoder. k and m may be integers of 0 or more.

[0040] The global lines GL0 to GLk may be connected to the global line decoder GL decoder. The global line decoder GL decoder may
20 include switches respectively connected to the global lines GL0 to GLk. By turning on or off the switches based on addresses, it is possible to selectively activate the global lines GL0 to GLk.

[0041] The select lines SL0 to SLm may be connected to gate electrodes of the select transistors ST, and may be connected to the

select line decoder SL decoder. The select line decoder SL decoder may include switches respectively connected to the select lines SL0 to SLm. By turning on or off the switches based on addresses, it is possible to selectively activate the select lines SL0 to SLm.

5 **[0042]** According to the configuration described above, the connection between the global lines GL0 to GLk and the local lines LL00 to LLkm may be controlled by the select transistors ST. The local lines LL00 to LLkm, for example, the local bit lines, may be selected using the select line decoder SL decoder and the global line decoder GL decoder.

10 **[0043]** FIGS. 2A to 2D illustrate a semiconductor device in accordance with an embodiment. FIG. 2A is a plan view, FIG. 2B is a cross-sectional view taken along line A1-A1' of FIG. 2A, FIG. 2C is a cross-sectional view taken along line B1-B1' of FIG. 2A, and FIG. 2D is a circuit diagram.

15 **[0044]** Referring to FIGS. 2A to 2C, the semiconductor device may include channel pillars 22, a select line 23, and a local line 27. The semiconductor device may further include one or more of a global line 21, a gap-fill insulating layer 24, an interlayer insulating layer 25, a gate insulating layer 26, a contact plug 28, and insulating pillars 29.

20 Here, the global line 21 may be a global bit line, and the local line 27 may be a local bit line.

[0045] The channel pillars 22 may be arranged in a zigzag pattern along the first direction I and the second direction II intersecting the first direction I. The channel pillars 22 adjacent to each other in the

second direction II may be arranged with their centers staggered, forming the zigzag pattern. Each channel pillar 22 may include a first semiconductor layer 22A, a second semiconductor layer 22B, and a third semiconductor layer 22C.

5 **[0046]** The channel pillars 22 have a first interval W1 in the first direction I and a second interval W2 or a third interval W3 in the second direction II. The first interval W1 and the second interval W2 may be different from each other, and the second interval W2 and the third interval W3 may be different from each other. The first interval
10 W1 may be smaller than the second interval W2, and the third interval W3 may be smaller than the second interval W2.

[0047] The select line 23 may surround the channel pillars 22, and may extend in the first direction I. For example, the channel pillars 22 arranged in the first direction I may constitute one row, and the
15 select line 23 may surround at least two rows. The channel pillars 22 surrounded by the same select line 23 may be spaced apart from each other by the first interval W1 in the first direction I and the third interval W3 in the second direction II. The channel pillars 22 surrounded by different select lines 23 may be spaced apart from
20 each other by the second interval W2 in the second direction II.

[0048] Referring to FIG. 2D, the semiconductor device may include select lines SL0 to SLm, global lines GL00 to GLk1, local lines LL00_0 to LLkm_1, select transistors ST, a global line decoder GL decoder, and a select line decoder SL decoder. The select transistors ST may

be connected between the global lines GL00 to GLk1 and the local lines LL00_0 to LLkm_1.

[0049] The global lines GL00 to GLk1 may be connected to the global line decoder GL decoder. The select lines SL0 to SLm may be connected to gate electrodes of the select transistors ST, and may be connected to the select line decoder SL decoder.

[0050] According to the configuration described above, the connection between the global lines GL00 to GLk1 and the local lines LL00_0 to LLkm_1 may be controlled by the select transistors ST. The local lines LL00_0 to LLkm_1, for example, the local bit lines, may be selected using the select line decoder SL decoder and the global line decoder GL decoder.

[0051] FIGS. 3A, 4A, 5A, 6A, 7A, 8A, 9A, and 10A, FIGS. 3B, 4B, 5B, 6B, 7B, 8B, 9B, and 10B, and FIGS. 3C, 4C, 5C, 6C, and 7C illustrate a manufacturing method of a semiconductor device in accordance with an embodiment. FIGS. 3A, 4A, 5A, 6A, 7A, 8A, 9A, and 10A are plan views, FIGS. 3B, 4B, 5B, 6B, and 7B are cross-sectional views taken along lines C-C' of FIGS. 3A, 4A, 5A, 6A, and 7A, respectively, FIGS. 3C, 4C, 5C, 6C, and 7C are cross-sectional views taken along lines D-D' of FIGS. 3A, 4A, 5A, 6A, and 7A, respectively, and FIGS. 8B, 9B, and 10B are cross-sectional views taken along lines E-E' of FIGS. 8A, 9A, and 10A, respectively.

[0052] Referring to FIGS. 3A to 3C, a semiconductor layer 32 is formed on a first conductive layer 31. The semiconductor layer 32

includes a first semiconductor layer 32A, a second semiconductor layer 32B, and a third semiconductor layer 32C that are sequentially stacked in the third direction III. For example, the first semiconductor layer 32A is an N-type semiconductor layer and formed on the first conductive layer 31, the second semiconductor layer 32B is a P-type semiconductor layer and formed on the first semiconductor layer 32A, and the third semiconductor layer 32C is an N-type semiconductor layer and formed on the second semiconductor layer 32B.

10 **[0053]** Referring to FIGS. 4A to 4C, semiconductor lines 32L extending in the second direction II are formed by etching or patterning the semiconductor layer 32. Subsequently, global lines 31A extending in the second direction II are formed by etching the first conductive layer 31. Here, the global lines 31A may be global bit lines.

15 **[0054]** Subsequently, first gap-fill insulating layers 33A may be formed between the semiconductor lines 32L and between the global lines 31A. The first gap-fill insulating layers 33A may extend in the second direction II.

20 **[0055]** Referring to FIGS. 5A to 5C, channel pillars 32P are formed by etching the semiconductor lines 32L. The channel pillars 32P may be arranged in a matrix form along the first direction I and the second direction II. The channel pillars 32P may have a first interval W1 in the first direction I and a second interval W2 in the second direction II,

and the first interval W1 may be smaller than the second interval W2.

For example, trenches extending in the first direction I are formed by etching the semiconductor lines 32L and the first gap-fill insulating layers 33A. The channel pillars 32P adjacent to each other in the

5 second direction II may be separated from each other by the trenches. Subsequently, second gap-fill insulating layers 33B may be formed in the trenches.

[0056] Referring to FIGS. 6A to 6C, sidewalls of the channel pillars 32P are exposed by etching the first gap-fill insulating layer 33A and

10 the second gap-fill insulating layer 33B. For example, the first gap-fill insulating layer 33A and the second gap-fill insulating layer 33B are etched by an etch-back process. Through this, the second semiconductor layer 32B and the third semiconductor layer 32C of each channel pillar 32P may be exposed.

15 **[0057]** Subsequently, gate insulating layers 34 may be formed on the channel pillars 32P. The gate insulating layers 34 may be formed to surround the exposed sidewalls of the channel pillars 32P. For example, the sidewalls of the second semiconductor layer 32B and third semiconductor layer 32C of each channel pillar 32P are

20 surrounded by the gate insulating layer 34. The gate insulating layers 34 may each include an oxide.

[0058] Subsequently, a second conductive layer 35 is formed on the gate insulating layers 34 and covers upper surfaces of the channel pillars 32P. Because the channel pillars 32P adjacent to each other in

the first direction I have a relatively small interval, the second conductive layer 35 may fill a space between the channel pillars 32P adjacent to each other in the first direction I. On the other hand, because the channel pillars 32P adjacent to each other in the second direction II have a relatively great interval, the second conductive layer 35 may only partially fill a space between the channel pillars 32P adjacent to each other in the second direction II. The second conductive layer 35 may include a metal such as tungsten.

[0059] Referring to FIGS. 7A to 7C, select lines 35A extending in the first direction I are formed by etching the second conductive layer 35. For example, the second conductive layer 35 is etched using an etch-back process. As the second conductive layer 35 is etched back, the upper surfaces of the channel pillars 32P, the gate insulating layers 34, and upper surfaces of the second gap-fill insulating layers 33B may be exposed.

[0060] Subsequently, a treatment process may be performed on the channel pillars 32P. For example, a CO₂ laser annealing process may be performed. Through this, electron mobility of the channel pillars 32P may be increased, and channel characteristics may be improved.

[0061] Each select line 35A may fill the space between the channel pillars 32P adjacent to each other in the first direction I. Each select line 35A may extend in the first direction I while surrounding sidewalls of the channel pillars 32P arranged in the first direction I. The select lines 35A may each have a height sufficient to surround the second

semiconductor layers 32B, while potentially not surrounding the third semiconductor layers 32C. Each select line 35A may include two parallel first portions 35AA extending in the first direction I and a second portion 35AB located between the channel pillars 32P, connecting the two parallel first portions 35AA.

[0062] Referring to FIGS. 8A and 8B, first openings OP1 are formed by removing some of the channel pillars 32P. The global lines 31A may be exposed through the first openings OP1. For example, a mask pattern exposing ends of the select lines 35A may be formed, and the channel pillars 32P exposed by the mask pattern may be removed. The exposed channel pillars 32P may be removed using a dip-out process. The dip-out process may be a wet etching process having a high etching selectivity with respect to the channel pillars 32P. During the dip-out process, the gate insulating layers 34 may be removed together with the channel pillars 32P.

[0063] Referring to FIGS. 9A and 9B, insulating pillars 36 may be formed within the first openings OP1. The insulating pillars 36 may penetrate through the select lines 35A, and may be located above the global lines 31A. In other words, the select line 35A may fill spaces between the insulating pillars 36 arranged in the first direction I, and may extend in the first direction I while surrounding sidewalls of the insulating pillars 36.

[0064] An insulating layer 37 may be formed above the insulating pillars 36 and the channel pillars 32P. The insulating layer 37 may fill

the spaces between the channel pillars 32P. The insulating pillars 36 and the insulating layer 37 may be simultaneously formed, and may constitute a single, integrally connected layer.

[0065] Referring to FIGS. 10A and 10B, an interlayer insulating layer 5 38 may be formed above a resultant structure of FIGS. 9A and 9B. The interlayer insulating layer 38 may be formed above the insulating layer 37. Subsequently, second openings OP2 respectively exposing the select lines 35A are formed. The second openings OP2 may penetrate through the interlayer insulating layer 38 and the insulating 10 layer 37. In a process of forming each second opening OP2, a pair of insulating pillars 36 adjacent to each other in the first direction I may be partially etched, and the second portion 35AB located between the pair of insulating pillars 36 may be exposed.

[0066] Subsequently, contact plugs 39 may be formed in the second 15 openings OP2. The contact plugs 39 may be electrically connected to the select lines 35A, respectively. Each contact plug 39 may be electrically connected to the select line 35A exposed between the insulating pillars 36. The contact plug 39 may be connected to the second portion 35AB of the select line 35A exposed between the pair 20 of insulating pillars 36 adjacent to each other in the first direction I.

[0067] The insulating pillars 36 may be located between the contact plugs 39 and the global lines 31A in the third direction III, providing insulation between the contact plugs 39 and the global lines 31A. A plurality of contact plugs 39 may be arranged in a zigzag pattern or in

a staggered configuration.

[0068] Meanwhile, although not illustrated in FIGS. 10A and 10B, local lines respectively connected to the channel pillars 32P may be formed. Each local line may have a pillar-like shape and may
5 penetrate through the interlayer insulating layer 38 and the insulating layer 37. The local lines may be local bit lines.

[0069] According to the manufacturing method described above, select transistors ST arranged in the first direction I and the second direction II may be formed. The contact plugs 39 respectively
10 connected to the select lines 35A may also be formed. Select signals may be applied to the select lines 35A through the contact plugs 39, enabling the select transistors ST to be turned on or off in response to the select signals.

[0070] FIGS. 11A and 11B illustrate a semiconductor device in
15 accordance with an embodiment. Hereinafter, the content overlapping with the previously described content may be omitted.

[0071] Referring to FIG. 11A, the semiconductor device may include a cell region CELL in which stacked memory cells are located. In addition, the semiconductor device may include peripheral circuits
20 located around the cell region CELL. Here, the peripheral circuit may include a global bit line decoder GBL decoder, a select line decoder SL decoder, and a word line decoder WL decoder.

[0072] The cell regions CELL may be arranged in the first direction I and the second direction II. The select line decoder SL decoder may

be located between two cell regions CELL adjacent to each other in the first direction I. The global bit line decoder GBL decoder may be located between two cell regions CELL adjacent to each other in the second direction II. The word line decoder WL decoder and the select line decoder SL decoder may be adjacent to each other in the first direction I, and the cell region CELL may be located between the word line decoder WL decoder and the select line decoder SL decoder in the first direction I.

[0073] The cell regions CELL and the peripheral circuit may be located at the same level or at different levels in the third direction III. For example, the peripheral circuit may be located below the cell regions CELL. The cell regions CELL and the peripheral circuit, located at different levels, may be electrically connected through an interconnection structure. The interconnection structure may include at least one via and at least one wiring line.

[0074] Referring to FIG. 11B, the semiconductor device may include a peripheral circuit PC, a global bit line GBL, a select line SL, a word line WL, a local bit line LBL, a contact plug CT, a select line contact plug SLCT, a word line contact plug WLCT, a first interconnection structure IC1, and a second interconnection structure IC2. For reference and ease of explanation, an insulating layer and an interlayer insulating layer have been omitted in FIG. 11B.

[0075] The peripheral circuit PC may be located below the global bit line GBL, the select line SL, and the word lines WL. The peripheral

circuit PC may include a global bit line decoder GBL decoder, a select line decoder SL decoder, and a word line decoder WL decoder. The global bit line decoder GBL decoder may be located below the global bit line GBL, and may be connected to the global bit line GBL. The
5 select line decoder SL decoder may be located below the global bit line GBL, and may be connected to the select line SL.

[0076] The global bit line GBL may be located above the peripheral circuit PC, the select line SL may be located above the global bit line GBL, and the word lines WL may be located above the select line SL.
10 The word lines WL may surround the local bit line LBL, and may be stacked in the third direction III. The global bit line GBL and the select line SL may extend in mutually intersecting directions.

[0077] The contact plug CT may be electrically connected to the select line SL, and the select line contact plug SLCT may be electrically
15 connected to the contact plug CT. The select line contact plug SLCT may be electrically connected to the second interconnection structure IC2.

[0078] Channel patterns CP may penetrate through the select line SL. Lower ends of the channel patterns CP may be connected to global bit
20 lines GBL, and upper ends of the channel patterns CP may be connected to the local bit lines LBL. Select transistors ST may be located in regions where the channel patterns CP intersect the select lines SL.

[0079] The first interconnection structure IC1 may be located above

the peripheral circuit PC, and may be located below the select line SL. The first interconnection structure IC1 may be electrically connected to the peripheral circuit PC. The first interconnection structure IC1 may include wiring lines UM0 and UM1 and vias UMC. The second
5 interconnection structure IC2 may be located at a different level from the first interconnection structure IC1 in the third direction III, and may be located above the word lines WL. The second interconnection structure IC2 may be electrically connected to the word line contact plug WLCT, the select line contact plug SLCT, the first interconnection
10 structure IC1, and the like. The second interconnection structure IC2 may include wiring lines M1, M2, and M3 and vias M1C, M2C, and M3C.

[0080] The global bit line GBL may be connected to the global bit line decoder GBL decoder through the first interconnection structure IC1. The contact plug CT and the select line contact plug SLCT may be
15 connected to the select line SL, and the select line SL may be connected to the select line decoder SL decoder through the first interconnection structure IC1 and the second interconnection structure IC2.

[0081] The word lines WL may be stacked above the select line SL, and the local bit line LBL may penetrate through the word lines WL
20 and be connected to a channel pillar of the select transistor ST. Memory cells MC may be located in regions where the local bit line LBL intersects the word lines WL. The memory cells MC may be stacked along the local bit line LBL, and the memory cells MC stacked

along the same local bit line LBL may constitute a memory unit MU.

[0082] Each memory cell MC may include a variable resistance layer capable of reversibly transitioning between different resistance states in response to a voltage or a current applied to the memory cell MC.

5 For example, when the variable resistance layer has a low resistance state, data '1' may be stored, and when the variable resistance layer has a high resistance state, data '0' may be stored.

[0083] For example, the variable resistance layer may include a resistive material in which an electrical path is either formed or
10 disrupted, enabling data storage. The variable resistance layer may include a transition metal oxide or a metal oxide, such as a perovskite-based material.

[0084] For example, the variable resistance layer may have a magnetic tunnel junction (MTJ) structure including a magnetization
15 pinned layer, a tunnel barrier layer, and a magnetization free layer. Data may be stored based on changes in the magnetization direction of the magnetization free layer relative to the magnetization direction of the magnetization pinned layer. The magnetization pinned layer and the magnetization free layer may each include a magnetic
20 material, while the tunnel barrier layer may include a metal oxide.

[0085] For example, the variable resistance layer may include a phase change material or a chalcogenide-based material, capable of changing its phase during a program operation. Through a set operation, the variable resistance layer may transition to a low

resistance crystalline state. Conversely, through a reset operation, the variable resistance layer may transition to a high resistance amorphous state. Accordingly, data may be stored in the memory cell MC based on a difference in resistance corresponding to the phase of the variable resistance layer.

[0086] For example, the variable resistance layer may include a variable resistance material whose resistance changes without undergoing a phase change, or it may include a chalcogenide-based material. The variable resistance layer may retain its phase after the program operation. For example, the variable resistance layer may remain in an amorphous state without transitioning to a crystalline state after the program operation. A threshold voltage of the memory cell MC may vary based on a program voltage applied to the memory cell MC, allowing the memory cell MC to be programmed into at least two states. For example, the memory cell MC may be programmed to a set state or a reset state using program voltages having different polarities. Accordingly, data may be stored in the memory cell MC based on a difference in the threshold voltage of the memory cell MC.

[0087] The word line contact plugs WLCT may be connected to the word lines WL, respectively. For example, the word lines WL may be stacked in a staircase shape, and the word line contact plugs WLCT may be connected to ends of the word lines WL, respectively. The word lines WL may be connected to the word line decoder WL decoder

through the word line contact plugs WLCT, the second interconnection structure IC2, and the first interconnection structure IC1.

[0088] For reference, the word lines WL may also be stacked flatly without the staircase shape, with the word line contact plugs WLCT extending through the word lines WL. In this configuration, the penetrated word lines WL and the word line contact plug WLCT may be insulated from each other. Additionally, the word lines WL and the word line contact plugs WLCT may be connected in a one-to-one manner.

10 **[0089]** According to the structure described above, placing the peripheral circuit PC below the cell region CELL can improve the degree of integration of the semiconductor device. Additionally, by locating the select transistors ST below the stacked word lines WL and connecting the select transistors ST between the global bit lines GBL and the local bit lines LBL, it is possible to select a desired local bit line LBL.

[0090] FIG. 12 is a circuit diagram illustrating a cell array of a semiconductor device in accordance with an embodiment. Hereinafter, the content overlapping with the previously described content may be omitted.

20 **[0091]** Referring to FIG. 12, the semiconductor device may include select lines SL0 to SLm, global bit lines GBL0 to GBLk, local bit lines LBL00 to LBLkm, word lines WL0 to WLn, memory cells MC, select transistors ST, and memory units MU. Here, m, n, and k may be

integers of 0 or more.

[0092] The memory cells MC may be connected between the local bit lines LBL00 to LBLkm and the word lines WL0 to WLn, and may be stacked in the third direction III. Here, the third direction III may be
5 a direction perpendicular to a plane defined by the first direction I and the second direction II. The word lines WL0 to WLn may be connected to gate electrodes of the memory cells MC. Memory cells MC connected to the same local bit line may constitute one memory unit MU.

10 **[0093]** The select transistors ST may be connected to the memory units MU, respectively. The select lines SL1 to SLm may be connected to gate electrodes of the select transistors ST, and may extend in the first direction I. The global bit lines GBL0 to GBLk may extend in the second direction II, and each of the select transistors ST
15 may be connected between a corresponding one of the local bit lines LBL00 to LBLkm and a corresponding one of the global bit lines GBL0 to GBLk.

[0094] With the configuration described above, a desired memory unit MU can be selected using the select transistors ST. This enables set
20 and reset operations to be performed on individual memory units MU.

[0095] FIG. 13 is a flowchart for describing a manufacturing method of a semiconductor device in accordance with an embodiment. Hereinafter, the content overlapping with the previously described content may be omitted.

[0096] First, a peripheral circuit PC may be formed on a substrate (S10). The peripheral circuit PC may include a select line decoder SL decoder, a global bit line decoder GBL decoder, and a word line decoder WL decoder. Subsequently, a first interconnection structure
5 IC1 electrically connected to the peripheral circuit PC may be formed (S20). The first interconnection structure IC1 may include a wiring line, a via, and the like.

[0097] Subsequently, select transistors ST may be formed (S30). Global bit lines GBL may be formed, and the select transistors ST may
10 be formed above the global bit lines GBL.

[0098] Subsequently, memory cells MC may be formed (S40). Word lines WL stacked above the select transistors ST and local bit lines LBL penetrating through the word lines WL may be formed. The memory cells MC may be connected between the word lines WL and the local
15 bit lines LBL. The select transistors ST may be connected between the local bit lines LBL and the global bit lines GBL.

[0099] Subsequently, a second interconnection structure IC2 may be formed (S50). The second interconnection structure IC2 may be electrically connected to the select line SL, the word line WL, the first
20 interconnection structure IC1, and the like. The second interconnection structure IC2 may include a wiring line, a via, and the like.

[00100] In the present embodiment, a configuration where the peripheral circuit and a cell array are sequentially formed on the

substrate has been described, but the present disclosure is not limited thereto. It is also possible to separately manufacture a peripheral circuit chip including the peripheral circuit and a cell chip including the cell array, and then bond the peripheral circuit chip and the cell chip together.

[00101] FIGS. 14A to 14F illustrate a manufacturing method of a semiconductor device in accordance with an embodiment, and are cross-sectional views of a cell region CELL. Hereinafter, the content overlapping with the previously described content may be omitted.

10 **[00102]** Referring to FIG. 14A, a stack ST1 is formed. The stack ST1 may be formed above select transistors ST. A global bit line GBL, a select line SL, the select transistor ST, and an interlayer insulating layer IL may have structures according to the embodiment described above with reference to FIGS. 1A to 1C, and may be formed by the
15 manufacturing method according to the embodiment described above with reference to FIGS. 3A, 4A, 5A, 6A, 7A, 8A, 9A, and 10A, FIGS. 3B, 4B, 5B, 6B, 7B, 8B, 9B, and 10B, and FIGS. 3C, 4C, 5C, 6C, and 7C.

[00103] The stack ST1 may include first material layers 41 and second
20 material layers 42 that are alternately stacked in the third direction III. The first material layers 41 may be used to form word lines, and the second material layers 42 may be used to insulate the stacked word lines from each other. The first material layers 41 may each include a material having a high etching selectivity with respect to the second

material layers 42. For example, the first material layers 41 may each include a sacrificial material, such as nitride, and the second material layers 42 may each include an insulating material, such as oxide. The first material layers 41 may each include a conductive material such as polysilicon, tungsten, molybdenum, or the like.

[00104] Subsequently, openings OP are formed through the stack ST1. The openings OP may penetrate through the stack ST1, and may expose an upper surface of the interlayer insulating layer IL. The openings OP may be located to correspond to the select transistors ST and align with channel pillars of the select transistors ST. For example, in a plan view, the openings OP may be arranged in the first direction I and the second direction II, and an interval between the openings OP in the first direction I may be smaller than an interval between the openings OP in the second direction II.

[00105] Referring to FIG. 14B, recess regions are formed by etching the first material layers 41 exposed through the openings OP. The recess regions expand the openings OP in a horizontal direction at levels corresponding to the first material layers 41. Subsequently, a first electrode layer 43 may be formed along a surface of the stack ST1 exposed by the expanded openings OP. The first electrode layer 43 may be formed at a thickness sufficient to fill the recess regions.

[00106] Referring to FIG. 14C, first electrodes 43A are formed by etching the first electrode layer 43. The first electrodes 43A may be located in the recess regions, respectively. Subsequently, a variable

resistance material 44 is deposited along surfaces of the stack ST1 and the first electrodes 43A exposed through the openings OP. The variable resistance material 44 may be formed at a thickness sufficient to fill the recess regions.

5 **[00107]** Referring to FIG. 14D, variable resistance layers 44A are formed by etching the variable resistance material 44. The variable resistance layers 44A may be located in the recessed regions, respectively. Subsequently, a second electrode layer 45 is formed along surfaces of the stack ST1 and the variable resistance layers 44A
10 exposed through the openings OP.

[00108] Referring to FIG. 14E, a portion of the second electrode layer 45 formed on the upper surface of the interlayer insulating layer IL may be etched. Subsequently, the openings OP may be expanded downward by etching the interlayer insulating layer IL, thereby
15 exposing the channel pillars of the select transistors ST. Subsequently, a conductive layer 46 is formed on the second electrode layer 45. The conductive layer 46 may be formed along surfaces of the second electrode layer 45 and the interlayer insulating layer IL, filling the openings OP. The conductive layer 46 may include
20 a metal, such as tungsten.

[00109] Referring to FIG. 14F, the conductive layer 46 and the second electrode layer 45 may be etched. A second electrode 45A and local bit lines 46A may be formed by planarizing the conductive layer 46 and the second electrode layer 45 until an upper surface of the stack

ST1 is exposed. The planarization process may be performed by a chemical mechanical polish (CMP) method.

[00110] Each local bit line 46A may have a pillar shape, and the second electrode 45A may surround a sidewall of the local bit line 46A. The variable resistance layers 44A and the first electrodes 43A may surround the second electrode 45A. The variable resistance layers 44A and the first electrodes 43A may be located between the second material layers 42 stacked in the third direction III, and may each have a ring shape. The local bit lines 46A may extend through the stack ST1 in the third direction III, and may be connected to the channel pillars of the select transistors ST, respectively.

[00111] According to the manufacturing method described above, memory cells MC stacked along the local bit lines 46A may be formed. Each memory cell MC may include the first electrode 43A, the variable resistance layer 44A, and the second electrode 45A. The memory cells MC sharing the same local bit line 46A may constitute one memory unit MU.

[00112] FIGS. 15A, 16A, and 17A and FIGS. 15B, 16B, and 17B illustrate a manufacturing method of a semiconductor device in accordance with an embodiment, and illustrate a select line decoder region, a cell region, and a word line decoder region. FIGS. 15A, 16A, and 17A illustrate layouts, and FIGS. 15B, 16B, and 17B are cross-sectional views taken along lines F-F' of FIGS. 15A, 16A, and 17A, respectively. Hereinafter, the content overlapping with the previously

described content may be omitted.

[00113] Referring to FIGS. 15A and 15B, a global bit line GBL, a select line SL, a select transistor ST, an interlayer insulating layer IL, and a contact plug CT are formed. The global bit line GBL, the select line SL, the select transistor ST, the interlayer insulating layer IL, and the contact plug CT may have structures according to the embodiment described above with reference to FIGS. 1A to 1C, and may be formed by the manufacturing method according to the embodiment described above with reference to FIGS. 3A, 4A, 5A, 6A, 7A, 8A, 9A, and 10A, FIGS. 3B, 4B, 5B, 6B, 7B, 8B, 9B, and 10B, and FIGS. 3C, 4C, 5C, 6C, and 7C.

[00114] A stack ST1 and memory units MU are formed. In the stack ST1, first material layers 51 and second material layers 52 are alternately stacked in the third direction III. The stack ST1 may be formed in a select line decoder region SD, a cell region CELL, and a word line decoder region WLD. The memory units MU may be located to correspond to select transistors ST, and may have an interval W3 in the first direction I smaller than an interval W4 in the second direction II. The stack ST1 and the memory units MU may have structures according to the embodiment described above with reference to FIGS. 11A and 11B, and may be formed by the manufacturing method according to the embodiment described above with reference to FIGS. 14A to 14F.

[00115] Subsequently, the word line decoder region WLD of the stack

ST1 may be patterned to have a staircase structure. Each of the first material layers 51 may be exposed through the staircase structure. Subsequently, an interlayer insulating layer ILD may be formed on the stack ST1.

5 **[00116]** Referring to FIGS. 16A and 16B, a slit SLI penetrating through the stack ST1 is formed. The first material layers 51 may be exposed through the slit SLI. For example, the slit SLI may be formed in the select line decoder region SD of the stack ST1. For reference, although not illustrated in FIGS. 16A and 16B, the slit SLI may also be
10 formed in the cell region CELL and/or the word line decoder region WLD.

[00117] Subsequently, the first material layers 51 may be replaced with third material layers 53 through the slit SLI. For example, recess regions may be formed by removing the first material layers 51,
15 and the third material layers 53 may be formed in the recess regions. The third material layers 53 are used to form word lines, and may each include a metal such as tungsten or molybdenum. Through this, a word line stack WLST including the second material layers 52 and the third material layers 53 that are alternately stacked may be
20 formed. Subsequently, a gap-fill insulating layer GFI may be formed in the slit SLI.

[00118] For reference, when the first material layers 51 each include a conductive material, a process of replacing the first material layers 51 with the third material layers 53 may be omitted. In such a case, the

first material layers 51 may be used as the word lines, and the stack ST1 may be used as the word line stack WLST.

[00119] Referring to FIGS. 17A and 17B, word line contact plugs WLCT are formed. The word line contact plugs WLCT may be located in the word line decoder region WLD. The word line contact plugs WLCT may penetrate through the interlayer insulating layer ILD, and may be connected to the third material layers 53, respectively.

[00120] While forming the word line contact plugs WLCT, select line contact plugs SLCT may also be formed. The select line contact plugs SLCT may be located in the select line decoder region SD. The select line contact plugs SLCT may penetrate through the gap-fill insulating layer GFI, and may be connected to the contact plugs CT, respectively.

[00121] According to the manufacturing method described above, the word line contact plugs WLCT respectively connected to the word lines and the select line contact plugs SLCT respectively connected to the select lines SL may be formed.

[00122] FIG. 18 is a cross-sectional view illustrating a semiconductor device in accordance with an embodiment. Hereinafter, the content overlapping with the previously described content may be omitted.

[00123] Referring to FIG. 18, the semiconductor device may include a first semiconductor structure S1, a second semiconductor structure S2, and a bonding structure BS located between the first semiconductor structure S1 and the second semiconductor structure S2. The first semiconductor structure S1 and the second semiconductor structure

S2 may be formed by separate processes, and may be electrically connected to each other by the bonding structure BS. For example, the first semiconductor structure S1 may include a peripheral circuit PC, and the second semiconductor structure S2 may include a
5 memory cell array CA.

[00124] The first semiconductor structure S1 may include a substrate 100, a transistor TR, a first interconnection structure IC1, and a first interlayer insulating layer IL1. An active region may be defined by an element isolation layer 104 formed in the substrate 100, and the
10 transistor TR may be located in the active region. The transistor TR may include a gate insulating layer 101, a gate electrode 102, and a junction 103. The transistor TR may belong to the peripheral circuit PC.

[00125] The first interconnection structure IC1 may be located in the
15 first interlayer insulating layer IL1, and may include a via 105, a wiring line 106, and the like. The first interconnection structure IC1 may be electrically connected to the peripheral circuit PC, and may be electrically connected to the transistor TR.

[00126] The second semiconductor structure S2 may include global bit
20 lines GBL, select lines SL, select transistors ST, word lines WL, memory units MU, contact plugs CT, select line contact plugs SLCT, word line contact plugs WLCT, a second interconnection structure IC2, and a second interlayer insulating layer IL2. The word lines WL may be stacked in a staircase shape or stacked in an inverted staircase

shape. The select lines SL may be located above or below the word lines WL. The select transistors ST may be located above or below the memory units MU.

[00127] The second interconnection structure IC2 may be located in the second interlayer insulating layer IL2 and may include a via 207, a wiring line 208, and the like. The second interconnection structure IC2 may be electrically connected to the global bit lines GBL, the select lines SL, the word lines WL, and the like.

[00128] The bonding structure BS may include a first bonding layer BL1, a second bonding layer BL2, a first bonding pad BP1, and a second bonding pad BP2. The first bonding layer BL1 and the second bonding layer BL2 may be in contact with each other, and the first bonding pad BP1 and the second bonding pad BP2 may be in contact with each other. The first bonding layer BL1 and the second bonding layer BL2 may each include SiCN, tetra ethyl ortho silicate (TEOS), or the like. The first bonding pad BP1 may be electrically connected to the first interconnection structure IC1, and the second bonding pad BP2 may be electrically connected to the second interconnection structure IC2. The memory cell array CA and the peripheral circuit PC may be electrically connected to each other through the first bonding pad BP1 and the second bonding pad BP2.

[00129] The structure and the manufacturing method according to the above-described embodiments may be applied to semiconductor devices with various configurations. FIGS. 19 and 20 illustrate

schematic configurations of semiconductor devices to which the above-described embodiments are applicable.

[00130] FIG. 19 is a configuration diagram of a semiconductor device according to an embodiment of the present disclosure.

5 **[00131]** Referring to FIG. 19, the semiconductor device may include a substrate SUB, a peripheral circuit PC, and a memory cell array CA. Here, the peripheral circuit PC and the memory cell array CA may be formed on the same substrate.

[00132] The substrate SUB may be made of or include a semiconductor material. In an embodiment, the semiconductor material may include at least one of a group IV semiconductor, a group III-V compound semiconductor, and a group II-VI compound semiconductor. Here, the group IV semiconductor may include single crystal silicon (Si), polycrystalline silicon, germanium (Ge), or silicon germanium (SiGe). The group III-V compound semiconductor may include GaAs, GaN, GaP, GaAsP, GaInAsP, AlAs, AlGa, InP, InSb, or InGaAs. The group II-VI compound semiconductor may include ZnS, ZnO, or CdS.

[00133] The substrate SUB may include a dielectric layer. The substrate SUB may be a silicon-on-insulator (SOI) substrate, a germanium-on-insulator (GeOI) substrate, or a glass substrate. The substrate SUB may include an organic material. In an embodiment, the substrate SUB may include graphene.

[00134] The substrate SUB may be a bulk wafer or an epitaxial layer grown using a selective epitaxial growth (SEG) method. Alternatively, the substrate SUB may be formed using a metal induced lateral crystallization (MILC) method and may partially include metal. The
5 substrate SUB may have a single crystalline, polycrystalline, or amorphous state. The substrate SUB may include an impurity of group II, group III, group IV, group V, or group VI. In an embodiment, the substrate SUB may include an n-well region doped with an n-type impurity and/or a p-well region doped with a p-type
10 impurity.

[00135] The peripheral circuit PC may be disposed between the substrate SUB and the memory cell array CA. The peripheral circuit PC may include one or more of a row decoder, a column decoder, a page buffer, a logic circuit, a control circuit, a sense amplifier, an
15 input/output circuit, and the like. In an embodiment, the peripheral circuit PC may include an NMOS transistor, a PMOS transistor, a resistor, a capacitor, and the like. The peripheral circuit PC may further include an interconnection structure. The interconnection structure may serve as a path for transferring an operating voltage,
20 and may include components such as a contact plug, a line, and the like.

[00136] The memory cell array CA may include memory cells. In an embodiment, the memory cell array CA may include memory strings

connected between a source line and a bit line, and each memory string may include stacked memory cells. In an embodiment, the memory cell array CA may include memory cells, each connected between a word line and a bit line. The memory cell array CA may
5 further include an interconnection structure.

[00137] FIG. 20 is a configuration diagram of a semiconductor device according to an embodiment of the present disclosure.

[00138] Referring to FIG. 20, the semiconductor device may include a substrate SUB, a peripheral circuit PC, a bonding structure BS, and a
10 memory cell array CA. Here, the peripheral circuit PC and the memory cell array CA may be respectively formed on separate substrates and then bonded. The semiconductor device may further include a support base SP_B.

[00139] The substrate SUB may serve as a support in a process of
15 forming the peripheral circuit PC. The support base SP_B may serve as a support in a process of forming the memory cell array CA. In an embodiment, a first wafer including the memory cell array CA and a second wafer including the peripheral circuit PC are separately manufactured and then electrically connected via the bonding
20 structure BS. After bonding, at least a portion of the support base SP_B of the first wafer may be removed. The support base SP_B may either be completely removed or partially remain on the memory cell array CA.

[00140] The support base SP_B may be a semiconductor substrate, an insulating substrate, a silicon-on-insulator (SOI) substrate, a germanium-on-insulator (GeOI) substrate, or the like. The support base SP_B may be a bulk wafer, an epitaxial layer grown using a selective epitaxial growth (SEG) method, or a layer formed using a metal induced lateral crystallization (MILC) method. The support base SP_B may have a single crystalline, polycrystalline, or amorphous state. The support base SP_B may include an impurity of group II, group III, group IV, group V, or group VI.

[00141] The bonding structure BS may connect the memory cell array CA to the peripheral circuit PC. In an embodiment, the memory cell array CA and the peripheral circuit PC may be bonded using a method such as a wafer-on-wafer bonding method, a chip-on-wafer bonding method, a chip-on-chip bonding method, or the like. The bonding structure BS may include one or more of components such as a bonding pad, a bonding layer, a bonding interface, and the like. The bonding pad may include a metal such as copper and aluminum, or their alloys. The bonding interface may be a non-metal-to-non-metal interface, a metal-to-metal interface, or the like. The bonding structure BS facilitates the electrical connection between the memory cell array CA and the peripheral circuit PC.

[00142] For reference, the interconnection structures included in the memory cell array CA and/or the peripheral circuit PC may be directly

connected without the use of a bonding pad. In an embodiment, a bonding layer from the memory cell array CA and a bonding layer from the peripheral circuit PC may be bonded to form a bonding interface, enabling direct connection of the interconnection structures
5 from the memory cell array CA and the peripheral circuit PC. This allows contact plugs, lines, and similar elements formed on different wafers to be electrically connected without requiring a separate bonding pad.

[00143] Other configurations may be identical or similar to those
10 described above with reference to FIG. 19.

[00144] Meanwhile, the semiconductor device may feature a structure combining the embodiments described with reference to FIGS. 19 and 20 or a partially modified structure. In the embodiment described with reference to FIGS. 19 and 20, the positions of the memory cell
15 array CA and the peripheral circuit PC may be interchanged. Additionally, one or more memory cell arrays CA and/or peripheral circuits PC may be bonded to the configuration described in FIGS. 19 and 20. In an embodiment, a portion of the peripheral circuitry PC may be integrated in the memory cell array CA.

20 **[00145]** Although embodiments according to the technical idea of the present disclosure have been described above with reference to the accompanying drawings, this is only for explaining the embodiments according to the concept of the present disclosure, and the present

disclosure is not limited to the above embodiments. Various types of substitutions, modifications, changes, and combinations for the embodiments may be made by those skilled in the art, to which the present disclosure pertains, without departing from the technical idea
5 of the present disclosure defined in the following claims, and it should be construed that these substitutions, modifications, changes, and combinations belong to the scope of the present disclosure.

WHAT IS CLAIMED IS:

1. A semiconductor device, comprising:

channel pillars arranged along a first direction and a second
5 direction intersecting the first direction, wherein the channel pillars
are spaced apart by a first interval in the first direction and a second
interval in the second direction, the first interval being smaller than
the second interval;

a select line surrounding multiple channel pillars arranged in the
10 first direction and extending in the first direction;

word lines stacked above the select line in a third direction
perpendicular to the first and the second directions; and

local bit lines extending through the word lines in the third
direction and electrically connected to the channel pillars.

15

2. The semiconductor device of claim 1, further comprising
insulating pillars extending through the select lines in the third
direction.

20

3. The semiconductor device of claim 2, further comprising
a contact plug electrically connected to the select line, the contact
plug being positioned between two adjacent insulating pillars in the
first direction.

4. The semiconductor device of claim 3, wherein the select line includes first portions extending along the first direction and a second portion located between the two adjacent insulating pillars and connecting the first portions to each other, and the contact plug is connected to the second portion.

5. The semiconductor device of claim 1, wherein the plurality of channel pillars arranged in the first direction constitute one row, and the select line surrounds at least one row.

6. The semiconductor device of claim 5, wherein, when the select line surrounds at least two rows, the plurality of channel pillars surrounded by the select line are spaced apart by a third interval in the second direction, and the third interval is smaller than the second interval.

7. The semiconductor device of claim 6, wherein the multiple channel pillars surrounded by the select line are arranged in a zigzag pattern.

8. The semiconductor device of claim 1, further comprising global bit lines, each connected to channel pillars arranged in the second direction and extending in the second direction.

9. The semiconductor device of claim 8, further comprising select transistors located in regions where the select lines intersect the global bit lines, each select transistor being connected between a global bit line and a corresponding local bit line and including a
5 global bit line and a corresponding local bit line and including a corresponding one of the channel pillars.

10. The semiconductor device of claim 8, further comprising a global bit line decoder located below the global bit lines in the third
10 direction and connected to the global bit lines.

11. The semiconductor device of claim 1, further comprising a select line decoder located below the select lines in the third direction and connected to the select lines.

15

12. The semiconductor device of claim 1, further comprising a word line decoder located below the select lines in the third direction and connected to the word lines.

20 13. The semiconductor device of claim 1, wherein each of the channel pillars includes a first junction, a second junction, and a channel region located between the first junction and the second junction in the third direction.

14. The semiconductor device of claim 13, wherein the select line surrounds the channel region.

15. The semiconductor device of claim 13, wherein the first junction and the second junction each include P-type impurities, and the channel region is an intrinsic semiconductor or includes N-type impurities.

16. The semiconductor device of claim 13, wherein the first junction and the second junction each include N-type impurities, and the channel region is an intrinsic semiconductor or includes P-type impurities.

17. The semiconductor device of claim 1, further comprising:
a peripheral circuit located below the select lines in the third direction; and

a first interconnection structure located below the select lines and electrically connected to the peripheral circuit.

18. The semiconductor device of claim 1, further comprising a second interconnection structure located above the word lines in the third direction and electrically connected to the word lines.

19. A semiconductor device, comprising:

local lines arranged in a first direction and a second direction that intersects the first direction, and extending in a third direction perpendicular to the first and the second directions;

global lines extending in the second direction; and

5 select transistors connected between the local lines and the global lines, each select transistor including a corresponding one of channel pillars, the channel pillars being spaced apart by a first interval in the first direction and a second interval in the second direction, the first interval being different than the second interval.

10

20. The semiconductor device of claim 19, further comprising select lines connected to gate electrodes of the select transistors and extending in the first direction, wherein the first interval is smaller than the second interval.

15

21. The semiconductor device of claim 20, wherein multiple channel pillars arranged in the first direction constitute one row, and each of the select lines surrounds at least one row.

20

22. The semiconductor device of claim 21, wherein, when the select line surrounds at least two rows, the multiple channel pillars surrounded by the select line are spaced apart by a third interval in the second direction, and the third interval is smaller than the second interval.

23. The semiconductor device of claim 19, wherein the local lines are local bit lines, and the global lines are global bit lines.

5 24. The semiconductor device of claim 19, further comprising:
word lines surrounding the local lines and stacked in the third
direction; and
memory cells connected between the local lines and the word
lines.

10

25. The semiconductor device of claim 19, further comprising
a global line decoder located below the global lines in the third
direction and connected to the global lines.

15 26. The semiconductor device of claim 19, further comprising:
select lines connected to gate electrodes of the select transistors
and extending in the first direction; and
a select line decoder located below the global lines in the third
direction and connected to the select lines.

20

27. A method of manufacturing a semiconductor device, the
method comprising:
forming channel pillars arranged in a first direction and a second
direction that intersects the first direction;

forming a select line surrounding multiple channel pillars and extending in the first direction;

forming insulating pillars extending through the select line in a third direction perpendicular to the first and the second directions;

5 and

forming a contact plug electrically connected to the select line between two adjacent insulating pillars in the first direction.

28. The method of claim 27, wherein the channel pillars are
10 spaced apart by a first interval in the first direction and a second interval in the second direction, and the first interval is smaller than the second interval.

29. The method of claim 28, wherein channel pillars
15 arranged in the first direction constitute one row, and each of the select lines surrounds at least one row.

30. The method of claim 29, wherein, when the select line surrounds at least two rows, the multiple channel pillars surrounded
20 by the select line are spaced apart by a third interval in the second direction, and the third interval is smaller than the second interval.

31. The method of claim 27, further comprising forming global bit lines extending in the second direction.

32. The method of claim 27, wherein the forming of the channel pillars comprises:

forming a first conductive layer;

5 forming a semiconductor layer on the first conductive layer in the third direction;

forming semiconductor lines by etching the semiconductor layer, the semiconductor lines extending in the second direction;

forming global bit lines by etching the first conductive layer, the
10 global bit lines extending in the second direction; and

forming the channel pillars by patterning the semiconductor lines.

33. The method of claim 32, wherein the forming of the
15 semiconductor layer comprises:

forming a first semiconductor layer that is an N-type semiconductor layer;

forming a second semiconductor layer on the first semiconductor layer in the third direction, the second semiconductor
20 layer being a P-type semiconductor layer; and

forming a third semiconductor layer on the second semiconductor layer in the third direction, the third semiconductor layer being an N-type semiconductor layer.

34. The method of claim 27, wherein the forming of the select lines comprises:

forming gate insulating layers to surround sidewalls of the channel pillars;

5 forming a second conductive layer on the gate insulating layers so as to fill a space between channel pillars adjacent to each other in the first direction, and to leave an open space between channel pillars adjacent to each other in the second direction; and

forming the select lines by etching the second conductive layer,
10 the select lines extending in the first direction.

35. The method of claim 27, wherein the forming of the insulating pillars comprises:

forming first openings by removing some of the channel pillars;

15 and

forming the insulating pillars in the first openings.

36. The method of claim 27, wherein the forming of the contact plug comprises:

20 forming an interlayer insulating layer to cover the select lines;

forming a second opening extending through the interlayer insulating layer in the third direction, the second opening exposing a portion of the select line; and

forming the contact plug in the second opening.

37. The method of claim 36, wherein the select line includes first portions extending in the first direction and a second portion located between two adjacent channel pillars to connect the first portions to each other and extending in the second direction, and
5 the second opening exposes the second portion.

38. A method of manufacturing a semiconductor device, the method comprising:

10 forming global bit lines;

forming channel pillars over the global bit lines in a third direction, the channel pillars being arranged in a first direction and a second direction intersecting the first direction and spaced apart by an interval in the first direction smaller than an interval in the second direction, the third direction being perpendicular to both the first and
15 second directions;

forming select lines, each configured to surround multiple channel pillars in the first direction and extending in the first direction;

forming local bit lines on the select lines in the third direction,
20 the local bit lines being connected to the channel pillars, respectively, and extending in the third direction; and

forming word lines surrounding the local bit lines and stacked in the third direction.

39. The method of claim 38, further comprising forming select line contact plugs respectively connected to the select lines.

40. The method of claim 39, further comprising:
5 forming first openings by removing some of the channel pillars;
and
forming insulating pillars in the first openings.

41. The method of claim 40, wherein the select line contact
10 plugs are connected to portions of the select lines, each portion being positioned between two adjacent insulating pillars.

42. The method of claim 38, further comprising forming word line contact plugs respectively connected to the word lines.