

Description

ZERO POWER POWER-ON-RESET CIRCUIT

5 TECHNICAL FIELD

The present invention relates to power-on reset circuits and more specifically to power-on reset circuits used in semiconductor devices.

10 BACKGROUND ART

When power (V_{cc}) is applied to a semiconductor device, the various components comprising the device receive power in an essentially random fashion. One potential outcome is an indeterminate state when V_{cc} reaches a steady-state level. Similarly, some components such as flip-flops require a settling time for the components to reach a steady operating condition. Thus a circuit, referred to as a power-on reset (POR) circuit, is employed to ensure that the components of a semiconductor device remain in a reset state until a stable V_{cc} is attained. The POR holds the device components in reset with a reset signal which is removed when steady state conditions are attained.

With increasing use of laptop computers, personal digital devices such as PDAs, cell phones and so on, there is an increased awareness to maintaining a low power consumption. A prime area of consideration is the design of POR circuits. Such circuits come into play only during the power-on cycle, and ideally become inactive and consume no power afterward. It is thus desirable to have a POR circuit that is capable of turning itself off in order to conserve power during its inactive (or steady state) condition.

35 SUMMARY OF THE INVENTION

A power-on reset circuit comprises a first charging means coupled between a power supply terminal and a node A. The potential at node A drives a first circuit consisting of first and second series coupled transistors, having an output which follows the potential

-2-

at node A. The output is coupled to a second circuit consisting of third and fourth transistors, having an output which charges a capacitor coupled between the input of the inverter and ground, thus completing a feedback circuit to node A. The second circuit responds to the output of the first circuit by delaying for a period of time before actually charging the capacitor.

In a preferred embodiment, the charging means is a capacitor coupled between the power supply terminal and node A. The transistors of the first circuit are N-channel zero threshold devices. The transistors in the second circuit include a P-channel device and an N-channel device, the N-channel device also being a zero threshold voltage device.

BRIEF DESCRIPTION OF THE DRAWING

The Figure shows a schematic diagram of the POR circuit of the present invention.

BEST MODE OF CARRYING OUT THE INVENTION

With reference to the Figure, the power-on reset circuit 100 of the present invention comprises two outputs POR and $\overline{\text{POR}}$, respectively providing a reset signal and an active low reset signal at the front end of circuit 100. The POR signal is driven by inverters 106 and 102, and the $\overline{\text{POR}}$ signal is driven by inverter 104 which simply inverts the output of inverter 102. The width-to-length (W/L) ratios of the transistors comprising each inverter are given. The top ratio specifies the device dimensions for the P-channel device, while the bottom ratio specifies the dimensions for the N-channel device. This is exemplified in the Figure by the internal representation of inverter 130, showing the transistors and their corresponding W/L ratios. In addition to the inverters, the W/L ratios of the transistors comprising the circuit are also shown in the Figure.

The back end of the power-on reset circuit includes a voltage detection stage 162 comprising

-3-

N-channel transistor 150 having a source-drain coupling between a power rail 110 and a node B. N-channel transistor 152 has a similar source-drain coupling between node B and ground. Each N-channel transistor
5 150, 152 is a zero threshold voltage ($V_t = 0$ V) device.

Moving forward, node B is coupled to the gates of transistors 140 and 142 which constitute charging circuit 164. Transistor 140 is a P-channel device having a source coupled to power rail 110 and a drain coupled to
10 the drain of an N-channel, zero threshold voltage transistor 142. The source of transistor 142 is coupled to ground.

Continuing forward, the drain-drain connection node C of the 140/142 transistor pair is coupled to the
15 input to inverter 130. Node C is also coupled to ground via capacitor 122. The output of inverter 130 is coupled to node A which in turn is coupled to power rail 110 via capacitor 120. A feedback path 160 is provided from node A to drive the gates of transistors 150 and 152.

20 In operation, when power is initially applied to the circuit, power rail 110 begins ramping up from zero volts. The voltage V_A at node A follows the voltage $V_{\text{power rail}}$ at power rail 110 as capacitor 120 begins to charge. As V_A increases above 0 V, transistors 150, 152
25 begin to turn on. Since the gate of transistor 152 is coupled to node A, it immediately begins to conduct, recalling that transistor 152 has a source coupled to ground and $V_t = 0$ V, and will continue to do so during the power-up sequence since the condition $V_A \geq 0$ V holds
30 during power-up. This has the effect of lowering the potential V_B of node B to ground potential. Consequently, transistor 150 begins to turn on, since its V_{gs} too is greater than $V_t = 0$ V. This tends to drive V_B from ground potential to $V_{\text{power rail}}$. However, the gate-source
35 capacitance of transistor 142 is large; observe in the Figure that the W/L ratio for transistor 142 is 3.1/117. This has the effect of delaying the rise of V_B and, as a result, V_B will lag behind $V_{\text{power rail}}$.

-4-

Continuing with the next stage, if V_B lags behind $V_{\text{power rail}}$ by a sufficient amount, P-channel transistor 140 will begin to turn on, thus allowing a charge to accumulate on capacitor 122. As V_B continues to rise, transistor 142 begins to turn on, since its $V_t = 0$ V and V_B is positive. This will tend to slow the charge time of capacitor 122 as the charge flowing from transistor 140 is divided between capacitor 122 and transistor 142. As the capacitor charges, the voltage V_C at node C begins to rise. V_C continues to rise until it reaches the trip point of inverter 130, namely the threshold voltage of the N-channel device comprising the inverter. When that happens node A is coupled to ground via the N-channel device of inverter 130, thus taking the voltage V_A at node A to ground.

As a consequence, the gate potential of transistors 150, 152 go to ground because of the feedback path 160 from node A to the gates of the transistors. Since V_B is positive at this point, the effect of grounding the gate of transistor 150 is to turn the transistor off, since its V_{gs} becomes less than the transistor's threshold voltage. However, transistor 152 remains on, since $V_{gs} = 0$ V and its V_t is 0 V. This combination of circumstances tends to drive V_B to ground potential. Though V_B goes to ground, transistor 150 remains off even though the gate potential is at 0 V and V_B is at 0 V. Any tendency for transistor 150 to turn on will drive V_B above the transistor's gate potential, which remains at 0 V by virtue of the feedback path 160 to node A, and thus turn itself off (recall that $V_t = 0$ V). V_B is driven back to ground through transistor 152 and in this way, V_B is maintained at ground potential.

P-channel transistor 140 remains turned on since $V_{gs} = V_B - V_{\text{power rail}}$, which at this point is less than the transistor's V_t . Capacitor 122 maintains its charge via transistor 140, thus maintaining a HI at the input of inverter 130 and producing a constant LO (i.e. ground) at its output. Thus node A remains grounded. Consequently,

-5-

transistors 150, 152 are maintained in their current state (via feedback path 160); i.e. transistor 152 is turned on (because $V_{gs} = V_t = 0$ V) and transistor 150 remains off since any tendency for the transistor to turn on will be counteracted by the rising of V_g above its gate potential. With V_g maintained at ground potential, transistor 140 remains on and transistor 142 is off. This condition presents a logic HI to inverter 130 which outputs a LO, thus holding node A to ground.

Thus, in the steady state condition, it can be seen that there are no power burning stages. Transistor 152 remains on to hold node B at ground potential, and since transistor 150 is off there is no current flow from the power supply through transistor 152. Transistor 140 serves to provide a logic HI to inverter 130, thus maintaining a LO at node A, which is fed back to transistor 152 and so on, maintaining the steady state condition. Capacitor 120 and capacitor 122 maintains its charged state since there is no discharge path and so does not dissipate energy in the steady state condition.

As noted above, the triggering of inverter 130 drives node A to ground thus putting the circuit into a zero power-consuming steady-state condition. There are two factors which affect the triggering of inverter 130. First, is the charge build up of capacitor 122. It is the charging of the capacitor which brings V_c up to a positive voltage. The charge time of capacitor 122 can be adjusted so that the trip point of inverter 130 is not reached until the power reaches the desired voltage level V_{cc} . As shown in the Figure, a value of 2.2226 pF for capacitor 122 was shown to exhibit the desired effect.

The second factor is the sizing of N-channel transistor 142. The high ground-source capacitance resulting from the large gate area of the transistor (W/L is 3.1/117) permits V_g to lag behind $V_{\text{power rail}}$. Moreover, V_g must be at a potential sufficiently lower than $V_{\text{power rail}}$ so that V_{gs} of P-channel transistor 140 becomes less than its threshold voltage, allowing transistor 140 to turn on

-6-

to charge capacitor 122. Using known simulation and design techniques, it was determined that a W/L ratio of 3.1/117 was adequate.

-7-

Claims

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1. A power-on reset circuit comprising:
charging means (120) for outputting a voltage
5 level in response to a rising power supply voltage;
first means (130), electrically coupled to the
charging means, for providing a ground potential in
response to a trigger signal, the first means adapted to
hold the voltage level of the charging means at ground
10 potential when triggered; and
second means (162, 164, 122), electrically
coupled to the first means, for providing a trigger
signal in response to a rising voltage level at the
charging means (120), the second means adapted to trigger
15 the first means;
a feedback path coupling the charging means
(120) to the second means (122).
- 20 2. The reset circuit of claim 1 wherein the charging
means is a first capacitor (120) coupled between the
power supply voltage and a first node (A), thereby
producing a rising voltage level as a power supply begins
to increase in voltage.
- 25 3. The reset circuit of claim 2 wherein the first means
is an inverter (130) having an input to receive the
trigger signal and having an output coupled to the first
30 node (A).
4. The reset circuit of claim 3 wherein the second
means includes a second capacitor (122) coupled between
35 the inverter input and ground, the trigger signal being a
first voltage potential across the second capacitor.





5. The reset circuit of claim 4 wherein the second means further includes a circuit (164) for charging the second capacitor (122) to a level equal to the first voltage potential, in response to the rising voltage level of the charging means.

6. The reset circuit of claim 3 wherein the second means includes:

a second capacitor (122) coupled between the inverter input and ground;

a P-channel (140) device coupled in series with an N-channel device (142) at a second node (C), the second node being coupled to the second capacitor to be charged thereby; and

a pair of zero voltage threshold transistors (150, 152) coupled at a third node (B), the third node being coupled to the gates of the P-channel and the N-channel devices;

the feedback path (160) coupling the first node to the gate of each of the zero voltage threshold transistors.

7. The reset circuit of claim 6 wherein the N-channel device (142) is a zero threshold voltage device.

8. A power-on reset circuit comprising:

first means (120) for raising the potential at a node A as a power supply voltage increases;

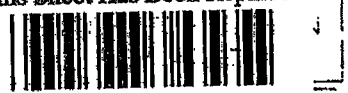
second means (150, 152), electrically coupled to node A, for raising the potential at a second node B in response to a rising potential at node A;

third means (140), electrically coupled to node B, for raising the potential at a third node C in response to a rising potential at node B, the third means having means for delaying the onset of raising the potential at node C; and



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-9-



fourth means (130) for holding the potential at node A to ground in response to node C reaching a first voltage level, the fourth means having an input electrically coupled to node C to receive the potential at node C, the fourth means further having an output electrically coupled to node A.

9. The reset circuit of claim 8 further including an inverter (106) having an input coupled to node A, an output of the inverter providing a reset signal.

10. The reset circuit of claim 8 wherein the fourth means is an inverter (130) and the first voltage level is the trip point of the inverter.

11. The reset circuit of claim 8 further including a power supply terminal and a ground terminal, wherein the first means is a first capacitor (120) coupled between the power supply and ground terminals.

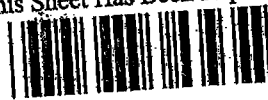
12. The reset circuit of claim 11 wherein the second means includes first and second series-coupled, N-channel transistors (150, 152), coupled at node B, gates of the transistors coupled to node A.

13. The reset circuit of claim 12 wherein the N-channel transistors are zero threshold voltage devices.

14. The reset circuit of claim 12 wherein the third means is a P-channel transistor (140) having source and drain terminals coupled between the power supply terminal and node C, and having a gate coupled to node B.



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15. The reset circuit of claim 14 wherein the means for delaying is an N-channel, zero threshold voltage device (140) having drain and source terminals coupled between node C and ground, and having a gate coupled to node B.

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16. The reset circuit of claim 15 wherein the third means further includes a second capacitor (122) coupled between node C and ground.

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17. The reset circuit of claim 14 wherein the first and second N-channel transistors (150, 152) are zero threshold voltage devices.

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18. A power-on reset circuit comprising:

a first terminal (110) for connection to a first potential;

20 a second terminal for connection to a second potential;

a first capacitor (120) coupled between the first terminal and a first node (A);

25 an inverter (130) having an input and an output, the output coupled to the first node;

a second capacitor (122) coupled between the input of the inverter and the second terminal;

30 first means (162), electrically coupled to the first node (110), for outputting a voltage level that follows the potential of the first node; and

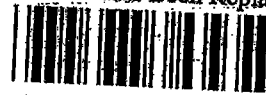
second means (164) for charging the second capacitor (122), the second means having an input coupled to receive the output voltage of the first means, the second means further having an output coupled to the second capacitor.

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-11-



19. The reset circuit of claim 18 wherein the second means includes means for delaying the onset of the charging of the second capacitor.

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20. The reset circuit of claim 18 wherein the first means includes a pair of series connected transistors (150, 152) coupled between the first and second terminals, a gate of each of the transistors being coupled to the first node (110).

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21. The reset circuit of claim 20 wherein each of the transistors is an N-channel device having a zero threshold voltage.

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22. The reset circuit of claim 20 wherein the pair of transistors (150, 152) is coupled at a second node (B); the second means includes a P-channel transistor and an N-channel transistor coupled in series between the first and second terminals, a gate of each being coupled to the second node; and a source of the P-channel transistor and a drain of the N-channel transistor are coupled to charge the second capacitor.

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23. The reset circuit of claim 18 wherein the first terminal is a power supply rail and the second terminal is a ground rail.

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24. A power-on reset circuit comprising:

a power connection (110);

a ground connection;

an output node A;

a first capacitor (120) coupled between the power node and the output node;

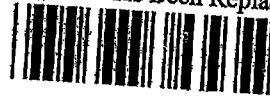
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-12-



first and second transistors (150, 152) coupled in series between the power connection and the ground connection, the first and second transistors coupled together at a node B;

5 third and fourth transistors (140, 142) coupled in series between the power connection and the ground connection, the third and fourth transistors coupled together at a node C, the third and fourth transistors each having a gate coupled to node B;

10 a second capacitor (122) coupled between node C and the ground connection;

a first inverter (130) having an input coupled to node B and an output coupled to node A; and

15 a feedback path (160) coupling the output node to gate terminals of the first and second transistors.

25. The reset circuit of claim 24 wherein the first and second transistors (150, 152) are zero threshold voltage
20 N-channel devices.

26. The reset circuit of claim 24 wherein the third transistor (140) is a P-channel device and the fourth
25 transistor (142) is a zero threshold voltage N-channel device.

27. The reset circuit of claim 24 wherein the first and
30 second transistors are zero threshold voltage N-channel devices, the third transistor is a P-channel device, and the fourth transistor is a zero threshold voltage N-channel device.

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-13-



28. The reset circuit of claim 27 further including a second inverter (106) having an input coupled to the output node, whereby the output node serves as a reset signal and an output of the second inverter serves as a complement of the reset signal.

29. The reset circuit of claim 28 further including a third inverter (102) having an input coupled to the output of the second inverter (106), and a fourth inverter (104) coupled to an output of the third inverter, whereby the output of the third inverter serves as the reset signal and an output of the fourth inverter serves as a complement of the reset signal.



AMENDED CLAIMS

[received by the International Bureau on 10 February 1999 (10.02.99);
original claims 12 and 20 cancelled; original claims 1, 6, 8, 13, 14, 18,
21 and 24 amended; remaining claims unchanged (7 pages)]

1. A power-on reset circuit comprising:

charging means (120) for outputting a voltage
5 level in response to a rising power supply voltage;

first means (130), electrically coupled to the
charging means, for providing a ground potential in
response to a trigger signal, the first means adapted to
hold the voltage level of the charging means at ground
10 potential when triggered; and

second means (162, 164, 122), electrically
coupled to the first means, for providing a trigger
signal in response to a rising voltage level at the
charging means, the second means adapted to trigger the
15 first means, the second means including a pair of series-
coupled zero voltage threshold transistors (150, 152);

a feedback path coupling the charging means
(120) to the pair of zero voltage threshold transistors
(122).

2. The reset circuit of claim 1 wherein the charging
means is a first capacitor (120) coupled between the
power supply voltage and a first node (A), thereby
25 producing a rising voltage level as a power supply begins
to increase in voltage.

3. The reset circuit of claim 2 wherein the first means
30 is an inverter (130) having an input to receive the
trigger signal and having an output coupled to the first
node (A).

35 4. The reset circuit of claim 3 wherein the second
means includes a second capacitor (122) coupled between
the inverter input and ground, the trigger signal being a
first voltage potential across the second capacitor.





5. The reset circuit of claim 4 wherein the second means further includes a circuit (164) for charging the second capacitor (122) to a level equal to the first voltage potential, in response to the rising voltage level of the charging means.

6. The reset circuit of claim 3 wherein the second means further includes:

a second capacitor (122) coupled between the inverter input and ground; and

a P-channel device (140) coupled in series with an N-channel device (142) at a second node (C), the second node being coupled to the second capacitor to be charged thereby;

the pair of zero voltage threshold transistors (150, 152) coupled at a third node, the third (B) node being coupled to the gates of the P-channel and the N-channel devices;

the feedback path (160) coupling the first node to the gate of each of the zero voltage threshold transistors.

7. The reset circuit of claim 6 wherein the N-channel device (142) is a zero threshold voltage device.

8. A power-on reset circuit comprising:

first means for raising the potential at a node A as a power supply voltage increases;

second means (150, 152), electrically coupled to node A, for raising the potential at a second node B in response to a rising potential at node A, the second means including first and second series-coupled, N-channel transistors, coupled at node B, gates of the N-channel transistors coupled to node A;

third means (140), electrically coupled to node B, for raising the potential at a third node C in response to a rising potential at node B, the third means





having means for delaying the onset of raising the potential at node C; and

fourth means (130) for holding the potential at node A to ground in response to node C reaching a first voltage level, the fourth means having an input electrically coupled to node C to receive the potential at node C, the fourth means further having an output electrically coupled to node A.

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9. The reset circuit of claim 8 further including an inverter (106) having an input coupled to node A, an output of the inverter providing a reset signal.

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10. The reset circuit of claim 8 wherein the fourth means is an inverter (130) and the first voltage level is the trip point of the inverter.

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11. The reset circuit of claim 8 further including a power supply terminal and a ground terminal, wherein the first means is a first capacitor (120) coupled between the power supply and ground terminals.

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12. [Cancelled]

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13. The reset circuit of claim 8 wherein the N-channel transistors are zero threshold voltage devices.

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14. The reset circuit of claim 8 wherein the third means is a P-channel transistor having source and drain terminals coupled between the power supply terminal and node C, and having a gate coupled to node B.



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15. The reset circuit of claim 14 wherein the means for delaying is an N-channel, zero threshold voltage device (140) having drain and source terminals coupled between node C and ground, and having a gate coupled to node B.

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16. The reset circuit of claim 15 wherein the third means further includes a second capacitor (122) coupled between node C and ground.

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17. The reset circuit of claim 14 wherein the first and second N-channel transistors (150, 152) are zero threshold voltage devices.

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18. A power-on reset circuit comprising:

a first terminal (110) for connection to a first potential;

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a second terminal for connection to a second potential;

a first capacitor (120) coupled between the first terminal and a first node;

an inverter (130) having an input and an output, the output coupled to the first node;

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a second capacitor (122) coupled between the input of the inverter and the second terminal;

first means (162), electrically coupled to the first node (110), for outputting a voltage level that follows the potential of the first node, the first means including a pair of series-connected N-channel transistors coupled between the first and second terminals, a gate of each of the transistors being coupled to the first node; and

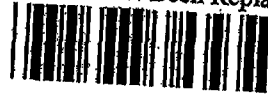
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second means (164) for charging the second capacitor (122), the second means having an input coupled to receive the output voltage of the first means, the second means further having an output coupled to the second capacitor.



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19. The reset circuit of claim 18 wherein the second means includes means for delaying the onset of the charging of the second capacitor.

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20. [Cancelled]

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21. The reset circuit of claim 18 wherein each of the transistors has a zero threshold voltage.

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22. The reset circuit of claim 20 wherein the pair of transistors (150, 152) is coupled at a second node (B); the second means includes a P-channel transistor and an N-channel transistor coupled in series between the first and second terminals, a gate of each being coupled to the second node; and a source of the P-channel transistor and a drain of the N-channel transistor are coupled to charge the second capacitor.

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23. The reset circuit of claim 18 wherein the first terminal is a power supply rail and the second terminal is a ground rail.

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24. A power-on reset circuit comprising:
a power connection (110);
a ground connection;
an output node A;
a first capacitor (120) coupled between the power node and the output node;





first and second transistors (150, 152) coupled in series between the power connection and the ground connection, the first and second transistors coupled together at a node B;

5 third and fourth transistors (140, 142) coupled in series between the power connection and the ground connection, the third and fourth transistors coupled together at a node C, the third and fourth transistors each having a gate coupled to node B;

10 a second capacitor (122) coupled between node C and the ground connection;

a first inverter (130) having an input coupled to node C and an output coupled to node A; and

15 a feedback path (160) coupling the output node to gate terminals of the first and second transistors.

25. The reset circuit of claim 24 wherein the first and second transistors (150, 152) are zero threshold voltage N-channel devices.

26. The reset circuit of claim 24 wherein the third transistor (140) is a P-channel device and the fourth transistor (142) is a zero threshold voltage N-channel device.

27. The reset circuit of claim 24 wherein the first and second transistors are zero threshold voltage N-channel devices, the third transistor is a P-channel device, and the fourth transistor is a zero threshold voltage N-channel device.

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28. The reset circuit of claim 27 further including a second inverter (106) having an input coupled to the output node, whereby the output node serves as a reset signal and an output of the second inverter serves as a complement of the reset signal.

29. The reset circuit of claim 28 further including a third inverter (102) having an input coupled to the output of the second inverter (106), and a fourth inverter (104) coupled to an output of the third inverter, whereby the output of the third inverter serves as the reset signal and an output of the fourth inverter serves as a complement of the reset signal.



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