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AN ERROR SUPPRESSING CIRCUIT AND METHOD THEREFOR FOR A PHASE LOCKED LOOP

Abstract of the Disclosure

An error suppressing circuit (301) and method therefor for a phase locked loop (PLL) (300). According to one embodiment of the present invention, a transient condition, for example, a bandwidth switch, in the PLL (300) is detected. The PLL (300) is opened for a period of time (509) responsive to detecting the transient condition. The phase of a reference frequency signal (115) and the phase of a output frequency signal (116 or 117) are synchronized after a lapse of the period of time (509). The PLL (300) is closed responsive to the phase of the reference frequency signal (115) and the phase of the output frequency signal (116 or 117) being synchronized. The present invention advantageously reduces the length of time it takes for the PLL (300) to correct for the phase and frequency error generated by the transient condition, and is capable of operating with various types of PLLs.

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