CLAIMS

1. A method for manufacturing a semiconductor-on-insulator structure, comprising the following steps:

- providing an FD-SOI substrate successively comprising, from its base to its top:
  - a monocrystalline semiconductor substrate having electrical resistivity ranging between 500 Ω.cm and 30 kΩ.cm, an interstitial oxygen content ranging between 20 and 40 old ppma, and having first P- or N-type doping;
  - an electrically insulating layer having a thickness ranging between 20 nm and 400 nm;
  - a monocrystalline semiconductive layer having P-type doping;
- heat treating the FD-SOI substrate at a temperature greater than or equal to 1175°C for a time greater than or equal to 1 hour, in order to form a P-N junction in the monocrystalline semiconductor substrate at a determined depth with respect to the electrically insulating layer,
  - by diffusing P-type dopants from the monocrystalline semi-conductive layer through the electrically insulating layer in said substrate; and
  - if the substrate has P-type doping, forming, in said substrate, heat donors by precipitation of the interstitial oxygen;

in order to form, in the substrate, a first region having N-type doping extending between the base of the substrate and the P-N junction and a second P-doped region located between the first region and the electrically insulating layer.

2. The manufacturing method as claimed in claim 1, wherein the monocrystalline substrate is made of silicon and/or the monocrystalline layer is a silicon layer.

3. The manufacturing method as claimed in claim 1 or claim 2, wherein the FD-SOI substrate is obtained by transferring a layer of a donor substrate onto a recipient substrate, according to the following steps:

- supplying:
  - the donor substrate comprising a monocrystalline semiconductive layer having P-type doping, and an embrittlement zone located in the monocrystalline silicon layer defining the layer to be transferred; and
  - the monocrystalline semiconductor recipient substrate having electrical resistivity ranging between 500 Ω.cm and 30 k Ω.cm, an interstitial oxygen content ranging between 20 and 40 old ppma, and first P- or N-type doping;
- bonding the donor substrate onto the recipient substrate by means of an electrically insulating layer, the thickness of which ranges between 20 nm and 400 nm;

- detaching the donor substrate along the embrittlement zone in order to form the FD-SOI substrate.

4. The manufacturing method as claimed in claim 1 or claim 2, wherein the FD-SOI substrate is obtained by transferring a layer of a donor substrate onto a recipient substrate, according to the following steps:

- supplying:
    - the donor substrate comprising a monocrystalline semiconductive layer having P-type doping; and
    - the monocrystalline semiconductor recipient substrate having electrical resistivity ranging between 500 Ω.cm and 30 kΩ.cm, an interstitial oxygen content ranging between 20 and 40 old ppma, and P- or N-type doping;
- bonding the donor substrate onto the recipient substrate by means of an electrically insulating layer, the thickness of which ranges between 20 nm and 400 nm;
- thinning the donor substrate from the surface opposite the receiver substrate in order to form the transferred layer, so as to obtain the FD-SOI substrate.

5. The method as claimed in claim 3, wherein the embrittlement zone is formed by implanting atomic species in the donor substrate so as to define the transfer layer.

6. The method as claimed in any one of claims 3 to 5, wherein the recipient substrate and the monocrystalline layer of the donor substrate are P-doped with boron.

7. The method as claimed in any one of the preceding claims, wherein the P-N junction is formed at a depth ranging between 1 µm and 5 µm from the electrically insulating layer.

8. The method as claimed in any one of the preceding claims, wherein the electrically insulating layer comprises a silicon oxide layer.

9. A semiconductor-on-insulator structure obtained directly by implementing the manufacturing method as claimed in any one of the preceding claims, wherein said semiconductor-on-insulator structure successively comprises, from its base to its top:

- a monocrystalline semiconductor substrate having electrical resistivity ranging between 500 Ω.cm and 30 k Ω.cm, an interstitial oxygen content ranging between 20 and 40 old ppma, and comprising:
    - a first region comprising N-type doping; and
    - a second region arranged on the first region, comprising P-type doping, the second region being separated from the first region by a P-N junction;

- an electrically insulating layer;
- a monocrystalline semiconductive layer comprising P-type doping.

10. The semiconductor-on-insulator structure as claimed in claim 9, wherein the monocrystalline semiconductive layer is P-doped with boron.

11. The semiconductor-on-insulator structure as claimed in claim 9 or claim 10, wherein the P-N junction is located at a depth ranging between 1 µm and 5 µm from the electrically insulating layer.

12. The semiconductor-on-insulator structure as claimed in any one of claims 9 to 11, wherein the electrically insulating layer comprises a silicon oxide layer.

13. The semiconductor-on-insulator structure as claimed in any one of claims 9 to 12, wherein the monocrystalline substrate is made of silicon and/or the monocrystalline layer is a silicon layer.