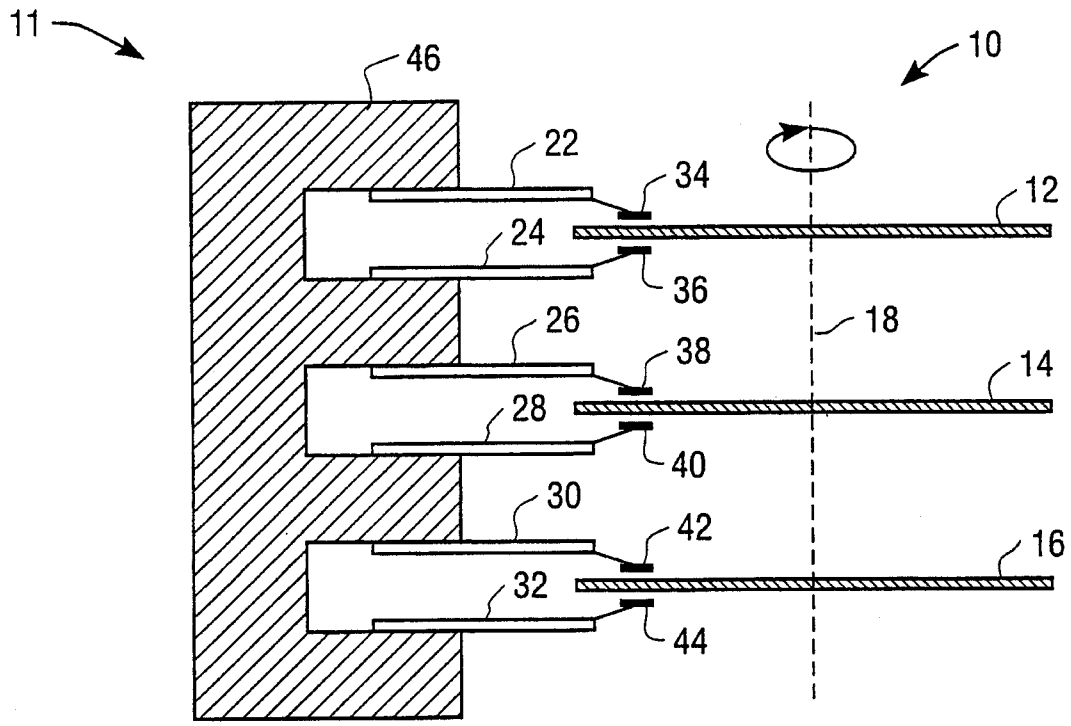


FIG. 1A
(PRIOR ART)

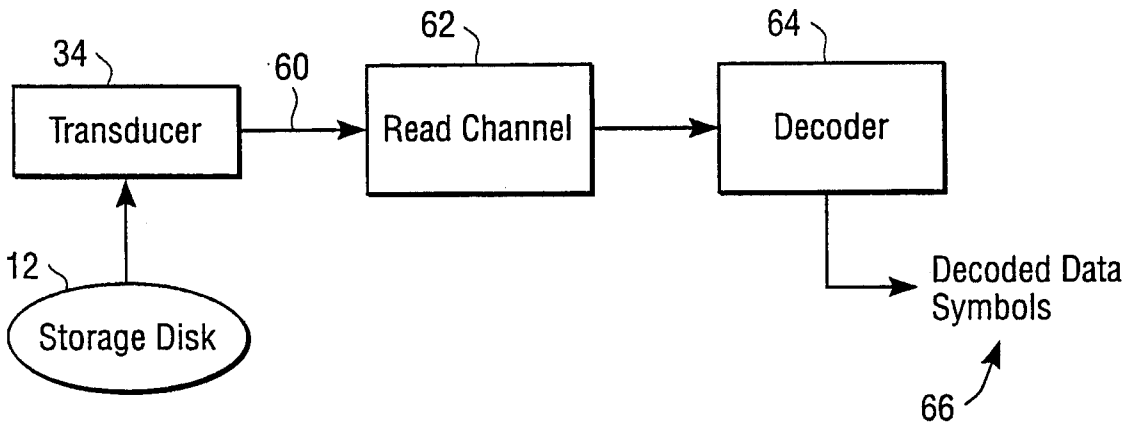


FIG. 2
(PRIOR ART)

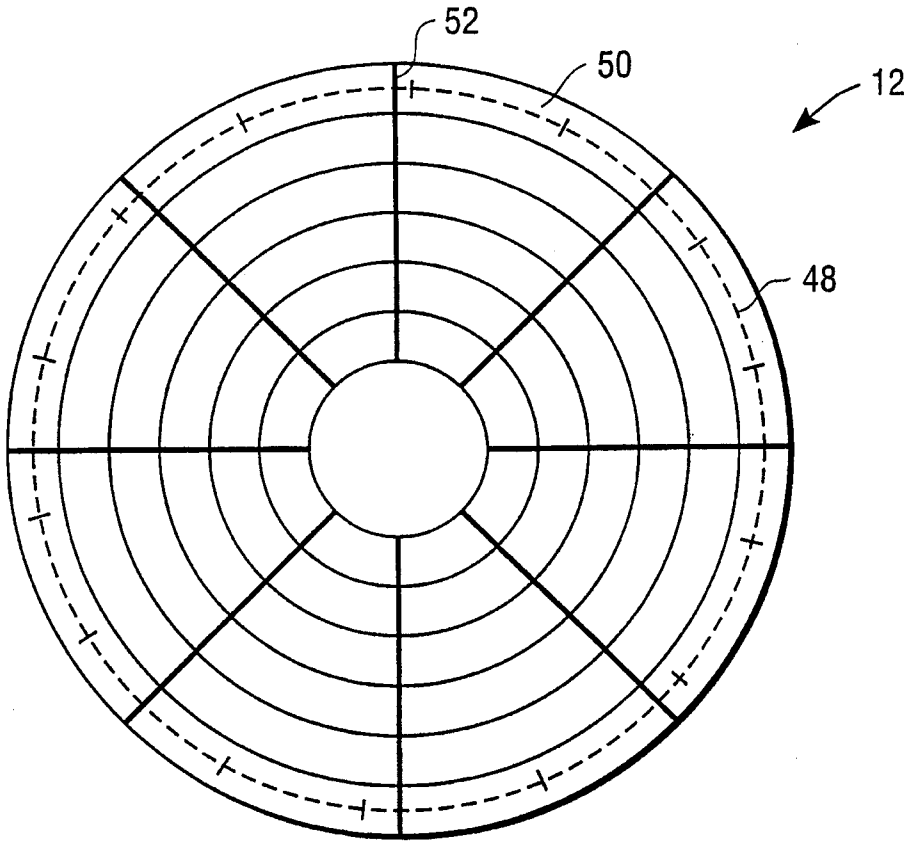


FIG. 1B
(PRIOR ART)

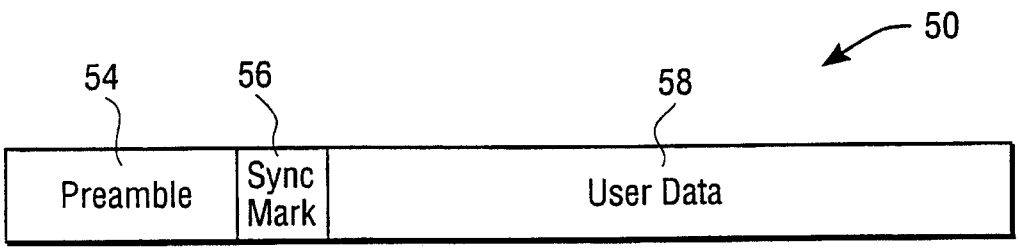


FIG. 1C
(PRIOR ART)

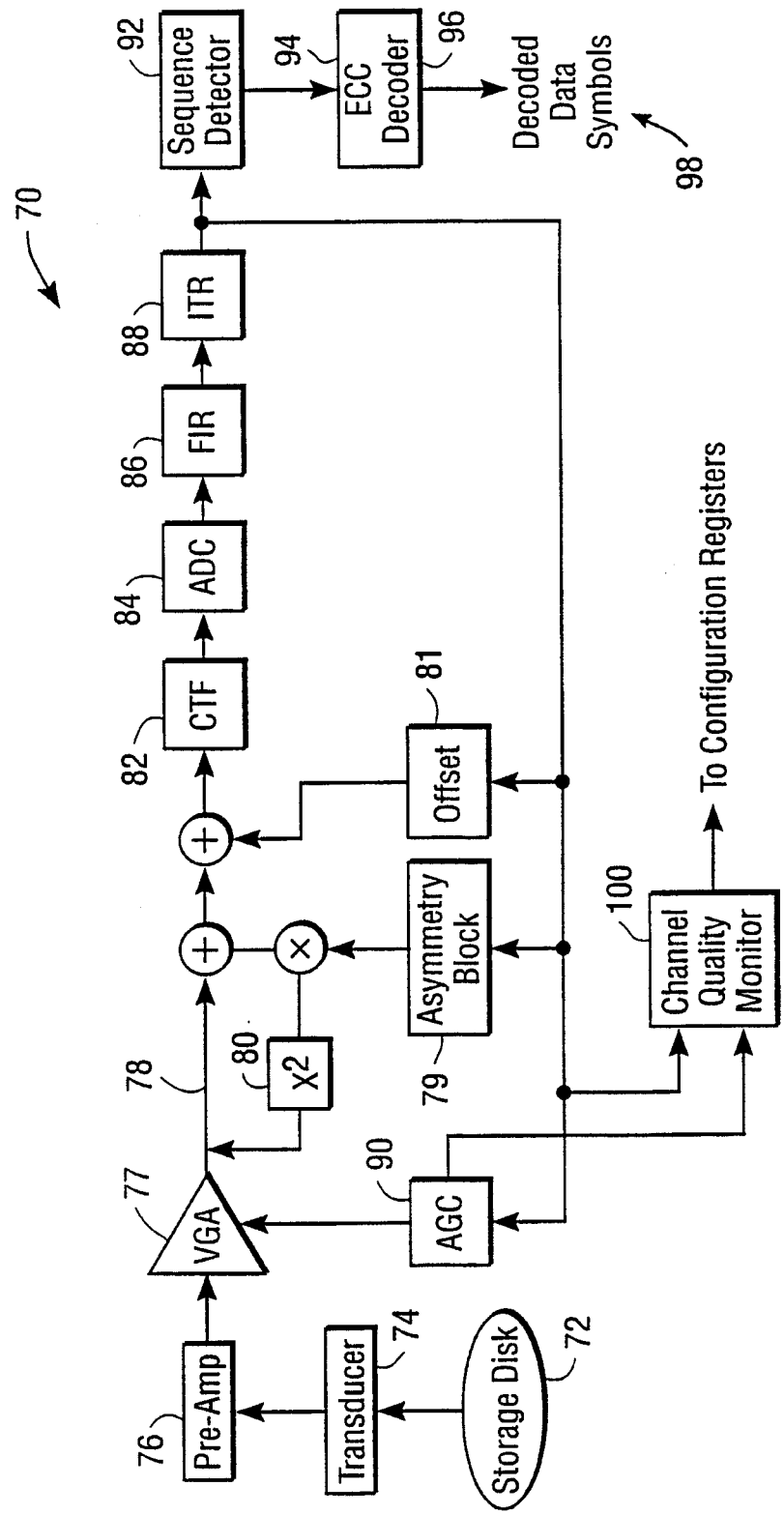

70
Storage Disk
72
Transducer
74
Pre-Amp
76
VGA
77
78
X2
80
Asymmetry Block
79
Offset
81
CTF
82
ADC
84
FIR
86
ITR
88
AGC
90
Sequence Detector
92
94
ECC Decoder
96
Decoded Data Symbols
98
Channel Quality Monitor
100
To Configuration Registers

FIG. 3

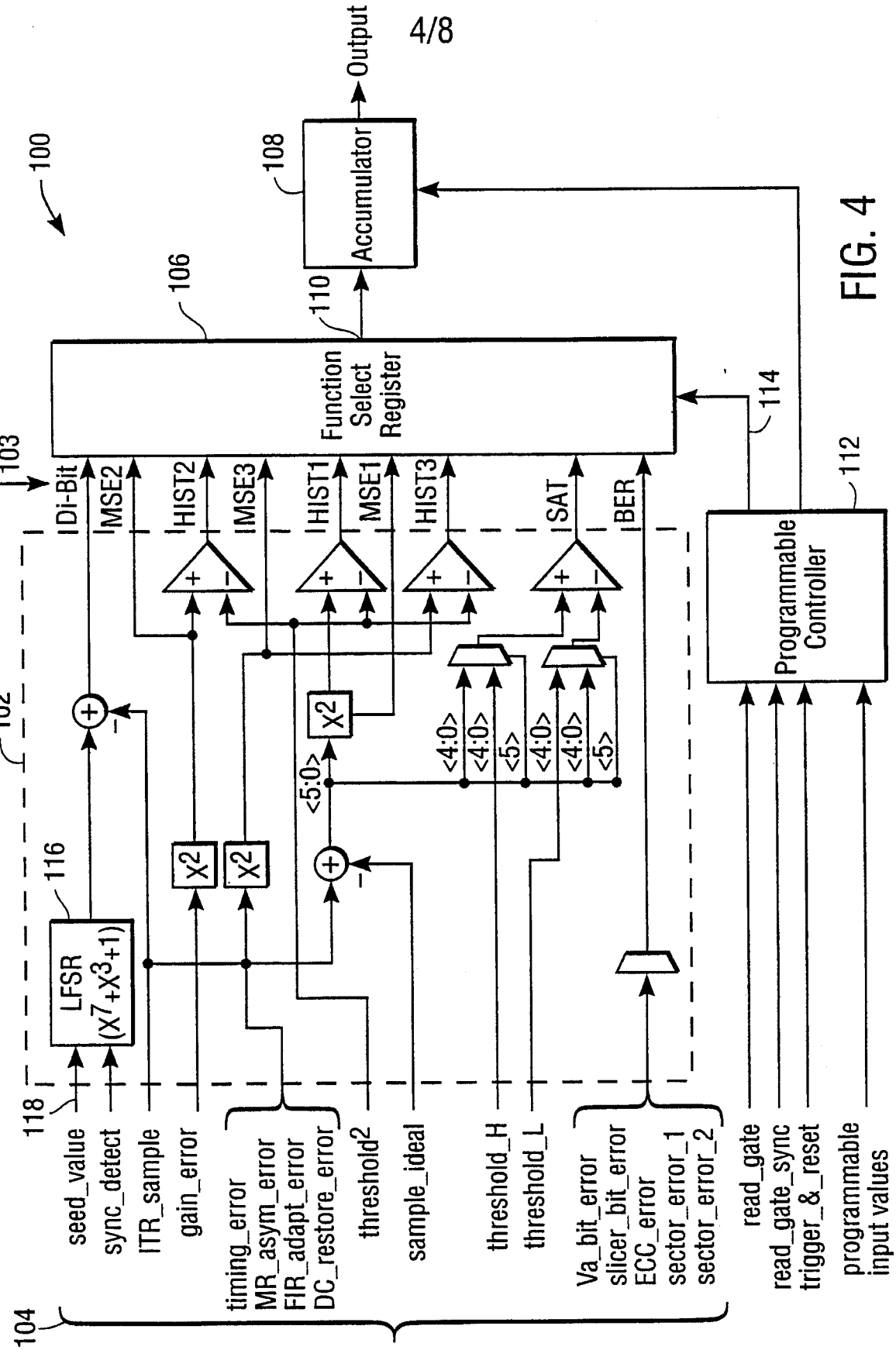

100
Output
108
Accumulator
106
110
Function Select Register
114
103
Di-Bit
MSE2
HIST2
MSE3
HIST1
MSE1
HIST3
SAT
BER
112
Programmable Controller
102
116
LFSR (X7+X3+1)
X2
X2
X2
<5:0>
<4:0>
<4:0>
<5>
<4:0>
<4:0>
<5>
118
seed_value
sync_detect
ITR_sample
gain_error
timing_error
MR_asym_error
FIR_adapt_error
DC_restore_error
threshold2
sample_ideal
threshold_H
threshold_L
Va_bit_error
slicer_bit_error
ECC_error
sector_error_1
sector_error_2
read_gate
read_gate_sync
trigger_&_reset
programmable input values
104

FIG. 4

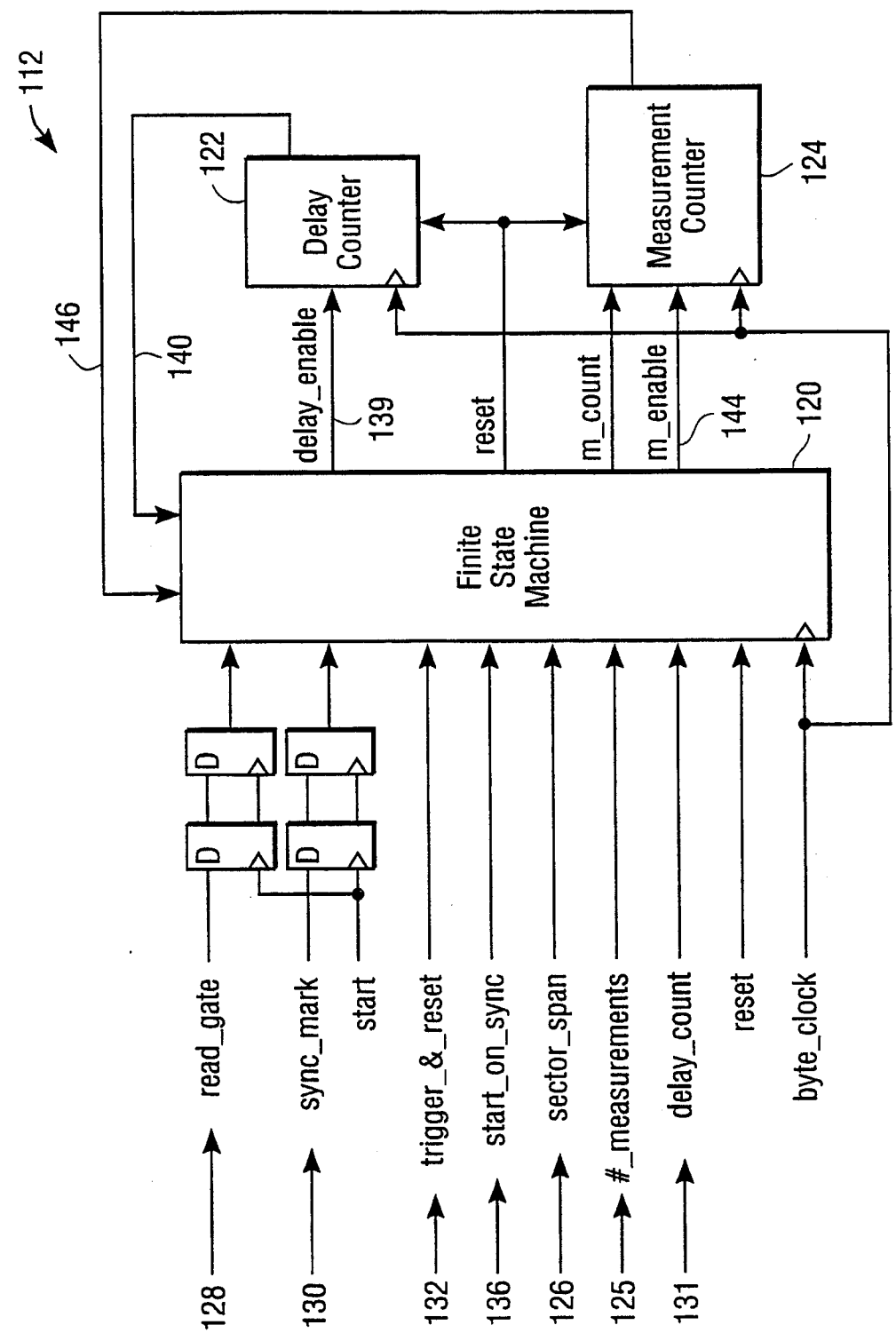

112
146
140
122
Delay Counter
124
Measurement Counter
delay_enable
139
reset
m_count
m_enable
144
120
Finite State Machine
D
read_gate
sync_mark
start
trigger_&_reset
start_on_sync
sector_span
#_measurements
delay_count
reset
byte_clock
128
130
132
136
126
125
131

FIG. 5

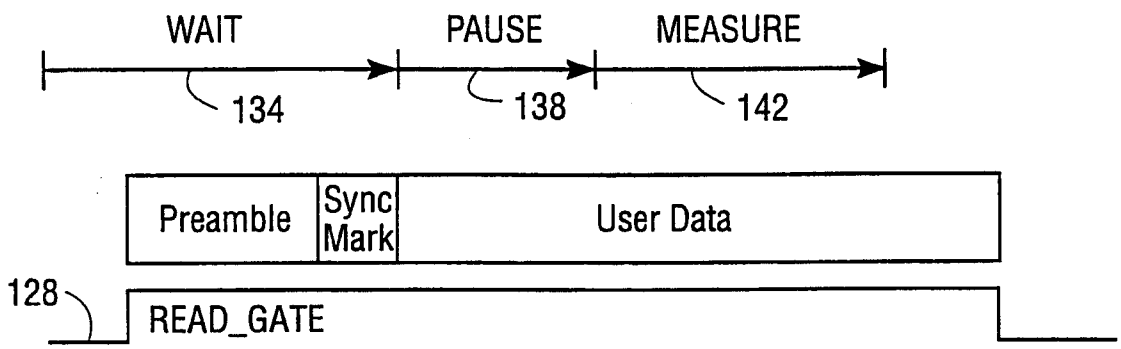


FIG. 7A

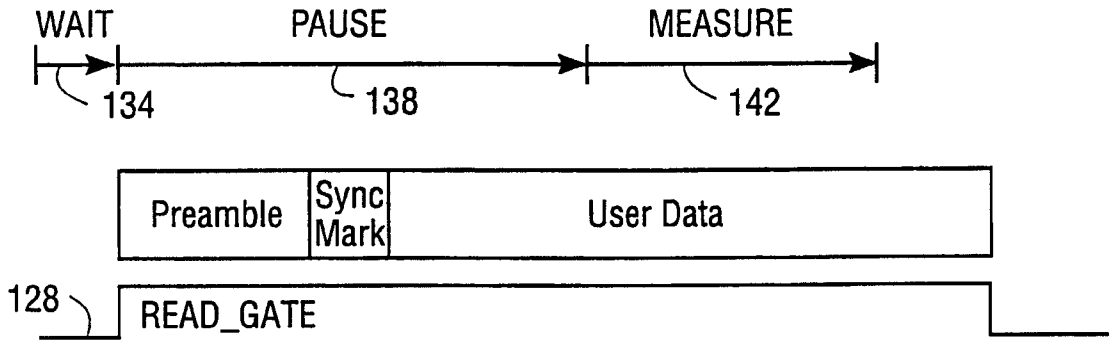


FIG. 7B

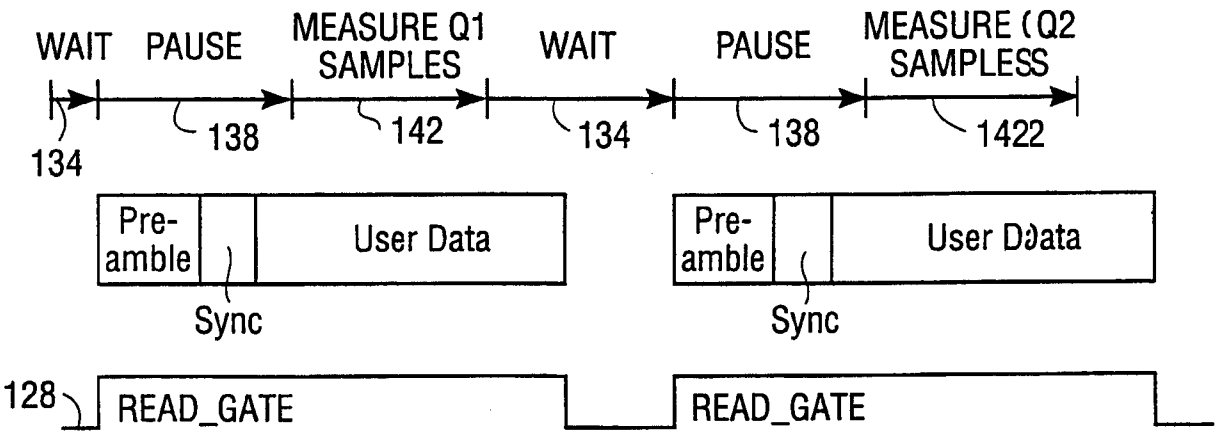


FIG. 7C

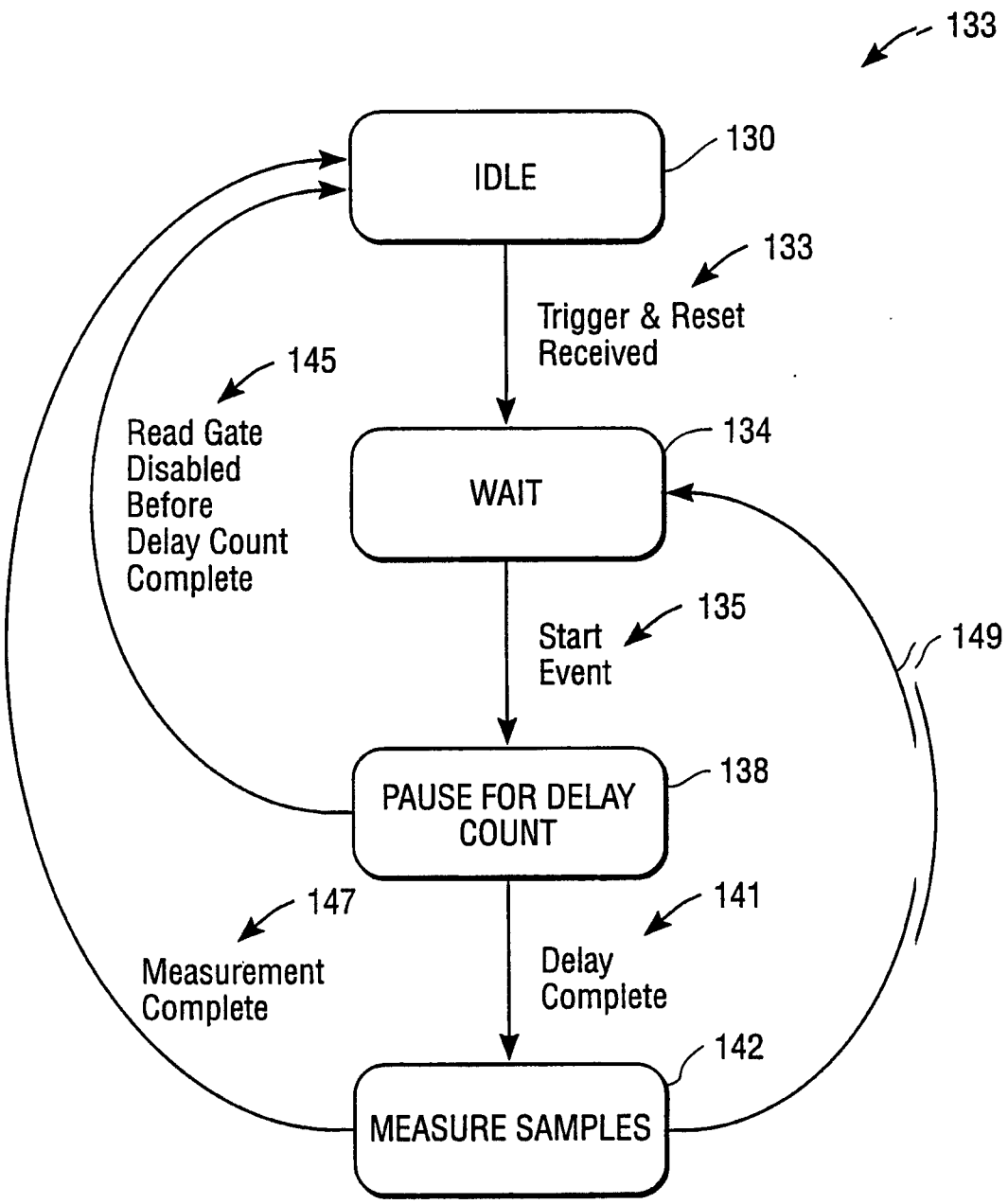

133
IDLE
130
133
Trigger & Reset
Received
145
Read Gate
Disabled
Before
Delay Count
Complete
WAIT
134
135
Start
Event
149
PAUSE FOR DELAY
COUNT
138
147
Measurement
Complete
141
Delay
Complete
142
MEASURE SAMPLES

FIG. 6

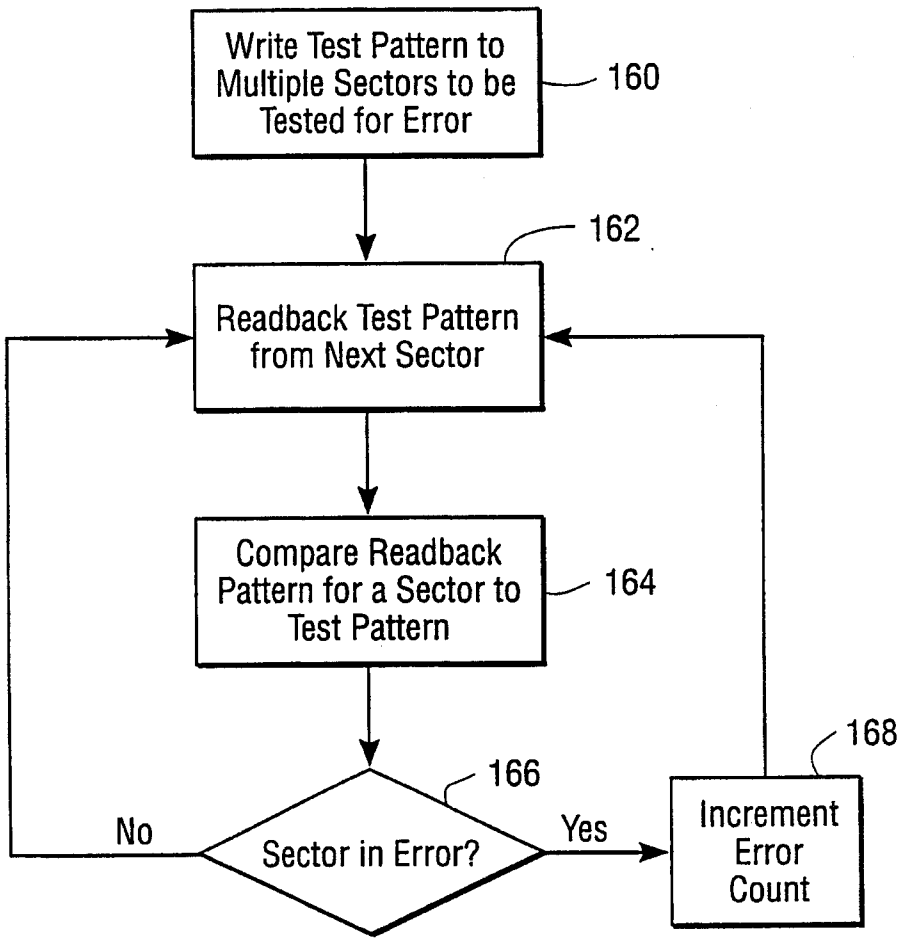

Write Test Pattern to Multiple Sectors to be Tested for Error
160
162
Readback Test Pattern from Next Sector
Compare Readback Pattern for a Sector to Test Pattern
164
166
Sector in Error?
No
Yes
168
Increment Error Count

FIG. 8